APPLIED PHYSICS LETTERS **93**, 112103 (2008)

Electrical transport properties of wafer-fused p-GaAs/n-GaN heterojunctions

Chuanxin Lian,[1] Huili Grace Xing,[1,a)] Yu-Chia Chang,[2] and Nick Fichtenbaum[2]
[1]*Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556, USA*
[2]*Department of Electrical and Computer Engineering, University of California, Santa Barbara, California 93106, USA*

(Received 4 March 2008; accepted 25 August 2008; published online 15 September 2008)

GaAs/GaN *pn* heterojunction diodes have been fabricated by direct wafer fusion and characterized by capacitance-voltage (*C-V*) measurements and temperature dependent current-voltage (*I-V*) measurements. The wafer-fused *pn* diode showed a good rectifying behavior, but a small turn-on voltage was observed, which was attributed to defect-assisted tunneling-recombination. The flat-band voltage extracted from *C-V* is around 0.46 V, much smaller than the built-in voltage calculated for an ideal GaAs/GaN *pn* heterojunction. A band diagram including interface charge effects together with a possible energy barrier, stemming from a layer of disordered material at the fused GaAs/GaN interface, has been proposed to explain the experimental observations. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2983648]

Hybrid integration using wafer fusion can combine optimal properties of different material systems, offering unique device characteristics that are otherwise unobtainable by either of the single materials involved. The AlGaAs/GaAs/GaN heterojunction bipolar transistor (HBT) is such an example, which could potentially take advantage of the high emitter injection efficiency of AlGaAs/GaAs, short transit time in p-type GaAs, and high breakdown voltage of GaN, and thus is a promising candidate for high speed, high power applications. Wafer-fused AlGaAs/GaAs/GaN HBTs were reported by Estrada *et al.*[1] (current gain of ~2) and us (current gain of ~5 to 20).[2–4] To further improve the current gain of these HBTs, it is critical to understand the band alignment between the p-GaAs base and the n-GaN collector. In this work, GaAs/GaN *pn* heterojunction diodes fused at 550 °C for 1 h were fabricated and characterized by capacitance-voltage (*C-V*) and temperature dependent current-voltage (*I-V*) measurements. Defect-assisted tunneling-recombination was found to be the predominant conduction mechanism at low forward bias. A band diagram taking into account the interface barrier and interface charges was proposed based on the experimental observations.

The GaAs wafer in this study was grown by molecular beam epitaxy and GaN by metal-organic chemical vapor deposition. After solvent clean and native oxide removal, the two wafers were joined together in methanol and then annealed at 550 °C for 1 h in a N_2 atmosphere with a background pressure of ~600 mT inside a furnace. During the annealing process, an external pressure of ~5 MPa was maintained on the two wafers. After the two wafers were bonded together, the GaAs substrate was removed and a 100 nm thick p-type GaAs film was obtained on n-type GaN. Nonalloyed Ti/Au and Al/Au were used as Ohmic contacts on p-GaAs and n-GaN, respectively, and the effective device area is 200×200 μm^2. The detailed diode structure is shown in Fig. 1(a). *C-V* were measured using an Agilent 4294A Precision Impedance Analyzer. Temperature dependent *I-V* were measured using an Agilent 4155B Semiconductor Parameter Analyzer and Temptronic ThermoChuck TP03000 between 233 and 353 K.

The energy band diagram of an ideal p-GaAs/n-GaN heterojunction can be constructed by using Anderson's model and assuming the conduction band offset to be 0.3 eV,[5] as shown in Fig. 1(b). Since GaAs in this work is much more heavily doped than GaN, the heterojunction can be treated as a one-sided junction. By plotting $1/C^2$ versus V, a linear line is expected and the doping concentration in GaN can be extracted from its slope, while the diffusion potential related to the band bending in n-GaN can be obtained from its intercept with the transverse axis,[6] which should be around 1.6 V as indicated in the band diagram. As for the carrier transport, if thermionic emission is the dominant transport mechanism, electrons in n-GaN need to gain sufficient energy to pass over the barrier at forward bias, and the *I-V* ideality factor should be close to unity and independent of temperature.

Figures 2(a) and 2(b) display the measured *C-V* and *I-V* characteristics of the wafer-fused p-GaAs/n-GaN heterojunction diode, respectively. It can be seen that $1/C^2$ is a linear function of the applied voltage and the calculated ionized doping concentration in n-GaN is 2.45×10^{16} cm^{-3}, close to what is obtained from the C-V measurements of Schottky diodes fabricated on n-GaN cleaved from the same wafer. The capacitance at zero bias is 23.5 pF, revealing a depletion region width of 134.0 nm in GaN. From the doping

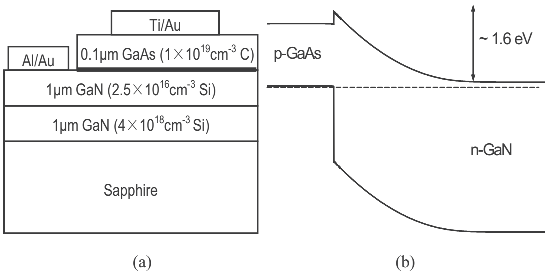
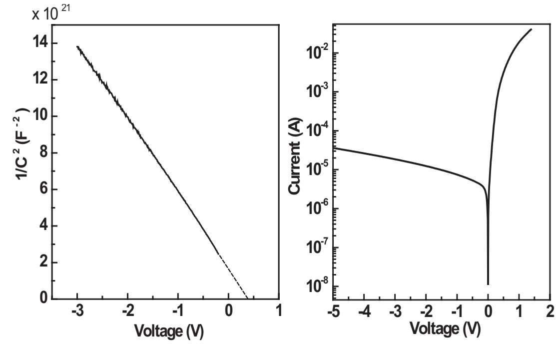


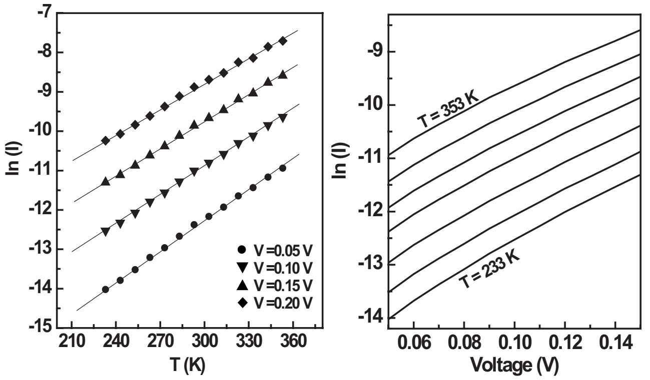
FIG. 1. (a) Detailed GaAs/GaN *pn* diode structures and (b) band diagram of an ideal GaAs/GaN *pn* heterojunction assuming an ideal interface and a conduction band offset of 0.3 eV.

[a)] Electronic mail: hxing@nd.edu.



(a) (b)

FIG. 2. (a) $1/C^2$ vs V and (b) *I-V* of wafer-fused GaAs/GaN heterojunctions measured at room temperature.



(a) (b)

FIG. 3. (a) Semilog plot of current vs temperature at different applied voltages and (b) semilog plot of current vs voltage at different temperatures.

concentration and depletion region width, the band bending in GaN was calculated to be 0.46 eV, consistent with the flat-band voltage (0.46 V) obtained by extrapolating $1/C^2$ to zero. The extracted diffusion potential is surprisingly small compared with the abovementioned theoretical prediction (1.6 V). It was pointed out by Donnelly and Milnes[7] that charged interface states can affect the apparent diffusion voltage obtained by extrapolating $1/C^2$ to zero. Therefore the extracted small diffusion potential indicates the possible existence of considerable interface charges/states at the fused GaAs/GaN interface.

The measured *I-V* shows typical rectifying effects and the current increases exponentially at small forward bias. By fitting the *I-V* using the empirical equation

$$I = I_s[e^{q(V-IR)/nkT} - 1], \tag{1}$$

where I_s is the saturation current, q is the electron charge, R is the series resistance, n is the ideality factor, k is Boltzmann's constant, and T is the absolute temperature, the ideality factor was found to be ~1.75 at room temperature, indicating that there are recombination and/or tunneling currents. But direct band to band recombination currents or tunneling currents should be negligible considering the large bandgap of GaN and the wide depletion region in GaN. It is worth noting that the current becomes sufficiently large when the forward bias is only about 0.25 V, much smaller than the predicted diffusion potential of 1.6 V, as shown in Fig. 1(b). Similar abnormal small "turn-on" voltage has been reported on p-SiC/n-GaN heterojunctions, and it is attributed to the defect-assisted tunneling current formed by electrons from the conduction band of GaN tunneling into the valence band of SiC through midgap defect levels and recombining with the holes there.[8,9]

To explore the carrier transport mechanisms in wafer-fused heterojunctions, temperature dependent *I-V* were measured from 233 to 353 K with a step of 10 K. It was found that the current at small forward bias increases with temperature and voltage following approximately $\exp(\beta T + \gamma V)$, where β and γ are constants independent of temperature or voltage. This relationship can be justified by Fig. 3. In Fig. 3(a), the current is plotted versus temperature at different applied voltages. The semilog plots are linear and almost parallel to each other, suggesting the current proportional to $\exp(\beta T)$ at a fixed voltage. Figure 3(b) shows the current versus voltage at different temperatures, indicating the current proportional to $\exp(\gamma V)$ at fixed temperature. Such current dependence on temperature and voltage has been reported in other semiconductor *pn* junctions, and a defect-assisted multistep tunneling-recombination model is usually employed to explain the experimental phenomena.[10–12] If there exist considerable amounts of midgap states in the depletion region of GaN, electrons from the conduction band of GaN can tunnel via these states and recombine with the holes from the valence band of GaAs. Such tunneling process has been often observed in GaN Schottky diodes.[13] The ideality factor extracted from the temperature dependent *I-V* was found to decrease from 1.99 at 233 K to 1.61 at 353 K, indicating that tunneling-recombination currents are more dominant at low temperature, while thermal currents begin to take over as the temperature increases, an observation consistent with the conventional tunneling current theory.[14]

The above analysis on the *C-V* and forward *I-V* characteristics indicates that the band diagram in Fig. 1(b), drawn for an ideal GaAs/GaN interface, is most probably inaccurate. During high temperature annealing employed in the fusion process, impurities and/or defects can migrate and getter at the interface. Dangling bonds can form at the fused interface and thermal expansion mismatch between GaAs and GaN/sapphire can result in strain. All these interface imperfections may induce extra charge sources in addition to the assumed uniform distribution of ionized dopants, modifying the band bending in GaN. Besides, transmission electron microscopy study on wafer-fused GaAs/GaN has revealed the presence of a thin disordered (1–2 nm thick) layer at the bonded interface.[15] Taking into account the extracted small diffusion potential, the interface charges, and disordered material, we redraw the band diagram, as shown in Fig. 4, with the electron transport process illustrated. Since both of the depletion region in GaAs and the interface disordered layer are thin, their contribution to the measured capacitance is negligible. Considerable interface charges significantly lower the band bending in GaN, resulting in a small flat-band voltage measured by *C-V* (~0.46 V). The even smaller observed turn-on voltage indicates that defect-assisted tunneling is significant. We speculate that the interface defects serve as effective recombination centers for electrons either tunneled or thermally emitted from GaN with holes from GaAs.

Under reverse bias, these defect states can also behave as generation centers resulting in high leakage currents [Fig. 2(b)] and low breakdown voltage V_{BR}. We have modeled V_{BR} of GaAs/GaN *pn* heterojunctions using a nonlocal energy model[16] and found a theoretical V_{BR} of ~120 V and an ex-

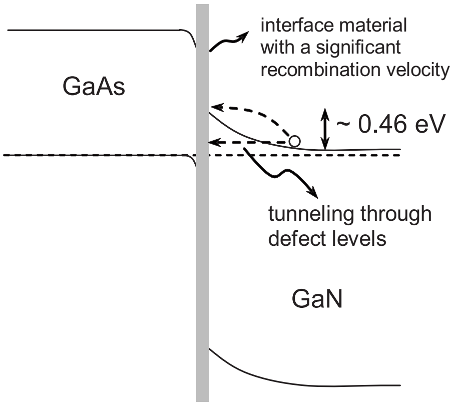


FIG. 4. Energy band diagram of wafer-fused p-GaAs/n-GaN heterojunction including the interface charge effect and disordered material layer.

perimental V_{BR} of ~75 V for the same device structure. In comparison to the V_{BR} of GaAs *pn* homojunctions (~20 V), the higher breakdown voltage of GaAs/GaN *pn* junction confirms the expected advantage of GaN collectors. However, the reverse bias leakage current needs to be reduced by minimizing concentrations of defects within the bandgap, which may be possible by optimizing the wafer fusion process. More investigations, both theoretical and experimental, are currently underway. Despite the abovementioned nonideality at the fused interface, current gain as high as 20 and breakdown voltage (V_{CEO}) of ~35 V have been achieved in fused HBTs with a 30 nm GaAs setback layer.[4] More recently, the first wafer-fused radio-frequency HBT with f_T~2.6 GHz has been fabricated and reported.[17] These experimental demonstrations suggest that it may be possible to minimize the adverse effects of the interface barrier/states to obtain functional devices using wafer fusion.

In summary, GaAs/GaN *pn* heterojunctions have been formed by direct wafer fusion at 550 °C for 1 h. The doping concentration in GaN was calculated reliably from the measured *C-V*. But the extracted diffusion potential energy was found to be much smaller than the band bending in GaN predicted for an ideal GaAs/GaN *pn* heterojunction. *I-V* showed a small turn-on voltage at forward bias and it is attributed to tunneling-recombination currents assisted by midgap defect energy levels. A band diagram taking into account the interface charges and a possible interface energy barrier was proposed to explain experimental observations.

This work is supported by ONR monitored by Paul Maki and Harry Dietrich. The authors are also grateful to Dr. Alan Seabaugh for the electrical measurement instrumentation.

[1] S. Estrada, J. Champlain, C. Wang, A. Stonas, L. Coldren, S. DenBaars, U. Mishra, and E. Hu, *MRS Symposium Proceedings No. 798* (Materials Research Society, Pittsburgh, 2004), Vol. 798, p. Y10.20.1.

[2] C. Lian, H. Xing, C. S. Wang, L. McCarthy, and D. Brown, IEEE Electron Device Lett. **28**, 8 (2007).

[3] C. Lian, H. Xing, C. S. Wang, D. Brown, and L. McCarthy, Appl. Phys. Lett. **91**, 063502 (2007).

[4] C. Lian and H. Xing, Proceedings of the CS MANTECH Conference Digest, 2008, p. 9.4.

[5] C. G. Van de Walle and J. Neugebauer, Nature (London) **423**, 626 (2003).

[6] A. M. Goodman, J. Appl. Phys. **36**, 1411 (1965).

[7] J. P. Donnelly and A. G. Milnes, IEEE Trans. Electron Devices **14**, 63 (1967).

[8] J. T. Torvik, C. Qiu, M. Leksono, and J. I. Pankove, Appl. Phys. Lett. **72**, 945 (1998).

[9] E. Danielsson, C. M. Zetterling, M. Östling, A. Nikolaev, I. P. Nikitina, and V. Dmitriev, IEEE Trans. Electron Devices **48**, 444 (2001).

[10] A. R. Riben and D. L. Feucht, Int. J. Electron. **20**, 583 (1966).

[11] E. G. Dierschke and G. L. Pearson, J. Appl. Phys. **41**, 329 (1970).

[12] V. Roberts and D. W. E. Allsopp, Semicond. Sci. Technol. **11**, 1346 (1996).

[13] L. S. Yu, O. Z. Liu, Q. J. Xing, D. J. Qiao, S. S. Lau, and J. Redwing, J. Appl. Phys. **84**, 2099 (1998).

[14] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), Chap. 5, p. 264.

[15] J. Jasinski, Z. Liliental-Weber, S. Estrada, and E. Hu, Appl. Phys. Lett. **81**, 3152 (2002).

[16] C. Lian and H. Xing, Phys. Status Solidi C **5**, 1989 (2008).

[17] C. Lian, X. Xing, P. Fay, H. Xing, Y.-C. Chang, and Z. Chen, Proceedings of the 66th Device Research Conference Digest, 2008 (unpublished), p. 209.