

## MATCHING NETWORK DESIGN AND CIRCUIT LAYOUT

### Lab #8

In this laboratory session and the associated out-of-lab computer-aided design work, the design of input and output matching networks in order to maximize the gain of the amplifier will be performed and the designs verified using computer simulations. After correct operation has been achieved in the simulation, the designs will be converted into a board layout and exported for fabrication.

#### Pre-lab Data Analysis and Matching Network Design

Using the simulation results from the end of Lab 7, design input and output matching networks at both the input and output at your assigned design frequency. Be sure to check the stability of your transistor in the vicinity of your design frequency; if it is unconditionally stable, then a simultaneous conjugate match is appropriate for a maximum-gain design. Conditionally-stable transistors require more care; mapping the input and output stability circles to find suitable regions is often a useful approach. If you've been assigned to design an LNA, a good target for the source match is the maximum gain that gives a noise figure of 0.5 dB larger than  $NF_{min}$ . For the noise parameters for LNA design, use the values given in the datasheet for the transistor type you're using. You may use single-stub, double-stub, quarter-wave transformer, or any combination of matching networks you choose. Be aware, however, that some designs may result in unacceptably large boards--you should try to minimize the size of your board whenever possible to minimize loss and other undesirable effects. A good size for a final board is around 6 inches long and 4-5 inches tall for 1 GHz designs, while higher-frequency designs should be smaller to minimize loss. If possible, use open-terminated stubs for your design; making a low-inductance, repeatable short-terminated stub is somewhat more difficult in practice. In working through your design, be alert for a few things:

- a.) Work through the design of the chosen topology by hand first, before going to the computer, to make sure there are no surprises. You may also wish to sanity-check your hand calculations using a Smith chart.
- b.) You may find it convenient to use equations on the data display page to calculate conjugate matching conditions, shunt susceptances, stub characteristic impedances, etc. Note: one way to find the complex conjugate is the expression "conj(A)" in ADS. An example data display page that calculates the possible matching networks for a single-stub tuner with quarter-wave transformer section is shown in Figure 1; you may use this as an example of the syntax, etc, for the display page in ADS.
- c.) The characteristic impedances of the matching stubs should be chosen so that the lengths of these stubs are near  $\lambda/8$  or  $3\lambda/8$  (using open-terminated matching stubs). This length restriction is chosen to minimize the sensitivity of the match to the exact length of the stubs.
- d.) Use linecalc to find the width of stubs on your substrate needed to get the desired characteristic impedance for each stub.

- e.) You may use either balanced or unbalanced stubs at your discretion; the use of balanced stubs is often helpful if the width of an unbalanced stub is too wide (i.e. if the width is comparable to or longer than the length).
- f.) Since the matching stubs will be perpendicular to the main input and output lines, be sure that in your design the stubs do not overlap (or aren't too close to) the bias stubs or the transistor. You may need to adjust the length of line between the start of your matching network and the bias stub in order to have enough room; keep in mind that if you do this you must recalculate the simultaneous conjugate match conditions.

### **Matching Network Simulation and Optimization**

- 1.) Enter the matching network designs that you found before lab into the amplifier schematic. Note that if you use MTEE elements to connect the lines and stubs together, you should adjust the length of the stubs downward by  $W/2$  for the main line. This is necessary because the transmission line theory does not account for the finite width of transmission lines; it assumes that all lines are 1-dimensional. Add a length of  $50 \Omega$  line before any matching network on the input and after any matching on the output to allow for the input and output transmission lines. A good length is usually about half an inch.
- 2.) We'll also want to install DC blocking capacitors on the input and output lines to prevent the DC bias of the transistor from being loaded by the source and load, while still permitting the microwave signal to pass unimpeded. A series-resonant capacitor is nearly ideal for this purpose. A pre-made model of the available chip capacitors including the series inductance and layout geometry is available on the course web site in the lab 8 section (filename: capacitor.zap). Download this file, and unarchive it (from the main ADS window chose File/Unarchive Project and select the downloaded file). From the schematic window in ADS, select File/Open, and click on Include/Remove. Browse to find the unarchived project (the default is capacitor\_prj), and click ">>Include>>" to allow this model to be accessed in your design. Note that this file contains models for both 1206 and 0805 sized surface-mount capacitors; be sure to select the correct size for the lab's inventory of capacitors at the value you need. From the design schematic, insert a capacitor of the correct physical size (1206 or 0805) at both the input and output (choose the component library--it looks like a bookshelf) and select subnetwork capacitor. Set the capacitance to the value necessary for self-resonance at your design frequency. Add an additional half inch of transmission line at both the input and output to allow for the mounting of a connector to the board. The result should look something like Figure 2.
- 3.) Simulate the performance of your circuit for a few hundred MHz on each side of your design frequency (e.g. from 500 MHz - 1.5 GHz for a 1 GHz design). It should at least come close to a match at the input and output near 1 GHz; if it does not, double-check your calculations and your schematic entry to find the problem. It is a good idea to engineer the start, stop, and number of points in the simulation so that the simulated frequencies match exactly those frequencies at which you measured the transistor in Lab 7 to minimize interpolation errors.

- 4.) Convert the matching stubs in your design to MLEF elements; these are open-circuited lines with an end-effect model built in to account for the parasitic capacitance at the end of the stub. As a starting point, use the same lengths as you used for the MLIN elements.

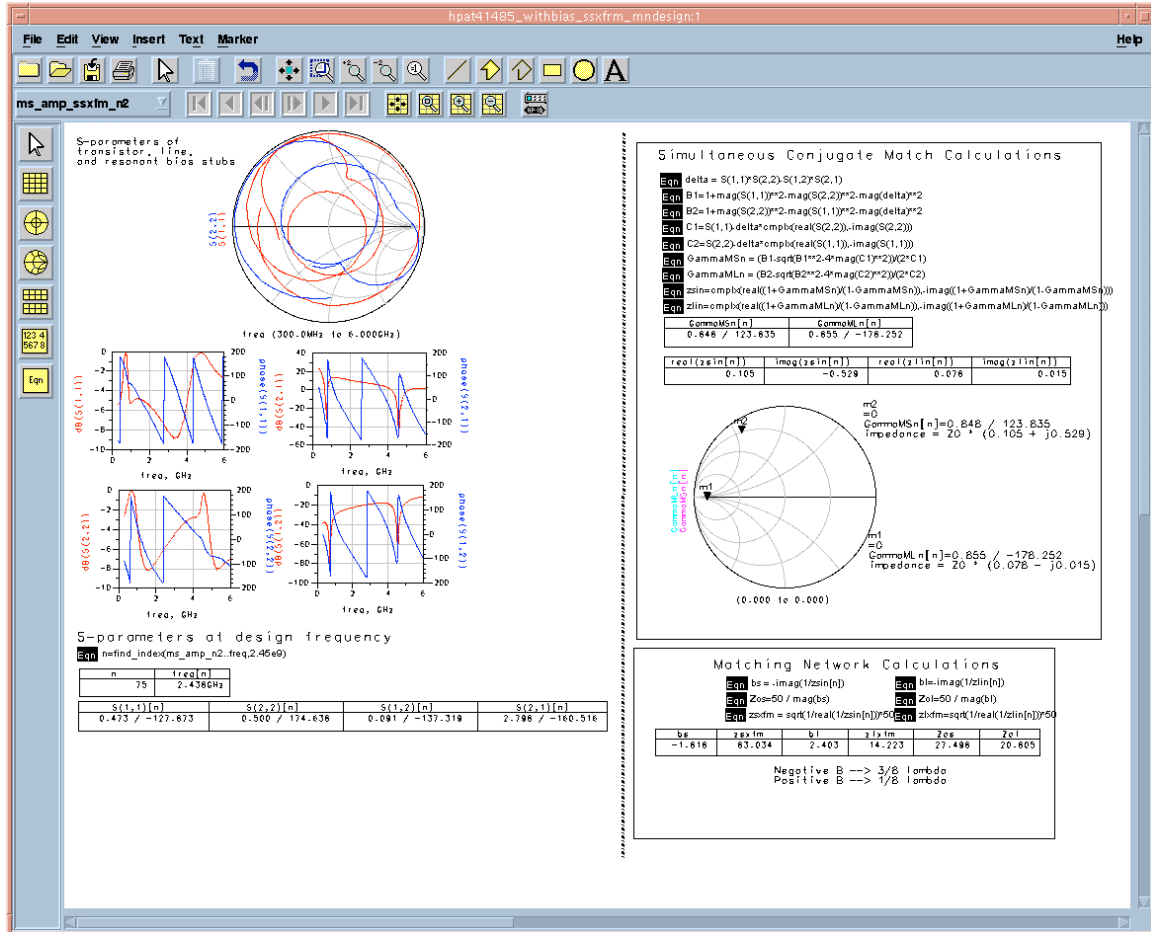


Figure 1. Example data display window with equations.

- 5.) Set up the circuit for optimization of the lengths of the stubs and widths of any  $\lambda/4$  transformers. Set reasonable bounds on these parameters, and devise an optimization scheme to achieve your design. For maximum gain, this corresponds to minimizing  $s_{11}$  and  $s_{22}$  at your design frequency. For an LNA, you want to minimize  $s_{22}$ , but insure that  $\Gamma_s$  is correct for your design. An example schematic for the maximum-gain case is shown in Figure 2--this is not directly applicable for an LNA design. It is often easiest to use variables to set the lengths and/or widths of the transmission lines for optimizations like this, since this way MTEEs and balanced stubs can automatically sized correctly.
- 6.) Update the schematic from the optimization, and re-run the simulation over frequency (you'll need to disable the optimization simulation first). After optimization, the input and output should be in almost perfect agreement with your design targets (e.g. matched for maximum gain) since the optimizer should



- 2.) To lay out the circuit, choose “Layout/Generate/Update Layout.” The starting component should be P1, with a location of 0,0 and an angle of 0. Click OK, and the board should be laid out automatically. Check to make sure no elements are overlapping and that all the stubs you expected to be laid out are there. If everything is OK, save the design.
- 3.) You may wish to add a *small* amount of text to your design to identify it; use the “straight” font with 200 mil lettering on the “cond” layer to do so. Don’t place the lettering too close to any stubs; keep in mind that the letters will be conductive and can affect the performance of the amplifier if they interfere with the electric and magnetic field distributions from the amplifier. Be sure you’ve saved your design; the next step is not reversible.
- 4.) To export the design for fabrication, select File/Generate Artwork. This converts the transmission lines in your design into simple geometric shapes suitable for the fabrication tool. This action will open a new layout window with the converted layout. Save this new design **USING A DIFFERENT FILE NAME** so that you can preserve both the original hierarchical version (with links to the transmission lines in the schematic page) and the new (purely graphical) version.
- 5.) Choose “File/Export” and select the file type as Gerber. Under “Translation Settings” be sure to select “Fill” and “RS274X.” Press Translate when these options have been set, and select “cond” as the layer to convert. Press “View Gerber” to make sure that everything worked out OK. Change from “Outline” to “Fill” mode in the Gerber viewer. If all went well, your design should be a solid block pattern that matches exactly what you laid out--if the rectangles or other shapes appear as outlines or have stripes in them, something has gone wrong. Check the pattern carefully to make sure it matches what you had in the layout window in ADS. If there is any discrepancy, now is the time to find it and fix it.
- 6.) The exported pattern is saved in a file named cond.gbr in the project directory. Email this to pfay@nd.edu, and it will be fabricated for next week’s lab.