

Quilt Packaging: Chip Edge Interconnects for High Performance Electronic Systems Performance

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Interchip communication is often the bottleneck to maximum performance for many electronic systems, including computers, RF electronics, microwaves (radar, imaging etc.), and more. This problem is so important that industry is looking at a variety of solutions to address size, weight, power, and bandwidth limitations including 3D integration (industry wide), Proximity Communications (Sun), Redistributed Chip Packaging (Freescale), optical interconnects (Intel), Neo-Stack (Irvine Sensors), Supercharged Copper (SiliconPipe), and more. We introduce a proprietary alternative to these options, called “Quilt Packaging™” (QP). QP is an edge interconnect scheme that uses novel metal “nodules,” built on the edges of the chips that allow them to electrically mate along their edges. Figure 1 is a micrograph of copper nodules protruding from the edge of a Si chip which, when connected between two ICs, provide a wide-bandwidth, high-speed, and low-power interconnect that also promises a small size and weight system at a lower cost, since fewer packages and board materials are required.

Several, possibly heterogeneous, ICs are placed together along their edges, and the mating nodules are soldered to each other. The completed quilt (see Fig. 2) is treated as if it were a single IC, and can be considered to be a “Metachip™.” The metachip is placed in an inexpensive IC package and connected in a conventional manner, e.g. by wirebonds or solder bumps, or placed on a multichip module substrate for interconnection to the system. The 100’s or 1000’s of nodules represent an additional set of interconnects that would otherwise not have been available for system throughput.

Benefits of QP include, but are not limited to:

- **Heterogeneous integration** of ICs and components fabricated using different processes (e.g. nanotechnology and CMOS)
- **Better thermal control** due to all chips on heat sink
- **Simpler fabrication** than chip stacking
- **High signal bandwidth** with excellent signal integrity
- **Reduced power dissipation and die size** (up to 50%) through reduction of pin I/O drivers and package capacitances
- **Cost reduction** by eliminating some packages and reducing package and board complexities
- **Decreased electrical noise**
- **Thinner profiles compared to chip stacking or PoP**

Coplanar waveguides spanning the gap between two high-resistivity Si substrates connected by QP nodules have been fabricated and tested. Figure 3 shows that the de-embedded insertion loss from 50 MHz to 100 GHz is less than -0.1 dB over the entire range, a world record performance metric. Figure 4 shows how these results compare to other data found in the literature. We believe that QP offers the very lowest chip-to-chip losses of any existing packaging method. Figure 5 shows the latency of less than only 3 ps across chips. These data suggest that QP could improve the performance of both RF and digital systems, and could decrease the cost, size, weight and power of any electronic system using multiple ICs.

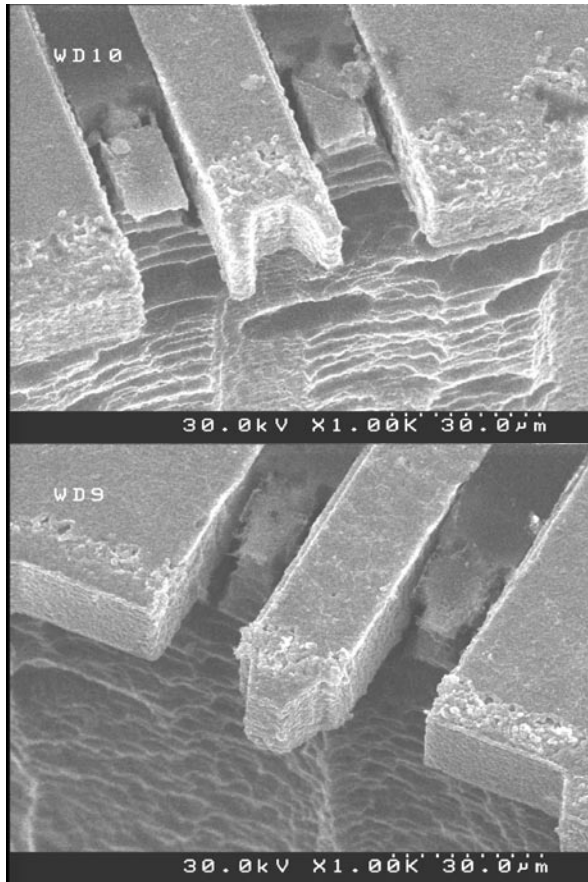


Fig. 1. Electron micrograph of complementary, self-aligning QP nodules. The three nodules form a coplanar waveguide that spans the gap between chips. Similar structures have yielded world-record insertion losses between chips.

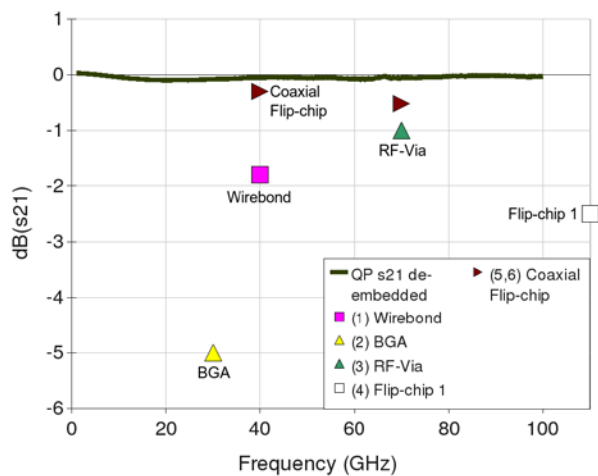


Fig. 4. Comparison of insertion losses from chip to chip with various packaging technologies. Quilt Packaging has no resonances, and is less than -0.1 dB from 50 MHz to 100 GHz, a world record metric.

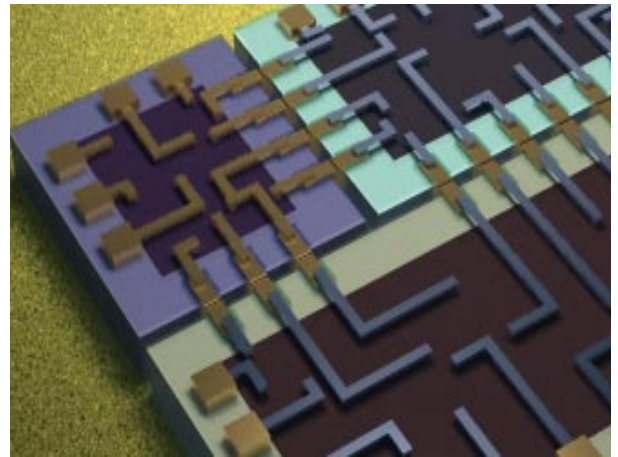


Fig. 2. Drawing of intersection of Quilt Packaged ICs. The chips are butted along their edges, and electrical interconnects are made by copper nodules that are soldered together across the gap. The entire “quilt” is packaged as if it were a single chip.

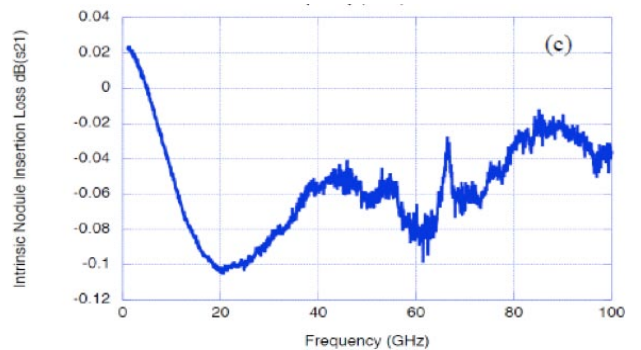


Fig. 3. De-embedded insertion loss of coplanar waveguide spanning two high-resistivity Si substrates.

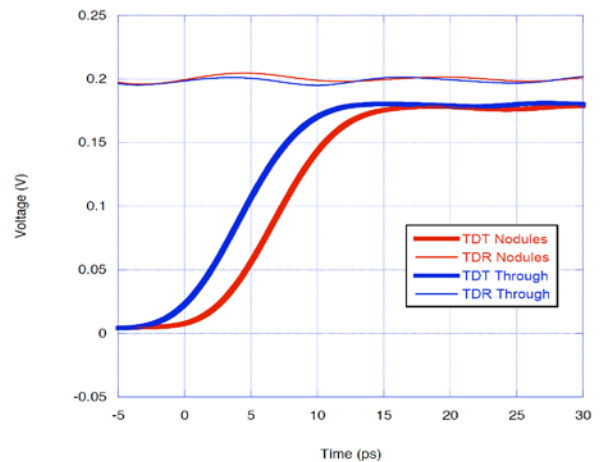


Fig. 5. Time domain data showing latency of less than 3 ps.