

A Novel Scheme for Wide Bandwidth Chip-to-Chip Communications

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Abstract

Quilt Packaging (QP), a novel chip-to-chip communication paradigm for system-in-package integration, is presented. By forming protruding metal nodules along the edges of the chips and interconnecting integrated circuits (ICs) through them, QP offers an approach to ameliorate the I/O speed bottleneck. A fabrication process that includes deep reactive ion etching, electroplating, and chemical-mechanical polishing is demonstrated. As a low-temperature process, it can be easily integrated into a standard IC fabrication process. Three-dimensional electromagnetic simulations of coplanar waveguide QP structures have been performed, and geometries intended to improve impedance matching at the interface between the on-chip interconnects and the chip-to-chip nodule structures were evaluated. Test chips with 100 μm wide nodules were fabricated on silicon substrates, and s-parameters of chip-to-chip interconnects were measured. The insertion loss of the chip-to-chip interconnects was as low as 0.2 dB at 40 GHz. Simulations of 20 μm wide QP structures suggest that the bandwidth of the inter-chip nodules is expected to be above 200 GHz.

Keywords

Chemical-mechanical polishing (CMP), coplanar waveguide (CPW), deep reactive ion etch (DRIE), electroplating, packaging, system-in-package (SiP).

Introduction

As state-of-the-art transistor features shrink to 45 nm or smaller, and incorporate strained and SiGe layers on silicon [1], chip density and performance are improved. However, not all of the performance enhancement can be passed to the system level due to packaging limitations, especially at multi-GHz clock rates [2]. Besides, the demand by consumer electronics for high speed, low power consumption (longer battery life), low cost, and better portability presents challenges to conventional packaging techniques. Several approaches, including system-on-chip (SoC), system-in-package (SiP) [3] and system-on-packaging (SoP) [4][5] have been actively pursued. SoC combines several kinds of functional blocks into one chip to form a complete system that offers the most compact and light-weight design, but also faces the challenges of long design times, integration complexity, low yield, and intellectual property issues. SiP incorporates multiple chips into a single package, which alleviates some of the

problems faced in SoC. There are about 30 IC and packaging companies gearing up to produce SiP-based multichip modules [4]. Some of these technologies being developed to especially address throughput issues include IBM's "Transfer and Join" [6], Sun Microsystem's "Proximity Communications" [7], SiliconPipe's "Off-the-Top" [8], and Freescale's "Redistributed Chip Package" [9]. SoP is a variation of SiP that utilizes thin film technology to combine passives into the package.

We have proposed a novel SiP method, called "Quilt Packaging" (QP) for interconnecting ICs that promises to circumvent the critical speed bottleneck in chip-to-chip communications [10]. Potentially, thousands of small metal nodules can be formed at the chip edges during IC fabrication, and once the ICs are separated the nodules protrude beyond of the edges of the chips as contacts. Chipsets are then connected by butting chips against each other and soldering the nodules. A basic schematic of two chips communicating through QP is shown in Figure 1 (a).

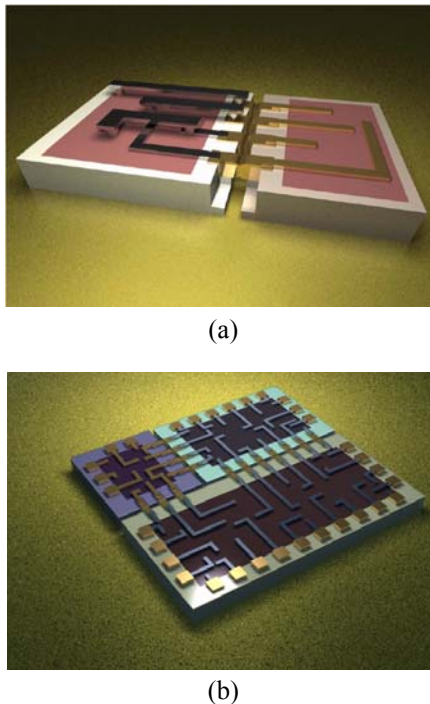


Figure 1. Cartoon representation of: (a) a simple two-chip QP connection, (b) a three-chip QP system.

The notch at the forefront is schematic only and reveals the depth of the metal nodules into the substrate. Figure 1 (b) shows a three-chip system interconnected by QP. The bonding pads shown in the figure (or, alternatively, solder bumps) suggest that QP can be used in combination with existing packaging techniques. Compared with the techniques currently pursued by industry, QP provides the shortest path ($< 50 \mu\text{m}$) between chips and leads to minimum delay, wider bandwidth and lower electrical noise [11]. Additionally, as will be shown in the fabrication process for QP, nodules are defined by standard photolithography and can achieve very high input/output (I/O) density. Furthermore, as much as 50% of generated heat and silicon die area can be attributed to the I/O buffers for high performance application specific integrated circuits. By connecting through QP, package capacitances - and therefore pin drivers - can be eliminated, effecting a reduction in power consumption.

Fabrication of QP

A fabrication process flow for QP structures is presented in Figures 2 (a) - (g). After the IC front-end processing on the wafer is completed, nodules are defined along the edges by standard photolithography processing, and etched by deep reactive ion etching (DRIE) to create trenches for the nodules (Figure 2a). A layer of plasma enhanced chemical vapor deposition (PECVD) SiO_2 is deposited to form an isolation layer inside the trenches between the silicon

substrate and the metal contacts formed later (Figure 2b). A thin Ti/Cu seed layer is then sputtered, and copper electroplating is performed to fill the trenches (Figure 2c).

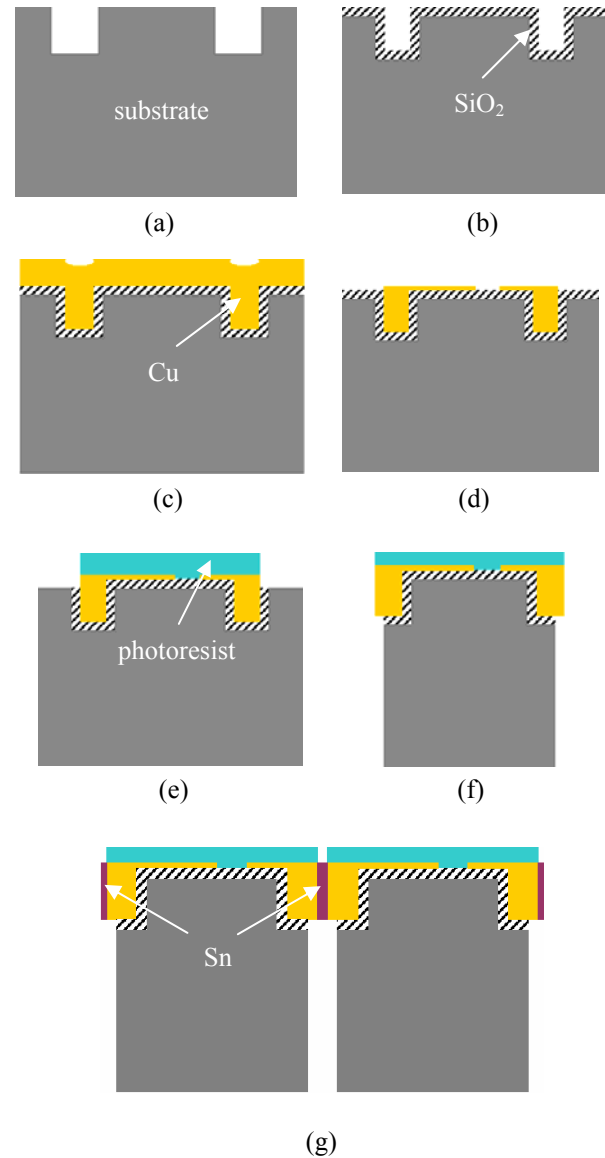


Figure 2. A fabrication process for QP structures. (a) Define and etch nodules by DRIE, (b) passivate trenches by PECVD SiO_2 , (c) sputter Ti/Cu seed layer inside trenches and plate copper to fill the trenches, (d) planarize the nodules by CMP and continue back-end-of-line process to finish ICs, (e) spin thick photoresist as protection layer, open separation area and remove SiO_2 on the surface, (f) use DRIE to separate the chips, (g) electrolessly plate Sn on the nodule sidewall and solder two chips together to form QP structure.

Chemical-mechanical polishing (CMP) is used to planarize the trenches and form the nodules. Subsequent processing to connect nodules with on-chip interconnects is included as part of the conventional back-end-of-line processing (Figure 2d). After the completion of interconnects, a thick photoresist layer is spun onto the wafer and the SiO_2 is etched by buffered HF (BHF) at the open area at the edges for the chip separation (Figure 2e). DRIE etches all the way through the wafer to undercut part of the nodules and separate the chips. The thick photoresist mask is consumed partly in the meantime (Figure 2f). Sn, electrolessly plated on the chips, coats only the copper surface at the protruding nodule sidewall. After stripping the photoresist, two or more chips are connected by soldering them together to form the QP structure (“quilt”) (Figure 2g).

We use the Bosch DRIE process [12], which alternates between an SF_6 etch cycle and a C_4F_8 sidewall passivation cycle. Both anisotropic etching to define the nodules and reentrant etching to expose copper nodules while separating the chips can be achieved by tuning the process parameters [13].

There are at least two ways that die separation for QP can be achieved. The first is called “dicing by thinning” [14][15], in which the wafers are thinned by back side grinding and polishing to separate the dice along the previously-etched trenches on the front side of the wafers. The vertical alignment of nodules depends on the control of wafer thickness after grinding, which is estimated at better than $1\ \mu\text{m}$ [16]. We used the second method, which is to DRIE all the way through the wafer for die separation. Figure 3 shows the cross section of a separated chip that has an undercut profile so as to ensure that the nodules will contact first as the dice are pushed together. The thickness of the wafer shown here is about $600\ \mu\text{m}$. The etch profile was achieved by the Bosch process in an Alcatel A601E inductively coupled plasma etcher with SF_6 flow rate at 300 sccm, C_4F_8 at 130 sccm, with cycle durations at 7 s and 2 s respectively. The automatic pressure control position was at 23%. The plasma was generated by a source power of 1800 W, and the substrate power was 80 W. The temperature on the surface of the wafer during processing was maintained at 20 deg. C.

By using DRIE die separation, the edges of ICs are no longer required to be straight, which is a limitation in conventional dicing saw separation. Self-aligned structures can be formed to help align the chips. Two approaches, interlocking self-aligning silicon structures and keyed copper nodules, were demonstrated. The devices we tested used the keyed nodules approach. Figures 4 (a) - (d) show scanning electron micrographs (SEMs) of released keyed copper nodules of test chips with substrate undercut. The Cu nodule thickness is about $20\ \mu\text{m}$.

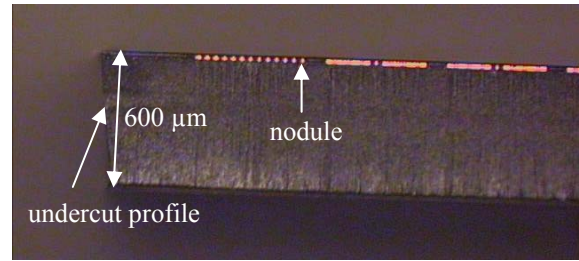


Figure 3. Cross section of separated chips shows undercut profile.

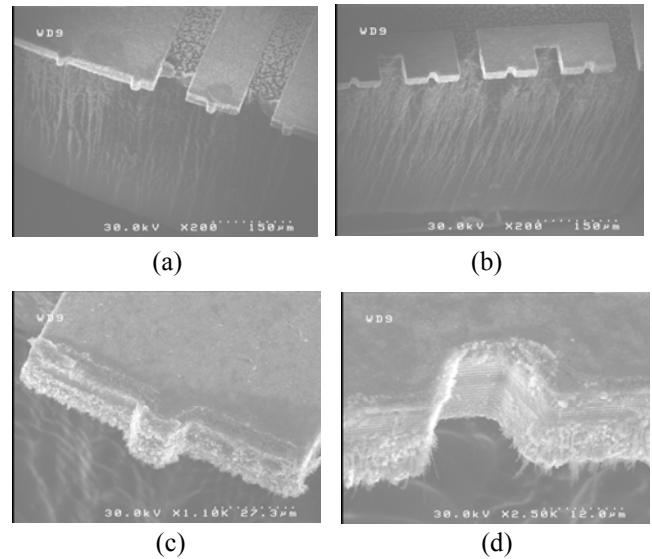


Figure 4. Released keyed copper nodules protruding from the die to form contacts. (a) and (b) show 100 μm wide nodules and (c) and (d) show magnified alignment structures.

Shown in Figure 2 (e), the thick positive photoresist used as the protection mask layer was AZ® P4620 spun four times to form a layer about $16\ \mu\text{m}$ thick, which was sufficient to survive the long DRIE die-separation step. The electroless Sn plating solution is from Transene. Figure 5 shows die photos of two chips connected through QP. Coplanar waveguide (CPW) microwave test patterns were fabricated. The center signal lines have widths of $100\ \mu\text{m}$ (Figure 5a). A closer look at the CPW QP connection is shown in Figure 5 (b). The detailed design of CPW QP prototypes will be discussed below.

The fabrication of QP is a low-temperature process, and can be easily integrated into a standard IC fabrication process. Only two additional masks, one for defining the nodules and the other one for die separation, are needed.

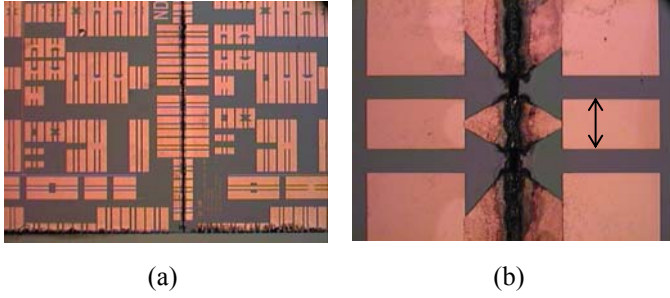


Figure 5. (a) Micrographs of two QP CPW prototype chips connected through nodule structures with a signal line width of 100 μm , and (b) a closer look at the QP nodules at the interface between the dice. The arrow represents 100 μm .

Microwave Measurements and Simulations

Since the QP structure results in a short extension of interconnects from one chip to another in almost the same planar geometry, the electromagnetic discontinuities inherent in conventional wire-bond or flip-chip packaging technologies can be nearly eliminated, which leads to resonance-free, high-speed interconnects that minimize signal and ground bounce, overshoot and ringing. The only sources of electromagnetic discontinuity in QP interconnects are from the thick, short copper nodules ($\sim 80 \mu\text{m}$ per chip) inlaid inside the silicon substrate and the nodule bridge between the two chips ($< 25 \mu\text{m}$ per chip).

Three CPW QP geometries along with on-chip interconnect (without nodules), as shown in Figure 6, were fabricated. Figure 6 (a) is a “simple QP” prototype. Figure 6 (b) is “QP improved 1,” which has a tapered nodule signal line to reduce capacitance and improve impedance matching between the on-chip interconnect and the nodule structure. Figure 6 (c) is “QP improved 2,” which has both a tapered signal nodule and a tapered ground plane to further reduce the interface discontinuity. Figure 6 (d) is a simple on-chip interconnect built for comparison of the effects introduced by the inlaid nodules. Figure 6 (e) is a closer look at Figure 6 (c). The symbols are the on-chip signal line length (l_o), on-chip signal line width, which is the same as the signal nodule width (W_o), spacing between on-chip signal line and ground plane (S_o), inlaid nodule length (l_n), nodule bridge length, which is the spacing between two chips (S_a), spacing between signal nodule and ground nodule (S_n), nodule width at the interface of on-chip interconnect (W_i), and recessed ground nodule width (W_{gr}).

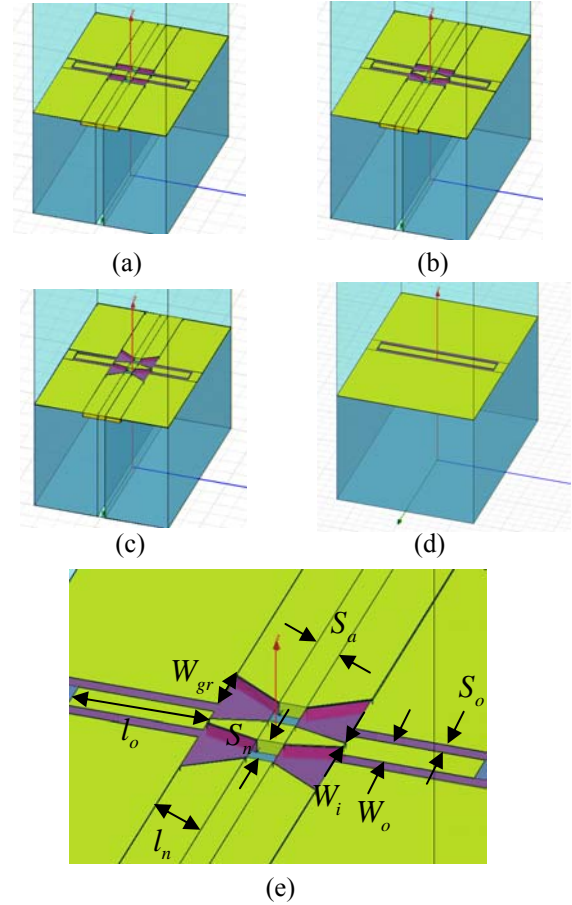


Figure 6. Prototypes in Ansoft HFSS: (a) “simple QP,” (b) “QP improved 1,” (c) “QP improved 2,” (d) on-chip interconnect, (e) a closer look at “QP improved 2”.

The silicon substrate has a relative permittivity of 11.9, resistivity of about $10 \Omega \cdot \text{cm}$, and thickness of around $600 \mu\text{m}$. The isolation SiO_2 has a thickness of $1 \mu\text{m}$. The metal (Cu) on-chip interconnect is $0.6 \mu\text{m}$ thick. The depth of the nodules for both signal and ground is about $20 \mu\text{m}$. Test chips with signal nodule widths of $100 \mu\text{m}$ were fabricated following the processes described in Figure 2, except for one variation. Instead of soldering by melting plated Sn, the chips were pushed together, fixed in place, and about $2 \mu\text{m}$ of electroless Sn was plated at the interfaces to ensure good electrical contact. The connections in Figure 5 were made with this variation. The QP geometries are summarized in Table I. QP structures I, II, III correspond to simple QP, QP improved 1 and QP improved 2, respectively, as shown in Figures 6 (a) - (c).

On-wafer s-parameters of the QP interconnects were measured from 100 MHz to 40 GHz. Measured on-wafer open and short test structures were used to de-embed the effects of the on-chip interconnects. S_{11} and S_{21} of the

nodule interconnects are shown in Figure 7. In all cases, the “improved” QP geometries provide better impedance matching and loss characteristics than the “simple QP” structure. A better than 18 dB return loss and less than 0.2 dB insertion loss at 40 GHz are achieved.

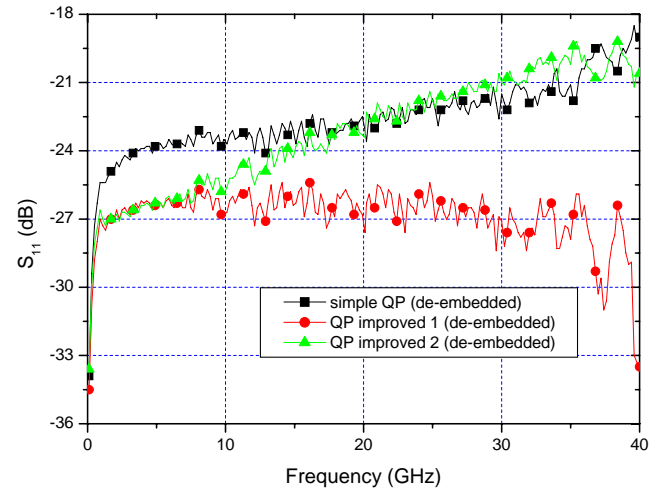
Table I
Dimensions of the 100 μm QP interconnects (Unit: μm)

	100 μm QP geometries		
	I	II	III
l_o	200	200	200
W_o	100	100	100
S_o	35	35	35
l_n	80	80	80
S_a	40	40	40
S_n	50	50	50
W_i	100	10	10
W_{gr}	0	0	95

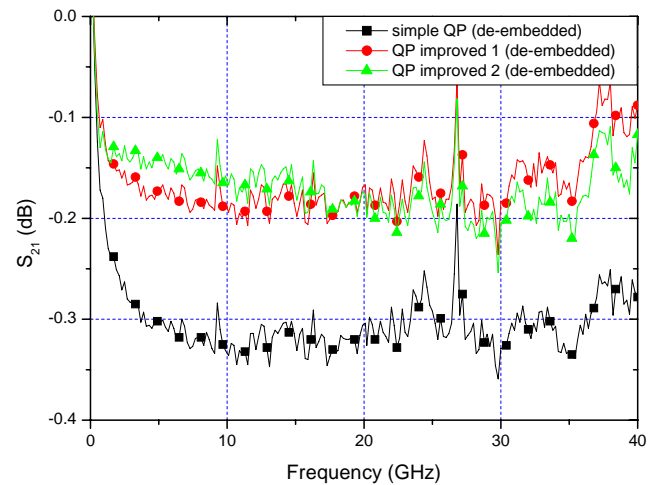
Quilt Packaging offers a highly-optimized chip-to-chip interconnect in terms of performance and overall benefits. In a system using QP technology, signals that originate near the edges of the dice need to traverse a very short distance between them, so that latency would be extremely low. A worst-case scenario would be signals that originate deep in the interior of a chip and must terminate deep within the receiving chip. Even in such cases, the combination of using a low-loss upper metal level interconnect in conjunction with QP will offer a significant advantage over a “standard” signal path through a solder bump to a package substrate and back again. The advantage to QP is that the connection between ICs is now direct without the need to traverse package structures such as leads, bumps, and package wiring.

Here, we compare our measured performance of QP to alternative structures. Devlin et al. [17] showed that a 25.4 μm (1 mil) diameter, 0.3 nH bond wire introduced an insertion loss of 2 dB at 40 GHz. Braunisch et al. [18] demonstrated solder joints with an insertion loss of more than 1 dB at 40 GHz. When considering the die-package interface with additional pad capacitance ($C = 300$ fF), the insertion loss at 40 GHz increased to about 4 dB. Mantysalo and Ristolainen [19] investigated stacked 3-D package interconnects. A single solder-plated polymer ball introduced 0.3 dB insertion loss and 15 dB return loss at 10 GHz, while a ball-via-ball structure introduced more than 0.5 dB insertion loss and about 12 dB return loss at 10

GHz. Pfeiffer and Chandrasekhar [20] showed that a 30 μm high, 90 μm wide gold stud bump for flip-chip interconnects introduced 0.35 dB insertion loss at 30 GHz. Above 30 GHz, the insertion loss was predominated by the onset of a structural resonance. Banerjee and Drayton [21] designed and measured both monolithic (on the same substrate) and hybrid (on different substrates, similar to QP) packages built on high-resistivity silicon substrates ($> 2000 \Omega \cdot \text{cm}$) using double aluminum wirebonds. The insertion loss due to the wirebonds was 0.15 dB for the monolithic package at 50 GHz and 0.5 dB for the hybrid package at 40 GHz, respectively.



(a)



(b)

Figure 7. (a) Return loss (S_{11}) and (b) insertion loss (S_{21}) of 100 μm QP structures after de-embedding.

Lahiji et al. [22] presented low-loss multiwafer vertical interconnects built on 100 μm thick, high-resistivity silicon ($> 2000 \Omega \cdot \text{cm}$) and GaAs substrates. At 20 GHz, the vertical vias in the two silicon designs showed 0.12 and 0.38 dB insertion loss and 12.9 and 17.3 dB return loss, respectively, and in the GaAs design, insertion loss was 0.2 dB and return loss was 13.6 dB. It is not surprising that excellent performance was obtained in 3-dimensional packaging systems, given the short distances involved in these direct chip-to-chip interconnects. Considering the costs and benefits of the myriad options in chip-to-chip interconnects, QP offers extremely high performance as well as many other advantages [10].

From Figure 7, we see that the insertion loss has a moderate increase at low frequencies (< 3 GHz). This is attributed to dielectric loss in the low-resistivity substrate. QP interconnects fabricated on high-resistivity substrates ($\sim 8000 \Omega \cdot \text{cm}$) do not exhibit this low-frequency dispersion.

It should be noted that due to the 100 μm nodule size, the characteristic impedance of the QP interconnects is not optimized. For the nodules, $Z_0 \approx 47 \Omega$, and so the measured insertion loss and return loss include the effects for this modest impedance mismatch.

Table II
Dimensions of the 20 μm QP interconnects (Unit: μm)

	20 μm QP geometries		
	I	II	III
l_o	200	200	200
W_o	20	20	20
S_o	10	10	10
S_n	20	20	20
l_n	80	80	80
S_a	40	40	40
W_i	20	2	2
W_{gr}	0	0	25

QP structures with 20 μm wide signal nodules on low- and high-resistivity silicon substrates were simulated over a broader frequency range (1 – 200 GHz) using a three-dimensional full-wave electromagnetic simulator [23]. The detailed dimensions used in the simulations are listed in Table II. QP structures I, II and III again correspond to the simple QP, QP improved 1 and QP improved 2, respectively.

Figure 8 shows the simulated return loss and insertion loss of the CPW QP structures after de-embedding. The insertion loss is less than 1.2 dB over the whole frequency range, which demonstrates that the bandwidth of QP structures is expected to be well beyond 200 GHz.

We are now working on the fabrication of QP structures with 50 μm and 20 μm wide nodules for measurements up to 110 GHz.

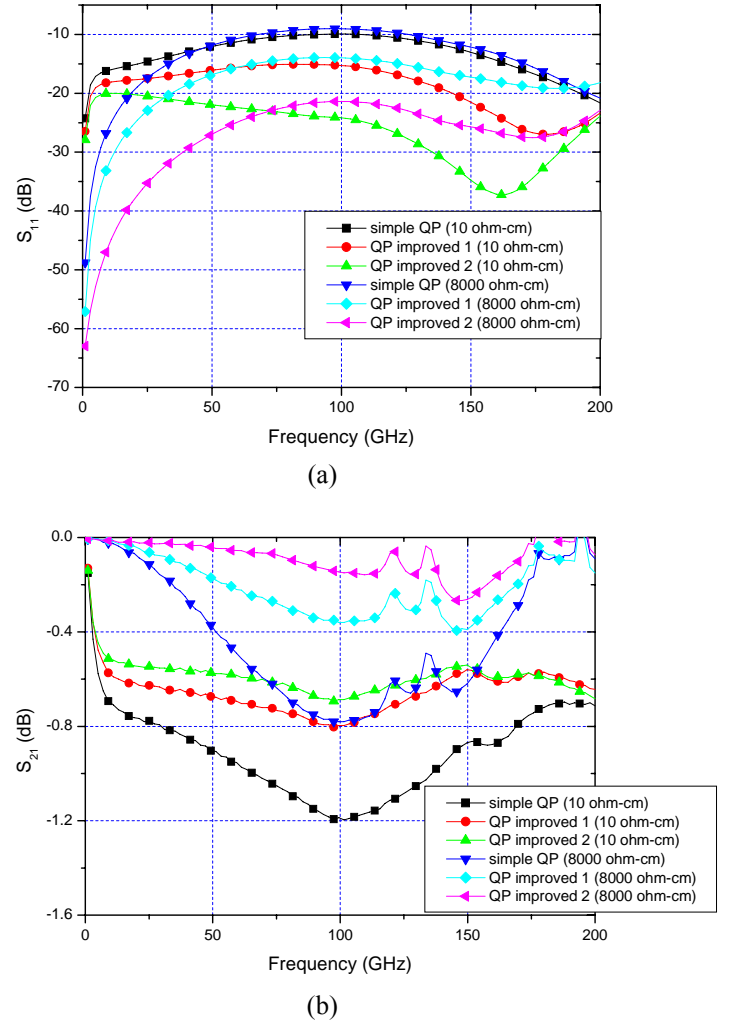


Figure 8. (a) Return loss (S_{11}) and (b) insertion loss (S_{21}) of 20 μm QP structures after de-embedding.

Conclusions

A novel inter-chip communication paradigm, Quilt Packaging (QP), for SiP is presented. QP uses protruding metal nodules fabricated during the IC fabrication process to form inter-chip contacts. A low-temperature fabrication process is demonstrated. To reduce the discontinuity between on-chip interconnect and nodule structures,

tapered nodule signal and ground lines were designed and fabricated. Test patterns with 100 μm wide signal nodules were measured up to 40 GHz. On low-resistivity silicon substrates (10 $\Omega \cdot \text{cm}$), insertion loss as low as 0.2 dB was measured. High-resistivity silicon substrates can eliminate most of the dielectric loss and improve insertion loss. Our data confirm that the QP interconnect scheme is capable of wide-band chip-to-chip communications.

Nodules are defined by standard photolithography and DRIE. There is no physical limit preventing nodules from scaling down to or below 20 μm wide. Simulations show that the bandwidth of QP is well above 200 GHz. Reliability issues including thermal conductivity and expansion, and mechanical strength of QP require further investigation.

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References

- [1] R. Chou, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros and M. Metz, "Silicon nano-transistors and breaking the 10 nm physical gate length barrier," *Proc. 61st Device Research Conf.*, pp. 123-126, Salt Lake City, June, 2003.
- [2] *International Technology Roadmap for Semiconductors (ITRS)*, 2005 Edition, SIA.
- [3] T. Sakurai, "Superconnect technology," *IEICE Trans. Electron.*, vol.E84-C, no. 12, 2001, pp. 1709-1716.
- [4] R.R. Tummala, "SOP: what is it and why? A new microsystem-integration technology paradigm - Moore's law for system integration of miniaturized convergent systems of the next decade," *IEEE Trans. Adv. Packag.*, vol. 27, no. 2, May 2004, pp. 241-249.
- [5] R.R. Tummala, M. Swaminathan, M.M. Tentzeris, J. Laskar, G. Chang, S. Sitaraman, D. Keezer, D. Guidotti, Z. Huang, K. Lim, L. Wan, S.K. Bhattacharya, V. Sundaram, F. Liu and P.M. Raj, "The SOP for miniaturized, mixed-signal computing, communication, and consumer systems of the next decade," *IEEE Trans. Adv. Packag.*, vol. 27, no. 2, May 2004, pp. 250-267.
- [6] K.W. Guarini, A.W. Topol, M. Jeong, R. Yu, L. Shi, M. R. Newport, D.J. Frank, D.V. Singh, G.M. Cohen, S.V. Nitta, D.C. Boyd, P.A. O'Neill, S.L. Tempest, H.B. Pogge, S. Purushothaman, and W.E. Haensch, "Electrical integrity of state-of-the-art 0.13 μm SOI CMOS devices and circuits transferred for three-dimensional (3D) integrated circuit (IC) fabrication," *Proc. Int'l. Electron Device Meeting*, 2002, pp. 943-945.
- [7] R.J. Drost, R.D. Hopkins, and I.E. Sutherland, "Proximity communication," *Proc. IEEE 2003 Custom Integrated Circuits Conf.*, 2003, pp. 469-472.
- [8] J. Fjelstad, "Novel interconnection technology for high speed chip to chip signal transmission," Available: <http://www.sipipe.com/docs/NovelInterconnectionTechnologyJ.pdf>.
- [9] K.J. Johnson, Available: www.freescale.com/files/abstract/overview/FTF2006_PE101.pdf.
- [10] G.H. Bernstein, Q. Liu, Z. Sun, and P. Fay, "Quilt-packaging: a new paradigm for inter-chip communication," *Proc. IEEE 7th Electronics Packaging Technology Conference*, 2005, pp. 1-6.
- [11] S.W. Song, M. Ismail, G. Moon, and D.Y. Kim, "Accurate model of simultaneous switching noise in low voltage digital VLSI," *Proc. 1999 IEEE Int. Symp. on Circ. and Sys.*, 1999, pp 210-213.
- [12] R.B. Bosch GmbH, U.S. Pat. 4855017, U.S. Pat. 4784720, and Germany Pat. 4241 045C1, 1994.
- [13] K.S. Chen, A.A. Ayon, X. Zhang, and S.M. Spearing, "Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (DRIE)," *J. Microelectromech. Syst.*, vol. 11, no. 3, 2002, pp. 264-275.
- [14] C. Landesberger, G. Klink, G. Schwinn, and R. Aschenbrenner, "New dicing and thinning concept improves mechanical reliability of ultra thin silicon," *Proc. 2001 IEEE Int. Symp. And Exhibition on Advanced Packaging Materials*, 2001, pp. 92-97.
- [15] G. Klink, M. Feil, F. Ansorge, R. Aschenbrenner, "Innovative packaging concepts for ultra thin integrated circuits," *Proc. 51st IEEE Electronic Components Conference*, 2001, pp. 1034-1039.
- [16] Available: <http://www.thatcorp.com/datashts/grinddata.pdf>.
- [17] L.M. Devlin, G.A. Pearson, A.W. Dearn, and S. Williamson, "28GHz multi-chip modules," Available: www.plextek.com/papers/mm_paper.pdf.
- [18] H. Braunisch, K.P. Hwang, and R.D. Emery, "Compliant die-package interconnects at high frequencies," *Proc. IEEE Electronic Components and Technology Conference*, 2004, pp. 1237-1243.
- [19] M. Mantysalo and E.O. Ristolainen, "Modeling and analyzing vertical interconnections," *IEEE Trans. Adv. Packag.*, vol. 29, no. 2, May 2006, pp. 335-342.
- [20] U.R. Pfeiffer and A. Chandrasekhar, "Characterization of flip-chip interconnects up to millimeter-wave frequencies based on a nondestructive *in situ* approach," *IEEE Trans. Adv. Packag.*, vol. 28, no. 2, 2005, pp. 160-167.
- [21] S.R. Banerjee and R.F. Drayton, "Wafer level interconnects for 3D packaging," *Proc. IEEE Electronic Components and Technology Conference*, 2004, pp. 1513-1518.
- [22] R.R. Lahiji, K.J. Herrick, Y. Lee, A. Margomenos, S. Mohammadi, and L.P.B. Katehi, "Multiwafer vertical interconnects for three-dimensional integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 6, 2006, pp. 2699-2706.
- [23] *Ansoft High-Frequency Structure Simulator (HFSS)*, Ansoft, Inc., Pittsburgh, PA.

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