Quilt Packaging: High-Density, High-Speed Interchip Communications

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***Abstract*—“Quilt Packaging” (QP), a new superconnect paradigm for interchip communication, is presented. QP uses conducting nodules that protrude from the vertical facets of integrated circuits to effect a dense, fast, and reduced-power method of interfacing multiple die together within a package or on a multichip module. The concept of QP is presented along with a discussion of advantages over traditional system-on-chip and other system-in-package technologies. A process flow and results of chip fabrication are detailed. Simulations show expected signal propagation between adjacent die of greater than 200 GHz, and measurements of interconnected chips confirming low losses and resonance-free operation to at least 40 GHz have been achieved.**

***Index Terms*—Bonding, chemical-mechanical polishing (CMP), chip-to-chip interconnection, copper plating, deep reactive ion etching (DRIE), multichip module (MCM), packaging, superconnect, system-in-package (SiP), system-on-chip (SoC), wafer-scale-integration (WSI).**

I. INTRODUCTION

THIS PAPER addresses issues of communications among integrated circuits (ICs), a bottleneck to the continued development of electronic systems. We introduce a novel method of interconnecting ICs that improves multiple metrics of system performance including bandwidth, system size and weight, power consumption, and potentially cost. The proposed superconnect technology, which we call “Quilt Packaging” (QP) [1], is a method of electrical communication among ICs with a reduced need for signals to propagate through packages or supporting printed wiring board substrates. QP uses conductive “nodules” that protrude horizontally from the vertical facets at the periphery of ICs, providing a means of a direct interconnection between ICs in a “quilt”-like fashion.

The success of the microelectronics industry has been so dramatic that it is difficult to concede that the continued pace of progress may begin to slow. In fact, with the advent of strained and SiGe layers on silicon, the demonstration of functioning 10-nm-long complementary metal oxide semiconductor (CMOS) gates [2], and other technological feats, it appears as if scaling of ICs may carry on for some time. As the performance of ICs continues to improve, the system-level performance has not kept up. In fact, while on-chip clock speeds increased from about 750 MHz in 1997 to about 3.6 GHz in 2004[1] , the off-package speed in microprocessor-based systems increased only from about 250–800 MHz (the 2004 data are for the Intel Xeon processor). Although this off-package speed is but a modestly smaller fractional increase than the on-chip clock speed, clearly the off-chip bottleneck is worsening. Hence, much of the performance gain made possible by the aforementioned technological advances may be underutilized at the system level. Speaking to this point, the High End Computing Revitalization Task Force’s report for the Workshop on the Roadmap for the Revitalization of High-End Computing states, “Off-chip interconnections for high-end systems remains our greatest concern. Even today, off-chip electronic connections are inadequate because they degrade chip clock frequencies by an order of magnitude or more.” [3]

The 2003 International Technology Roadmap for Semiconductors (ITRS) addressed the importance of packaging in continued system development as follows.

> The technology boundaries between semiconductor technology, packaging technology, and system technologies in electronics are blurring. Package designs no longer can be developed independently of the chip and system; they must be considered concurrently as part of the overall system design. As a result, a broad range of complex design parameters must be analyzed to optimize the complete system, and trade-offs among chip, package, and system are required.

We are aware of several efforts by industry and others to address the problems described above.

1) Sun Microsystems is developing “Proximity Communications,” [4] in which signals are coupled between chips via capacitive links. This approach has several possible disadvantages compared to QP: a) the capacitive links have limited signal bandwidth compared to QP; b) the links require transceiver circuits that take up chip real estate; c) the chips are laid face-to-face in two planes so that the capacitive links are physically contiguous, the result of which is that heat dissipation from the plane that is elevated from the package substrate may be impeded; and d) additional interposers are required to route direct current (dc) and low frequency signals. In a similar vein, using alternating current (ac)-coupling between chips via board structures, Luo

Manuscript received March 28, 2006; revised February 12, 2007. This work supported in part by the Defense Advanced Research Projects Agency (DARPA) under Contract NBCH3039003 and in part by the National Science Foundation (NSF) under Grant CCF-0515392.

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Digital Object Identifier 10.1109/TADVP.2007.901643

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[1] http://www.itrs.net

et al. [5] report data rates of 3 Gb/s/channel with power dissipation of 15 mW/channel, while Miura *et al.* [6] report an inductive inter-chip wireless superconnect functioning at a data rate of 1 Gb/s/channel at about 6 mW/channel.

2) SiliconPipe, Inc., is developing a technology for system-level interconnections based on impedance-matched, air-dielectric transmission lines running directly between ICs.[2] When compared with QP's direct interconnection between ICs, this approach suffers from the added complexity and cost of the long transmission line components and their limited bandwidth.
3) IBM has developed an interposer technology much like a thin, fine-pitch multichip module (MCM) that can be stacked on a conventional MCM [7], [8]. While it has been shown to have good performance, fabrication and assembly of this "Transfer and Join" process is complex. Complementary to this approach is Intel's bumpless buildup layer packaging (BBUL) [9], in which the die are embedded in a builtup package structures without bumps. This approach offers electrical performance improvements over conventional approaches, at the expense of increased process complexity.
4) Direct chip-to-chip electrical connections achieved by hand-applied wirebonds and careful integrated circuit (IC) edge lapping have been shown to provide good propagation characteristics to over 100 GHz [10]. This approach suffers from both a lack of manufacturing throughput, a low number of interconnects, and somewhat lower ultimate bandwidth, as will be discussed below.
5) Beam-lead packaging has some similarities to QP in that the beam-lead conductive tabs extend beyond the edge of the die, but are intended to interface to a package. A microbeam lead technology has been demonstrated [11] that incorporates the microbeams in the dielectric above the semiconductor substrate, and seeks to improve the lead density. QP, instead, is designed to directly interface ICs without intervening packages.

In this paper, we present our QP technique and further discuss its benefits relative to existing proposed solutions to the off-chip communications problem.

II. BENEFITS AND APPLICATIONS OF QP

Fig. 1 is a rendering showing three die connected together by QP. The three die are silicon or other semiconductor substrate in which nodules have been made to extend directly out of the sides of the chips. Using an appropriate die attach fixture, the die are pushed together and bonded so that signal paths are formed, routing up to thousands of high-speed signals between chips. Bonding could be achieved by ultrasonic welding, laser welding, or—as we demonstrate in Section III below—soldering. Alignment for the nodules could be performed by the external fixturing, or by other methods of self-aligned nodules and chip structures that alleviate some of the accuracy requirements, as discussed below. The completed quilt could be installed either in a package or on an MCM. Some type of external contact scheme is, in fact, necessary to provide power and signal transmission between the external system or package and the quilt. Fig. 1 shows a quilt with wire bond pads at the periphery, but conventional bump bonding is also allowed by this approach.

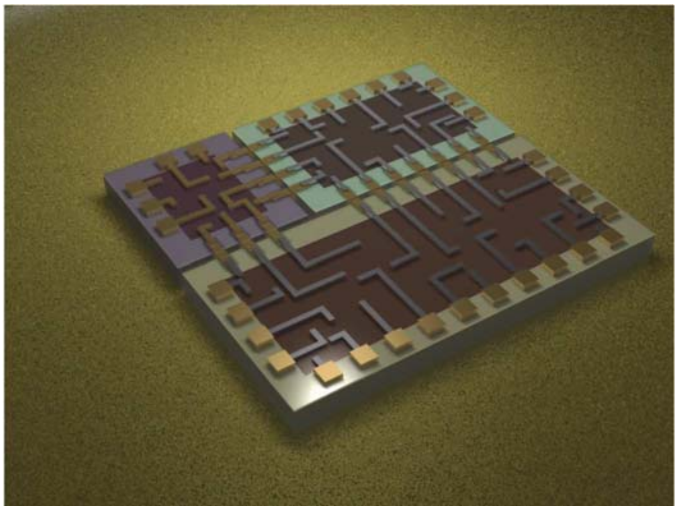

Fig. 1. Rendering of three ICs interconnected using QP. Quilt of die would be inserted into a conventional IC package. Squares around the periphery of the quilt represent conventional wire-bond pads, but alternatively, bumps could be used throughout the quilt.

Direct QP electrical contacts offer the potential for high frequency signal transfer, at more than 200 GHz, as discussed in Section IV. Additional advantages include the elimination of one IC package for every chip beyond the first included in the quilt (the entire multichip quilt being housed in a single, somewhat larger, conventional package), which leads to the aforementioned decrease in system size (and improved silicon efficiency) and weight. Less obvious is decreased power consumption and chip area (and higher yield) due to the elimination of input/output (I/O) buffers. In fact, as much as 50% of generated heat and silicon die area can be attributed to the I/O buffers for high performance application specific integrated circuits [12]. Naturally, smaller chip area results in more die per wafer and higher yields, and, therefore, lower costs. Moreover, advanced systems can be constructed by combining heterogeneous materials (such as Si, SiGe, GaAs, InP, etc.) into a quilt, allowing functionality that would heretofore be impossible, having implications for optical interconnects, optical communications, radio frequency (RF) communications, etc. Using QP, a mix-and-match approach to system-in-package (SiP) design is possible, making the exchange and upgrading of intellectual property (IP) more cost-effective than integrating the IP components on a single chip.

The list of potential benefits, as detailed above, is extensive. Considering speed, power consumption, heat dissipation, noise, size, decrease in printed wiring board complexity, weight and, potentially, cost, nearly every system characteristic is improved through QP. As to the applications of QP, not every electronic system requires improvements in every area. For example, a desktop computer may benefit from speed and cost improvements, but not necessarily from decreases in weight or size. Likewise, a space system might benefit most from decreases in weight and power, but not so much from cost. As another

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[2] http://www.siliconpipe.com

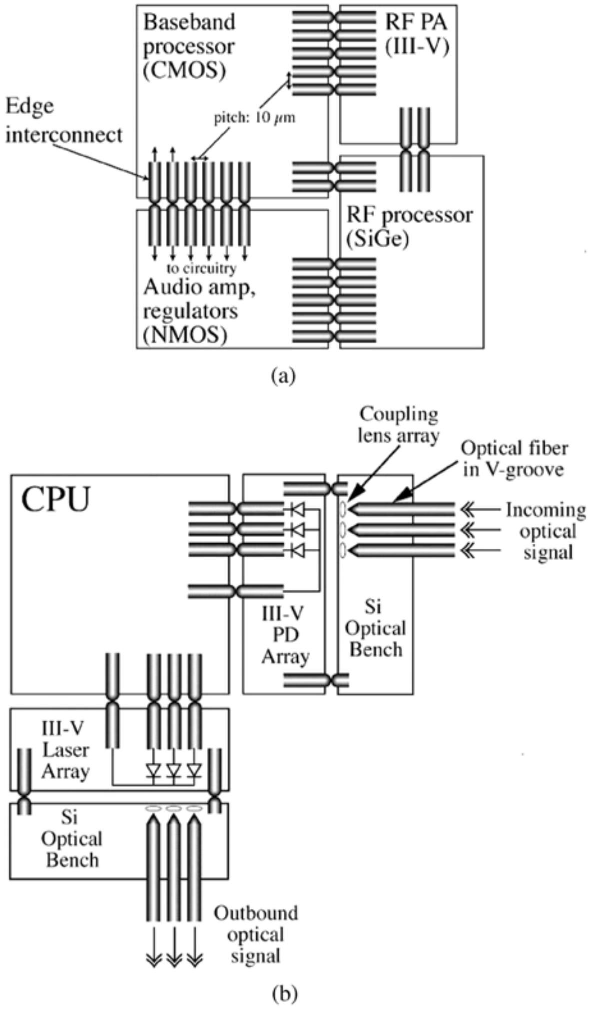
example, directly-coupled sensors and amplifiers might benefit primarily from decreased noise. Any potential drawbacks or advantages of implementing QP, therefore, depend on the particular application.

Without the burden of signal transmission through packages, a system can be expected to function at considerably higher speeds while dissipating less power. The optimum 2-D integrated electronic system would be configured like wafer scale integration (WSI), which in the 1980s was considered a major goal of systems development, but was discarded due to yield issues [13]. Barring this, putting as much functionality on a single chip as possible, as in system-on-chip (SoC) technology, would be the next best thing. In comparison, the remaining alternative, SiP, suffers from lower performance due to impedance discontinuities at the chip/substrate interfaces, but enjoys greater versatility since heterogeneous materials are allowed [14]. Three-dimensional integration is yet another alternative, but is complex and suffers from difficulties in thermal management [15].

In QP, the connection of ICs through low-loss nodule structures solves many of the problems of WSI, SoC, and SiP. QP allows the use of heterogeneous materials and device technologies in the system, something that is unthinkable for WSI or SoC. This feature makes possible the co-integration of optical, RF, analog, and digital functionality into tightly-integrated WSI-like systems for the highest possible system performance. QP allows separate manufacturing processes for each panel of the quilt, so it does not suffer from the tradeoffs in manufacturing complexity required of SoC for heterogeneous functionalities such as analog and digital or limitations to a single material system, e.g., for optical interconnects [16]. Therefore, QP can be used to create improved SoC-like performance with less difficulty overcoming various fabrication hurdles for single IC manufacturing, while avoiding many of the limitations of SiP.

As examples of the versatility of QP, Fig. 2 shows its use for interconnecting adjacent die for two potential applications. Fig. 2(a) shows a conceptual diagram of a mobile wireless terminal in which the baseband processor implemented with CMOS is attached directly to an RF signal processing block implemented with SiGe HBTs, which in turn is connected to a III-V based power amplifier, while all three ICs are connected to an NMOS-based audio amplifier and voltage regulator subsystem IC. Likewise, the optically-networked node illustrated in Fig. 2(b) could include a CMOS processor, arrays of III-V detectors and transmitters, and Si-based optical bench platforms for optical fiber alignment and fixturing. QP might serve as an assembly technology that facilitates accurate optical edge coupling, with QP nodules acting as precisely-placed spacers, as indicated in Fig. 2(b).

As these examples illustrate, ICs or devices fabricated with different processes can be integrated together in a single package, without requiring complex package wiring substrates or costly multicavity pin grid arrays [15]. The ability to directly interconnect III-V devices (e.g., GaAs-based low-noise or power amplifiers, InGaAs/InP photodetectors, GaN/AlGaN LEDs) with Si and SiGe VLSI circuits opens up myriad possibilities for new system concepts and applications.



(a)

(b)

Fig. 2. Illustration of possible QP architectures for (a) a wireless mobile terminal and (b) an optical network.

III. Chip Fabrication

We have fabricated chips using the process flow for QP structures presented in Fig. 3(a)–(g). After completion of the IC front-end processing [Fig. 3(a)], the nodules are created by first using deep reactive ion etching (DRIE) to form wells for the contacts [Fig. 3(b)], followed by isolation of the wells with plasma enhanced chemical vapor deposition (PECVD) oxide or nitride [Fig. 3(c)], and plating to fill the wells to form the nodules. Chemical-mechanical polishing (CMP) is used to planarize the nodules after plating [Fig. 3(d)]. Subsequent processing connects the nodules to the on-chip interconnects using conventional back-end-of-line processing [Fig. 3(e)]. Trenches for die separation are subsequently etched, also using DRIE, using a trench layout designed for easy die separation. This step incorporates a deep anisotropic etch that leaves the substrate shadowed under the nodules, followed by a short isotropic etch that clears material from under the nodules, leaving the nodules protruding from the edge facets of each IC on the wafer [Fig. 3(f)]. The amount of undercut in the DRIE trench-etch process controls the distance that the contacts protrude beyond the edge of the ICs.

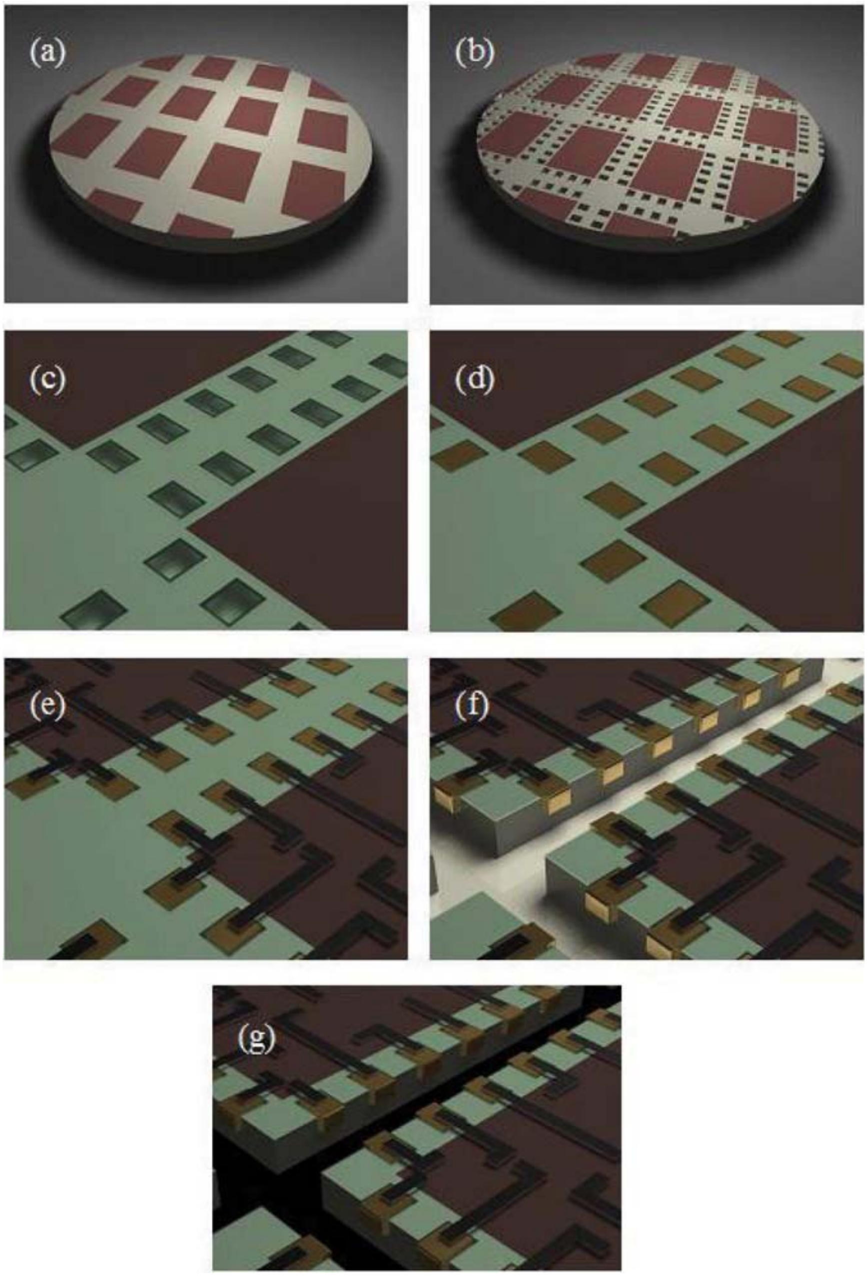


Fig. 3. Schematic process flow for formation of edge interconnects. Scales are exaggerated for illustration. (a) Wafer with ICs fabricated up to the start of the back-end-of-line processes, (b) definition and etching of nodule wells, (c) electrical isolation of nodules by PECVD oxide or nitride, (d) nodules after plating and planarization using CMP, (e) connection of nodules with on-chip multilevel interconnects, (f) die-separation trench by DRIE, (g) IC final die separation is completed by backside wafer thinning using CMP, or alternatively the wafer is etched through to the back.

Die separation [Fig. 3(g)] can be accomplished in at least two ways. The first method is based on the process known as "dicing-by-thinning," [17], [18] in which the wafer is thinned using backside grinding to separate the die along the previously DRIE-etched trenches. This is similar to a process called "dicing before grinding" (DBG) [19] developed by the Disco Corporation, Tokyo, Japan, in which a wafer is scribed with a dicing saw and then ground thin enough from the backside to separate the die. Instead, we have used DRIE to etch completely through the wafer (approximately 550–600 μm) while maintaining an appropriate undercut profile. Fig. 4 is a cross-sectional optical micrograph of two QP chips revealing the undercut that makes our die-coupling possible. The wafer thickness is 600 μm, and significant undercut is visible. This was achieved in our Alcatel 601E DRIE through a process of $\mathrm{SF_6}$ for etch and $\mathrm{C_4F_8}$ for passivation, alternating for 7 s and 2 s, at flow rates of 300 SCCM and 130 SCCM, respectively. The plasma was generated at 1800 W, and the substrate was maintained at 20 °C at a power of 80 W.

Following die separation, physical contact between adjacent die on a conventional package support substrate can be achieved by butting ICs directly against each other and fusing the nodules. Based on our experience fabricating nodules with widths as small as 10 μm with these DRIE, plating, and lithographic

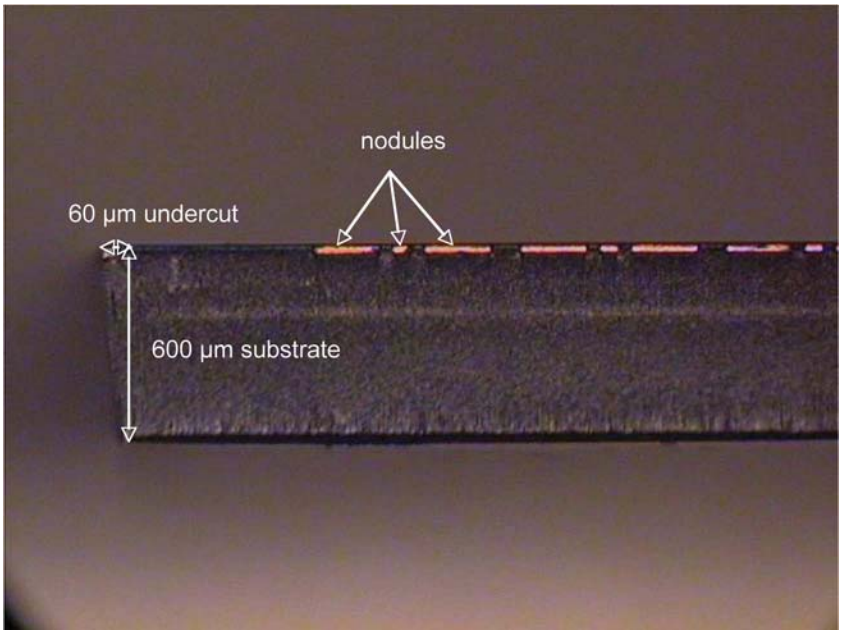
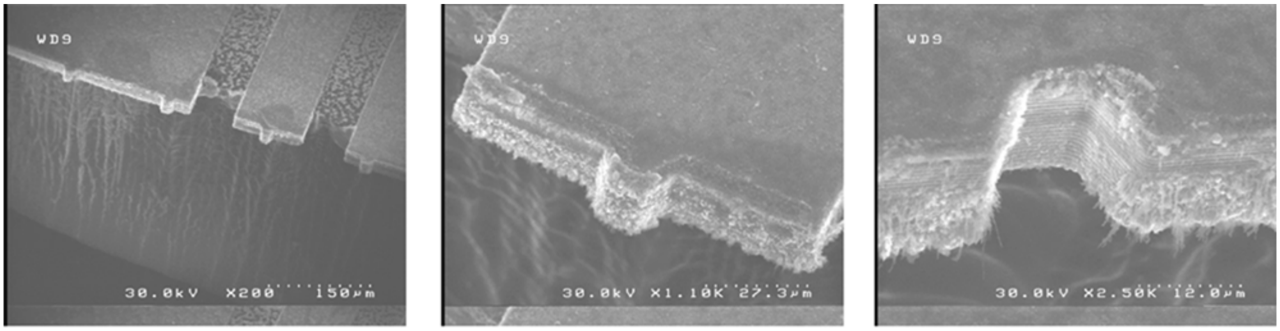


Fig. 4. Optical micrograph of edge of 600-μm-thick wafer showing undercut profile achieved by DRIE that is necessary to allow the metal nodules on separate die to touch without the substrate interfering.



(a) (b) (c)

Fig. 5. Scanning electron micrographs of copper nodules formed by electroplating extending beyond the edge of a completed QP die. Smaller nodule width is 100 μm, and the thickness is 18 μm. (a) Keyed nodules for a coplanar waveguide and background of substrate DRIE etched through to the back, (b) protruding key for self-alignment on first die, and (c) key receiver pattern on second die.

processes, we see no physical reason why contact pitches well below 5 μm cannot ultimately be achieved. At this size scale, a 1 cm^2 chip could support up to 4000 QP nodules. Vertical alignment of the nodules can be achieved by selecting the nodule thickness to be sufficient to allow for variations in wafer thicknesses after grinding (whose control is estimated at better than 1 μm [20]), or possibly by forming the connections face down with the nodules at approximately the same distance from the surfaces of the various die. The quilt can then be attached in either this configuration or face up. Solder can be applied after the formation of the quilt, as demonstrated in Section III, and the entire quilt attached in a conventional way to a package substrate.

The nodule material can be copper, gold, or other low-resistance material with an overlay of a solder material, although solid or layered metals such as copper or gold could be used with an ultrasonic weld or thermocompression bond step [21]. For the experimental demonstration in Section III, copper nodules with electrolessly-plated tin solder were used. Using the dicing-by-thinning die separation approach, the edges of the ICs are no longer required to be straight (a limitation due to the use of conventional dicing saws), so that a variety of interlocking and self-aligning silicon structures can be formed at the edges of the die. Alternatively, the metal nodules could also be keyed for self alignment. Both of these strategies are illustrated below.

In support of the QP concept, all of the steps in Fig. 3 have been demonstrated, and chips have been interconnected by soldering. Fig. 5 shows scanning electron micrographs of Cu nodules formed by electroplating and extending beyond the edge of a completed QP die, after the Ti seed layer and oxide well liner have been etched off. The smaller nodule width is 100 μm, and the thickness is 18 μm. Fig. 5 reveals several features discussed above. Fig. 5(a) shows the ends of a microwave coplanar waveguide test pattern on a substrate that has been etched through to the back. Fig. 5(b) and (c) show an example of keyed nodules, in which the metal allows for self alignment. Fig. 6 shows the two

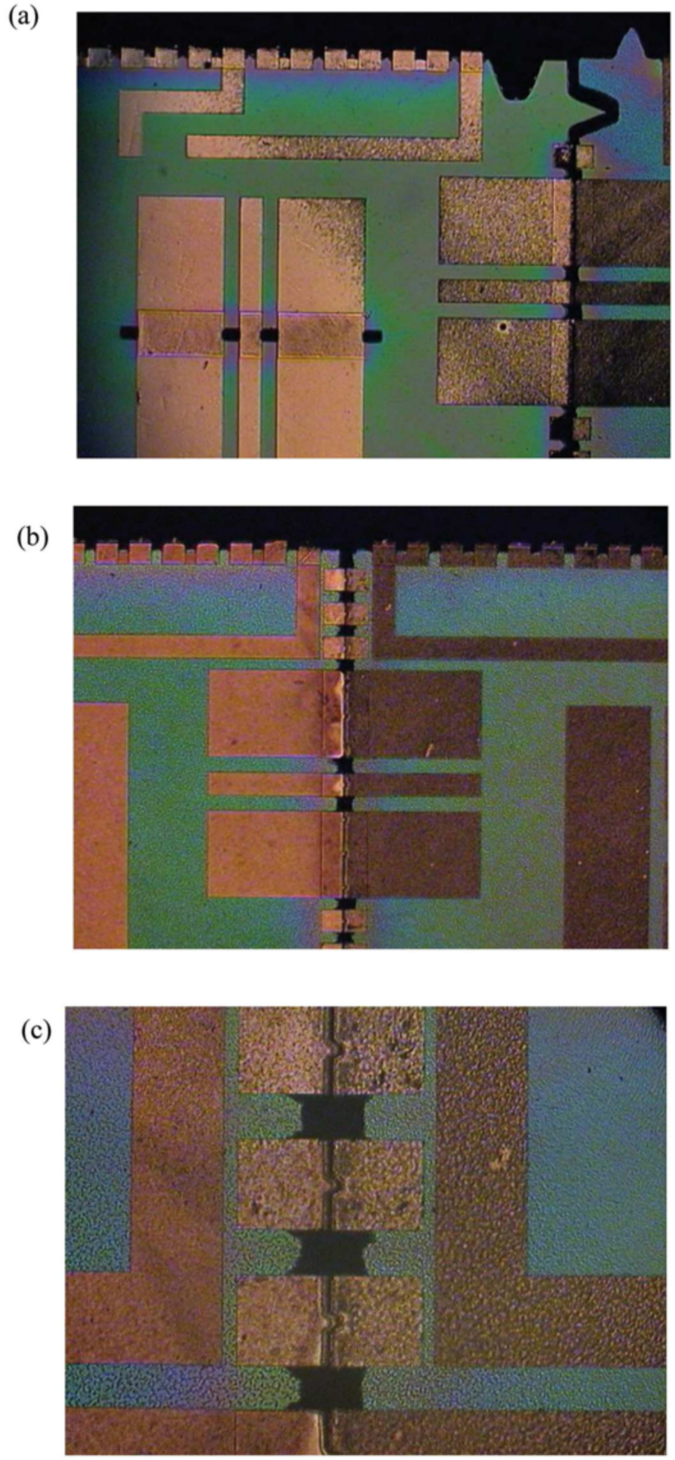


Fig. 6. Optical micrographs of QP chips aligned by self-aligning structures. (a) Alignment aided by notched patterns on the corners of the substrates. (b) Alignment aided by keyed metal nodules at low magnification and (c) at high magnification. Smallest nodule widths in this figure are 100 μm.

self-alignment methods. Fig. 6(a) is an optical micrograph of the edge of two die where two edges are pushed together manually, aided by alignment features notched in the silicon substrate, as shown at the top right of the picture. Fig. 6(b) is a low magnification image of two die aligned using the self-aligning keyed nodules of Fig. 5. Fig. 6(c) shows at higher magnification how the keys on the metal nodules find notches in the complementary die. Although the die in Fig. 6 are not fused, they suggest that alignment can be performed in a straightforward manner.

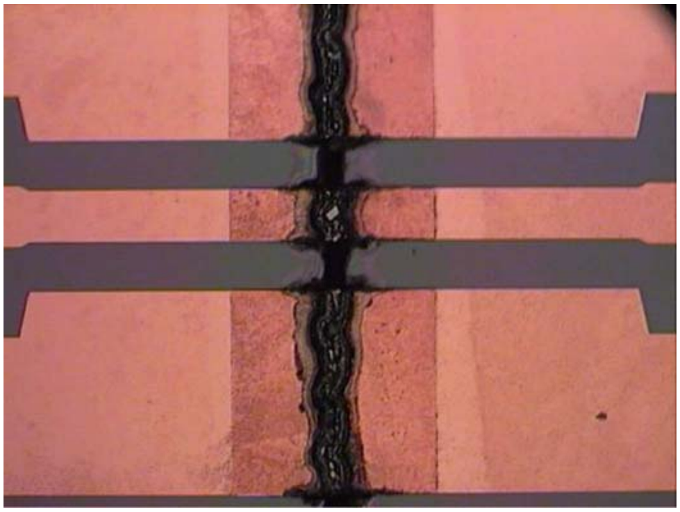


Fig. 7. Optical micrograph of a 50-μm coplanar waveguide fused using the bridge plating technique.

Die fusion is accomplished in two ways. With resist still in place from the DRIE etch step, the chips are immersed in an electroless Sn solution from Transene at 83 °C for up to 15 min, resulting in Sn layers as thick as 10 μm. Because of the resist masking, Sn is plated only on the exposed nodules. In one method, after resist removal, the plated die are manually held in place and heated on a hot plate to greater than 232 °C, the melting point of Sn, so that the Sn reflows and fuses the die. Alternately we spin a thin (2 μm) layer of glue (Loctite 460) onto a substrate, place the resist-coated die in contact and bake on a hot plate at 60 °C for 10 min. This is followed by the electroless plating step resulting in a solder bridge across nodules between chips. We estimate that the gaps between the chips are nowhere greater than 10 μm prior to plating. Subsequently, the resist and glue are removed by acetone. A cross-chip coplanar waveguide structure fabricated by this "bridge plating" method is shown in Fig. 7. The bridge plating technique was used for the quilted chips whose measurements are reported in the following section.

IV. MICROWAVE SIMULATIONS AND MEASUREMENTS

Since the quilt interconnect geometry results essentially in an extension of the planar chip interconnect structures across chip boundaries, the electromagnetic discontinuities that are inherent in wirebond-based interconnects (and to a lesser degree in flip-chip implementations) can be nearly eliminated. The QP nodules are resonance-free, high-speed interconnects that minimize overshoot and ringing. The only source of discontinuity in QP is the short (less than 100 μm) length of thick, inlaid nodule metal plus the short (less than 50 μm) air gap between the die. For 20-μm-thick nodules, we estimate that these features add about 0.1 nH and 50 fF to the interconnect between die.

Ansoft's HFSS electromagnetic simulator [22] was used to model both straight nodules and interconnects with a capacitance-reducing tapered geometry configured as coplanar

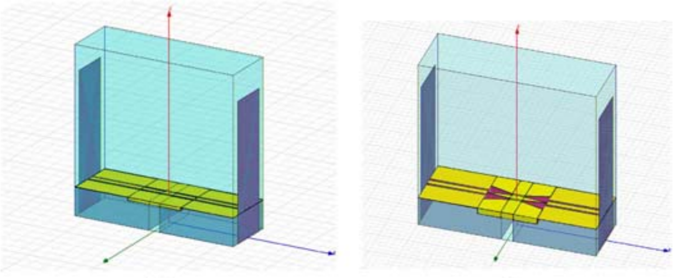

(a) (b)

Fig. 8. HFSS simulation models used to estimate return and insertion losses. (a) Straight coplanar waveguide pattern and (b) improved, tapered waveguide nodule pattern.

waveguides, as shown in Fig. 8. These simulated s parameters, extracted from 3-D frequency-domain simulations, show an expected chip-to-chip interconnect bandwidth of over 200 GHz. The nodules are connected to the interior of the chip by 1-μm-thick copper interconnects, and both the nodules and the interconnects are separated from the substrate by 1 μm of oxide. Fig. 9 shows s-parameters from dc to 200 GHz for both straight and improved interconnected nodules formed on 10-Ω-cm silicon for nodule center conductor width of 20 μm and depths of 10, 20, and 50 μm. Return loss, S_{11}, is shown in Fig. 9(a). In all cases, the improved geometry exhibits better impedance matching across the gap than does the geometry with straight nodules, and thicker nodules lead to poorer performance for each geometry. For 20-μm-thick nodules and the tapered geometry, return loss better than -12 dB up to 150 GHz is predicted. The performance for insertion loss S_{21} shown in Fig. 9(b) follows similar trends. Here, insertion loss for straight 20-μm-thick nodules better than 3.2 dB up to 200 GHz is predicted, and in the improved geometry that improves to 1.1 dB at 150 GHz and 2.1 dB at 200 GHz. It is important to note that a full optimization of the nodule geometry has not yet been performed, and we expect these numbers to further improve.

Coplanar waveguide QP structures of the variety shown in Fig. 8(a) have been fabricated and tested. The fabricated QP structures featured a 50-μm-wide signal nodule, a signal-ground spacing of 50 μm, and a 40-μm air gap between adjacent chips (corresponding to a 20-μm nodule extension from each chip). The copper nodules were 20 μm thick, and were embedded into the 10-Ω-cm substrate for a length of 80 μm. A 1-μm-thick deposited SiO_2 layer was used to isolate the copper nodules and interconnects from the substrate.

The simulated and measured return loss (S_{11}) and insertion loss (S_{21}) up to 40 GHz are shown in Fig. 10 where it can be seen that the measured return loss is better than 15 dB and the insertion loss is around 0.8 dB at 40 GHz. The deviation between the simulated and measured results may be due to variation in nodule depth from the 20-μm design target. As little as 0.8 dB of insertion loss is introduced by the QP structure at 40 GHz, which illustrates the excellent performance over wide bandwidths. The rapid increase in the insertion loss at low frequencies (<5 GHz) is due to the dielectric loss of the low resistivity silicon substrate. If built on high resistivity silicon or a III-V semi-insulating substrate, the performance is expected to be improved. Also, the dimensions of the QP nodules were not optimized for this demonstration. By decreasing the discontinuity between the on-chip interconnect and the nodule, even better performance is expected.

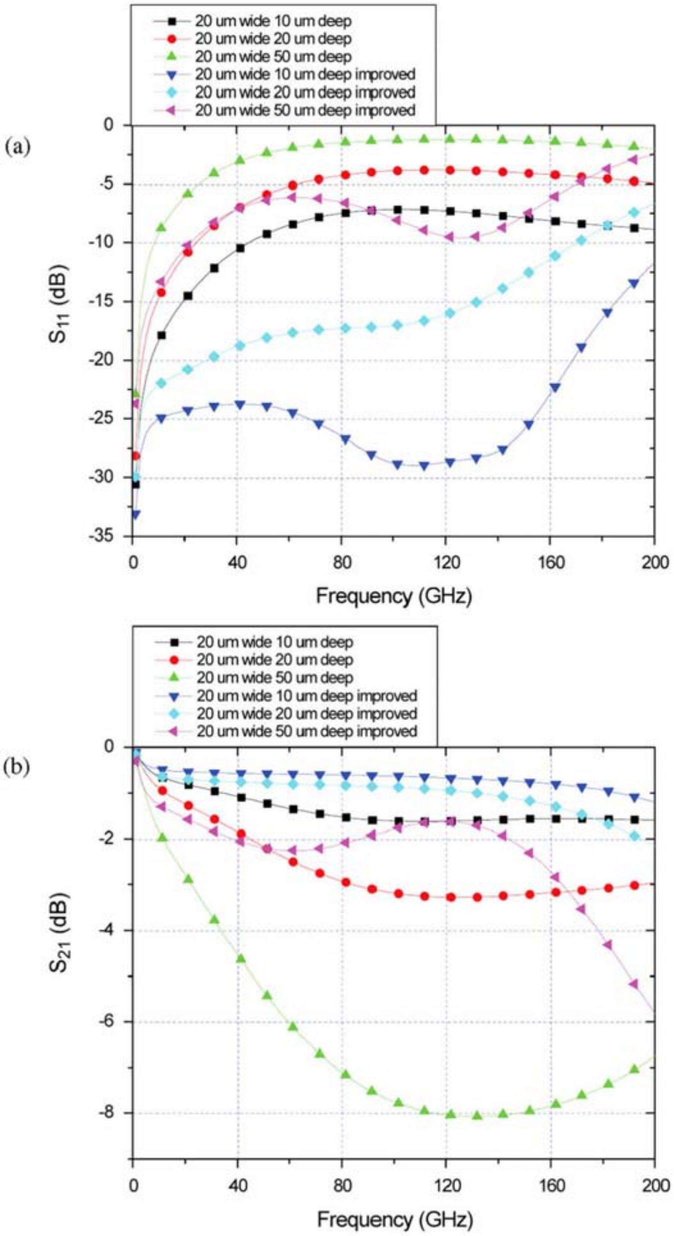


Fig. 9. Scattering parameters from dc to 200 GHz for the straight and improved coplanar waveguides of Fig. 7. (a) Return loss and (b) insertion loss for 20-μm-wide nodules of three different thicknesses.

V. Challenges to the Acceptance of QP

Although we are optimistic about the possibility for success of the QP technology, issues of manufacturability, reliability, and testability are yet to be investigated, and might present challenges that would limit its adoption.

Manufacturability: To our knowledge, there are no process steps required of QP that are incompatible with industry practices. The DRIE process is not currently a standard foundry process, but it is common in micromachining applications, which are, in themselves, becoming mainstream. Issues having

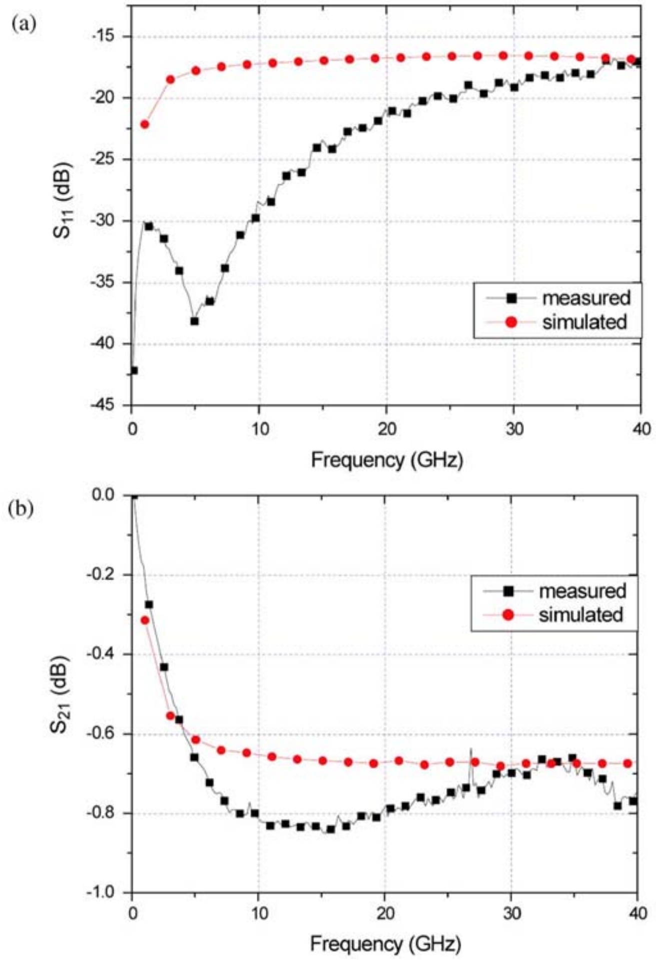


Fig. 10. (a) Return loss (s_{11}) and (b) insertion loss (s_{21}) of measured and simulated 50-μm-wide QP structure.

to do with manufacturing technology, particularly the accuracy of pick-and-place tools, would need to be resolved for mass production, and planarity of the package substrate would need to be sufficient to allow accurate alignment of the nodules.

Reliability: Integration of heterogeneous materials may introduce thermal expansion coefficient mismatch that will need to be managed, but for quilts consisting entirely of silicon die, this is not expected to be a significant issue. In any case, the reliability of the nodule connections will have to be thoroughly examined, including such other issues as ability to withstand shock, bending and drop.

Testability: Conventional ICs use the pad and bump structures for testing, so a new test technique must be developed. We anticipate that a test fixture for directly probing QP nodules can be developed that will allow testing to be performed, and thus permit assembly with known good die.

QP represents a paradigm shift in the manufacture of electronic systems. In spite of this, QP offers a real possibility for moving electronic systems to new levels of performance and efficiency.

VI. SUMMMARY AND CONCLUSION

A new paradigm for system integration was introduced, and joins the list of existing methods, including packages on printed wiring boards, multichip modules, SiP, SoC, wafer-scale integration, and 3-D integration. QP is unique in that it offers all of the advantages of 3-D integration (except for 3-D's extreme silicon efficiency) but with ease of fabrication and better thermal transfer properties. Most importantly, converting from conventional IC designs to QP would, in many cases, be straightforward, so system conversion to QP could be completed more quickly than to 3-D integration. In particular, the development of QP could pave the way for the evolution of new system architectures [23]–[26]. New systems incorporating diverse technologies such as high-speed or optical components with exceptional performance could be constructed with QP, where they would be impossible with 3-D integration. In conclusion, QP has the potential to positively impact electronic system cost and performance.

ACKNOWLEDGMENT

The authors thank R. Dunn, P. Kogge, J. Brockman, M. Niemier, J. Kulick, and W. Buckhanan for helpful discussions.

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