
EE566 Solid State Devices

Spring 2009

Dept of Electrical Engineering

University of Notre Dame

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Assignment 9

Posted: 04/14/2009

Due: 04/22/2009

Reading: Chapters 8 & 9 of the Textbook (MS).

Problem 1 (Charge and band-bending in MOSFET)

- Calculate *exactly* the total charge Q_s stored near the surface of the semiconductor in a MOS capacitor as a function of the surface band-bending ϕ_{bs} with respect to the body of the semiconductor layer.
- Plot $|Q_s|$ as a sheet density (units cm^{-2}). Compare with the plot in figure in pg 139 in handouts.
- Sketch the band-diagrams for each part of the plot.

Problem 2: (MOS – Capacitor, DRAM)

This problem is of utmost importance in understanding MOS capacitance-voltage behavior, as well as DRAM operation. Consider that a MOS system on p-type silicon (doping N_A) is biased to deep depletion by the sudden deposition of a total charge Q_G on the gate at time $t=0$. Carrier generation in the space-charge region at the silicon surface results in a charging current for the channel charge Q_n according to the net generation rate equation $J_G = qn_i x_d / 2\tau_0$, where x_d is the depletion region width, n_i the intrinsic carrier density, and τ_0 is the minority carrier (electron) lifetime (we have covered generation currents in class). This allows us to write

$$\frac{dQ_n}{dt} = -\frac{qn_i(x_d - x_{df})}{2\tau_0},$$

where x_d is the (time-dependent) depletion-region width at the surface, and x_{df} is the space-charge region width when thermal equilibrium is reached, i.e., when $x_d = x_{df}$ is reached, channel charging by generation goes to zero.

- Show that the time evolution of Q_n is governed by the differential equation

$$Q_n + \left(\frac{2\tau_0 N_A}{n_i} \right) \frac{dQ_n}{dt} = -[Q_G - qN_A x_{df}]$$

- Solve this equation subject to $Q_n(t=0) = 0$, and thus show that the characteristic charging time required to form an inversion layer is of the order $T \sim \tau_0 \times (2N_A / n_i)$. Estimate this charging time for an acceptor doping $N_A = 10^{15}/\text{cm}^3$. Can you explain why MOS capacitors are the building blocks of DRAMs from this example?

Problem 3 (MOSFET practice problem)

Solve problem 9.2, Page 486, Textbook. Also, sketch the band diagrams along S-D and gate-body axes. Note that part (c) of the problem should end as "...for the biasing in part (b).".

Problem 4 (Short channel effects in MOSFETs)

- Explain the rationale behind the "constant-field scaling" paradigm, and why both gate length and the gate oxide thickness are being reduced for current, and future devices.
- Explain briefly, using sketches and band diagrams, how short-channel-effect (SCE) changes the device performance as compared to a long-channel MOSFET. You should comment upon such effects as Drain-Induced Barrier Lowering (DIBL), subsurface punchthrough, mobility degradation, carrier velocity in the channel, and the effects on V_T , I_{Dsat} , and the speed f_T of the MOSFET.