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# EE566 Solid State Devices

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Dept of Electrical Engineering

University of Notre Dame

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## Assignment 7

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Due: 04/03/2009

**Reading:** Chapters 6, 7, & 8 of the Textbook (MS).

### **Problem 1: (Collector Transit Time in a Bipolar Transistor)**

Show that the collector transit time in a HBT (or BJT) is given by  $\tau_C = W_C / 2v_{sat}$ , where  $W_C$  is the collector thickness, and  $v_{sat}$  is the saturation drift velocity at which all carriers are assumed to be moving.

### **Problem 2: (Ballistic Collector Transistor)**

Solve the Midterm II problem (last 2 parts) on ballistic collector HBT with realistic numbers. Design the dopings etc required for ballistic collection at  $V_{CB}=0$  V, and at  $V_{CB}=-2$  Volt (investigate whether that is possible). You might find the paper by Ishibashi posted on the class website next to MidTerm II helpful in this regard.

### **Problem 3: (Practice Problem on MESFETs)**

Solve Problem # 8.9 (page 424) from the textbook (MS). In addition to the questions asked, draw band diagrams for each part of the problem.

### **Problem 4: (Survey of ITRS – the road trip...)**

The future of the semiconductor industry (chip, memory, electronic component manufacturers) is guided by a (or THE!) roadmap – the so called **I**nternational **T**echnology **R**oadmap for **S**emiconductors (*ITRS*). Your job in this problem is to assemble your own version of Moore's law – (futuristic) predictions of the path along which the semiconductor (& solid-state devices) industry is headed.

a) You are to collect data for your own use later – plot the recent past (starting late 90s), current, and projected values for MOSFET (or CMOS) scaling – a) gate lengths, b) gate oxide thicknesses, c) packing densities, d) supply voltages ( $V_{DD}$ ), e) threshold voltages, f) doping densities, g) speeds, h) static and i) dynamic power dissipation for each *node* (3 or 2-year cycle). Write a small paragraph on any additional information (such as major international players, problems/hindrances ahead with interconnects, lithography, solutions, new and emerging technologies etc) that you find interesting. Make generous use of resources available on the web – the ITRS website at <http://public.itrs.net> is a good start. Use other websites (such as Intel, IBM, TSMC etc) and of course Google to put together your graphs and paragraphs. This could be time-consuming, but I want you to get introduced to the real world of solid state devices based on silicon by this exercise.

b) Also discuss the new materials/technologies being proposed in the “beyond CMOS” scenario.  
*p.s.* This question seems straight out of a business school final exam!