EE566 Solid State Devices

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Dept of Electrical Engineering
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Assignment 9
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Due: 04/16/2008

Reading: Chapters 8 & 9 of the Textbook (Muller/Kamins/Chan: MKC) + Class Notes.

Problem 1: (MESFETs – Practice problem)
A MESFET is made with a $a = 100$ nm thick epitaxial GaAs layer on a semi-insulating GaAs substrate. The n-type doping in the channel is N_d=5x10^{17}/cm^3. Assume that the electron mobility is μ_n=8000 cm^2/Vs, and the electron saturation velocity is 10^7 cm/s. The gate length of the MESFET is L=0.5 μm, and the device width is W=10 μm. Assume perfect ohmic source-drain contacts, and that the device is "self-aligned" – meaning that the drain and the source are right next to the gate without any access regions. Also assume that the surface Fermi level at the Schottky junction is pinned at 1/3rd the bandgap above the valence band edge. Do the following:

A) Sketch a figure of the device geometry, and find the thickness of the conducting channel at equilibrium.

B) Find the threshold voltage V_T (gate voltage required to remove the channel) – is it an enhancement mode or a depletion mode FET? Also find V_{ds}(sat) as a function of the gate voltage V_g.

C) Sketch the band diagrams a) along the channel from source to drain, and b) perpendicular to the channel at the source- and drain-ends of the gate when i) $V_G<V_T$, $V_{DS}>V_{DS}$(sat), and ii) when $V_G>V_T$, $V_{DS}>V_{DS}$(sat). You should have *four* band diagrams (a-i, b-i, a-ii, b-ii).

D) Derive an expression for the current flowing in the MESFET in the linear regime. What is the order of magnitide of the current density (current per unit width, in A/mm)?

E) Derive an expression for the current flowing through the MESFET in the saturation regime. What is the order of magnitude of the current density?

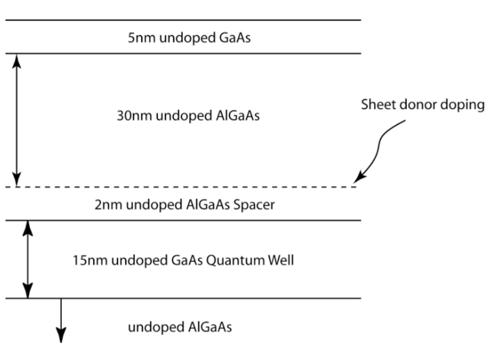
F) Sketch the I_{ds}-V_{ds} curves for different V_{gs}, and also a I_{ds}-V_{gs} curve at different V_{ds}.

G) Find and sketch the transconductance of the MESFET as a function of the gate bias.

H) Is it a long-channel or short channel device? How can you say?

Problem 2: (MESFETs – 2-dimensional problem)
Derive and plot the two-dimensional potential profile in the depletion region under the gate of a MESFET with zero gate voltage, and drain-source bias high enough that the current I_{ds} is saturated. Plot the electric field, potential, and band diagrams along the channel from source to drain, and perpendicular to the channel at the source- and drain-ends of the gate. Assume the MESFET channel to be long, such that gradual channel approximation holds near the source end. Explain everything you assume in the derivation. (Read the Grebene and Ghandhi paper!).

Problem 3: (HEMTs – Design your own structure)



Consider the AlGaAs/GaAs (ΔE_C=0.25eV) HEMT layer structure shown. Assume that surface states pin the GaAs surface Fermi level 1eV below the conduction band. I require the sheet –density of the channel to be n_s=10^{12}/cm^2.

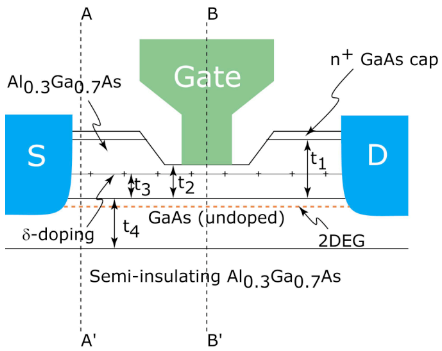
a) *Calculate* the sheet doping in the donor layer required to achieve that. Clearly draw the charge, field, and band diagrams. Verify with 1D Poisson. Note that the quantum well is triangular in shape.

b) Calculate the g_m vs V_{gs} curve for the HEMT, assuming v_{sat}(GaAs)=10^7cm/s, v_{sat}(AlGaAs)=2x10^6cm/s, gate length to be short, and V_{ds} is high, such that the saturated velocity model holds. Make any simplifying assumptions you think reasonable. Calculate the threshold voltage V_{th} required to deplete the channel.

c) Now, I want the quantum well to be flat instead of triangular. Design that for me.

d) Why would anyone need a flat quantum well? Are there any disadvantages? (Contd…)

Problem 4: (AlGaAs/GaAs HEMT charge control and transconductance)



Consider the AlGaAs/GaAs HEMT structure shown. The structure is grown by MBE, and the thickness and doping of the layers are - cap layer: N_D=7*10^{17}/cm^3, t_{cap}=5nm, $Al_{0.3}Ga_{0.7}As$ layer thickness t_1=25nm, after gate-recess etch, AlGaAs thickness t_2=17nm, delta-doped layer thickness=1nm & effective 3D-doping=3.5*10^{19}/cm^3, t_3=5nm, and GaAs quantum well thickness t_4=10nm. Assume the surface barrier is pinned at $q\Phi_s$=0.6eV below the conduction band edge for both GaAs and AlGaAs.

a) Calculate the 2DEG sheet density in the GaAs QW below the gate. Draw the charge-field-band diagram along line B-B' for finding the sheet density. Verify your calculated value with 1D Poisson simulation of the charge-field-band diagram. Is there any quantum-confinement*? How many quantum-confined states are formed in the GaAs QW? What are the eigenvalues?

b) Calculate the 2DEG sheet density in the GaAs QW below the source-and drain-access regions. Draw the charge-field-band diagram along line A-A' for finding the sheet density. Verify your calculated value with 1D Poisson simulation of the charge-field-band diagram. Comment on quantum confinement and eigenvalues.

c) What is the gate-capacitance C_g? Assuming the HEMT to be a short-channel FET, calculate the transconductance g_m using GaAs material parameters. Calculate the threshold voltage V_{th} for the HEMT.

d) Explain, using 2DEG-sheet density results of parts a) and b) and the transconductance of part c), what is gained by the gate-recess process. What would the transconductance be if the gate was not recessed?

In general, make sure you are comfortable with the chapter-end problems of MKC Chapters 8 & 9.

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* Run the "schrodingerstart", and "schrodingerstop" functions, and use the "*.status" file in 1-D Poisson.