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# EE566 Solid State Devices

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Dept of Electrical Engineering

University of Notre Dame

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## Assignment 10

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### Reading

Three chapters: MOS capacitors, MOSFETs, and advanced MOSFETs (last chp) of Muller/Kamins/Chan (MKC).

### Problem 1 (MOS Memory device based on the MOS capacitor)

MKC Problem 8.6.

Also, explain how this MOS capacitor can be used as a memory device.

### Problem 2 (Charge and band-bending in MOSFET)

- Calculate *exactly* the total charge  $Q_s$  stored near the surface of the semiconductor in a MOS capacitor as a function of the surface band-bending  $\phi_{bs}$  with respect to the body of the semiconductor layer.
- Plot it in the form shown in Figure 8.8 in MKC, but as a sheet density (units  $\text{cm}^{-2}$ ). Compare with the plot in figure in pg 139 in handouts.
- Draw the band-diagrams for each part of the plot.

### Problem 3 (Hysteresis in MOS capacitance-voltage measurements)

Problem 8.14, MKC. Include the band-diagrams in each part of your table. Your solution to this problem would help you in getting a feel for the major problem that most alternative device structures to the traditional MOSFET such as III-V MOSFETs, nanowire, nanotube MOSFETs, etc face today – the gate dielectric problem.

### Problem 4: (MOSFET Design) (easy practice problem!)

An n-channel MOSFET has a  $W/L=5$ , a  $\text{SiO}_2$  layer thickness  $t_{ox}=20\text{nm}$ , and electron mobility  $\mu_n=600\text{cm}^2/\text{Vs}$ . You are to use it as a *controlled resistor*. Remember that the MOSFET has a normally OFF channel, which is opened when the gate voltage ( $V_G$ ) is larger than a threshold voltage ( $V_T$ ).

- Sketch a figure of the MOSFET structure with labels of layers, doping, etc.
- Calculate the free-electron sheet density in the channel  $Q_n/q$  required for the MOSFET channel resistance to be  $R=500\Omega$  in the linear regime of MOSFET operation (i.e., low  $V_{DS}$ ).
- Using long-channel theory, find the excess gate voltage (i.e.,  $V_G-V_T$ ) required to produce the desired resistance under conditions of part b).

### Problem 5 (Electric field along the channel of a MOSFET)

Problem 9.18, MKC. Comment, after drawing the electric field profile from the source to drain region, why in current short gate-length MOSFETs, a lightly-doped-drain (LDD) halo implant is employed to enhance device performance. You can view the LDD MOSFET process flow at the following website - <http://www.ee.mnsu.edu/~khaliq/archive/ee5480/modules/lightly.html>

### Problem 6: (MOSFETs – Currents)

Consider a MOSFET biased in *strong inversion* in the *linear* region.

- Find expressions for the diffusion current  $I_{diff}(x)$  and drift current  $I_{drift}(x)$  at any point  $x$  along the channel.
- Which current component dominates?

### Problem 7 (CMOS improvements with scaling)

Problem 9.16, MKC. Explain the rationale behind the "constant-field scaling" paradigm.

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### Problem 8 (Subthreshold leakage currents)

Subthreshold leakage current flowing between the source and the drain is a major source of static power dissipation in MOSFET digital logic circuits.

a) Show that the subthreshold leakage current varies with the gate voltage as

$$I_{DS} \approx I_0 e^{\frac{\eta q V_{GS}}{kT}}, \quad \text{where}$$
$$\eta = \frac{1}{1 + 3t_{ox} / x_{depl}}$$

b) Plot the inverse subthreshold slope  $S = \ln 10 \cdot (kT / \eta q)$  for various ITRS technology nodes.

c) Explain why a low  $S$  is ideal for digital applications. What is the minimum  $S$  at room temperature? Explain why as gate lengths get scaled down further,  $S$  will increase unless proper care is taken in the design of the MOSFETs.

d) Recently, there have been some proposals of new device architectures to reduce  $S$  from the minimum values obtainable in traditional MOSFET design. Do some research and comment on these approaches. (Your best resource might be Dr. Seabaugh, but don't tell him I told you so!)

### Problem 9 (Short channel effects in MOSFETs)

Explain briefly, using sketches and band diagrams, how short-channel-effect (SCE) changes the device performance as compared to a long-channel MOSFET. You should comment upon such effects as Drain-Induced Barrier Lowering (DIBL), subsurface punchthrough, mobility degradation, carrier velocity in the channel, and the effects on  $V_T$ ,  $I_{Dsat}$ , and the speed  $f_T$  of the MOSFET.

NO more assignments!!!



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