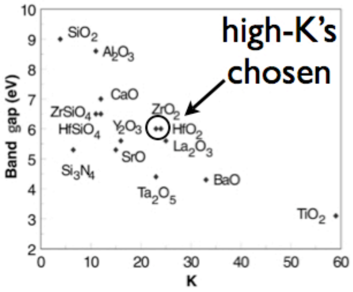
EE566 Solid State Devices

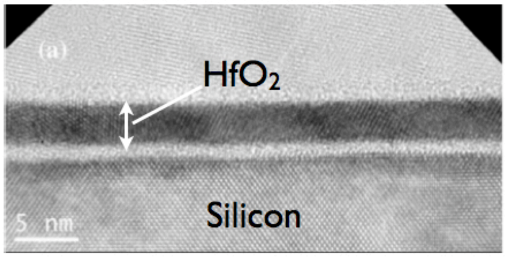
Spring 2008
Dept of Electrical Engineering
University of Notre Dame
Instructor: Debdeep Jena (djena@nd.edu, x8835)

Final Exam (2 Hours, 4 Problems, 25 Points)

05/08/2008

Problem 1: High-K Dielectrics (4 Points)





The MOSFETs in the latest CMOS microprocessors use high-K dielectrics such as HfO_2 on Silicon, and a metal gate. The figure above on the right shows a typical high-K MOSFET structure. The figure on the left shows the electronic bandgaps of various choices of oxides that were initially being considered for replacing the SiO_2 layer in MOSFETs. The oxide that was finally chosen is HfO_2 (bandgap ~ 6.0 eV, relative dielectric constant K ~ 22).

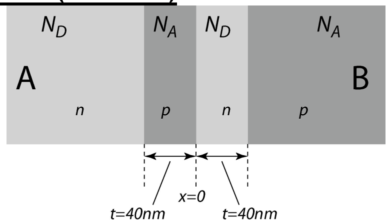
Answer the following questions:

a) Why did SiO_2 need replacement? Be qualitative, but answer comprehensively based on your knowledge of FETs; be to the point. (**1 Point**)

b) Based purely on the physics (plot of bandgaps vs dielectric constants), what is the reason behind the choice of HfO_2? Be partially quantitative in your answer. (**2 Points**)

c) If more dielectrics are discovered and added to the plot above, where must they be on the plot to be considered attractive for MOSFETs? Why? (**1 Point**)

Problem 2: A strange p-n junction (6 Points)



Consider the silicon p-n junction shown below with a rather messed-up junction region.

a) Sketch the charge, electric field and band diagram for this device at zero applied bias. What is the built-in voltage between the quasi-neutral regions in A and B? Use $n_i=10^{10}/cm^3$, and $N_D=N_A=10^{17}/cm^3$. Assume regions A and B to be very long. (**1 Point**)

b) Find a *general algebraic relation* between the depletion widths W in regions A and B in terms of the thickness t and the built-in voltage V_{bi}. Neglect Gummel correction. Assume $N_D=N_A=N_o$ for simplicity. Then, calculate W for t=40nm, $N_o=10^{17}/cm^3$. (**2 Points**)

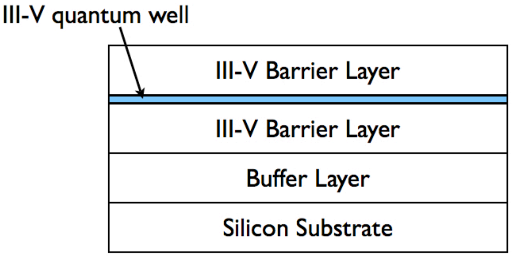
c) At what bias voltage will the electric field at x=0 fall to zero? Find algebraically first, then calculate the numerical value. Is it forward-bias or reverse-bias? (**2 Points**)

d) At this bias, sketch the band diagram, showing the quasi-Fermi levels. (**0.5 Point**)

e) Find the total current density (in A/cm^2) flowing through our funny junction at this bias. Use $\tau_n=\tau_p=10\mu s$. (**0.5 Point**)

(Continued on next page…)

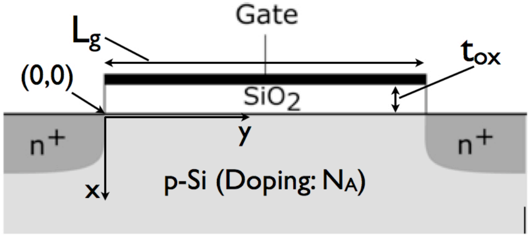
Problem 3: Compound Semiconductor MOSFETs - COSMOS (6 Points)



There is research being pursued currently on the possibility of incorporating thin layers of III-V semiconductors in the active regions of traditional Silicon devices. One of the major driving forces behind this is the high speed switching possible with III-Vs due to very high electron mobilities in them. The figure above schematically shows a hypothetical III-V semiconductor layer structure grown on a Silicon substrate. The goal is to make a high-speed FET on top of a Si substrate. Assume that you are the device designer. With the help of very skilled growers, the buffer layer makes the top three active layers of the device defect-free. Processing engineers are available to make any device structure you recommend. Answer the following:

a) What material properties (bandgaps, transport properties) are the most desirable for the choice of the three top layers for a FET faster than a Si-MOSFET? (**1 Point**)
b) Recommend the doping profile in the top three layers for a high-speed FET. (**1 Point**)
c) Sketch the device structure (gate, source, drain) that you would recommend to a processing engineer to fabricate a high-speed FET. (**2 Points**).
d) Sketch the charge-field-band diagram below the gate metal for the device, and label all quantities that determine the threshold voltage of the FET. Calculate the threshold voltage based on these parameters. (**2 Points**)

Problem 4: MOSFET design (9 Points)



Consider the MOSFET shown above. Assume that the n+ regions are degenerately doped ($N_D=N_c$), and that there are no charges in the oxide layer. Remember to draw relevant sketches. Give all answers *algebraically*. Use the following material properties for your answers.

Si: Intrinsic carrier concentration: n_i, Electron Affinity: $q\chi_{Si}$, Bandgap: E_{gSi}
SiO2: Electron Affinity: $q\chi_{ox}$, Bandgap: E_{gox}

a) Find the work-function of the gate metal for a zero flat-band voltage. (**0.5 point**)
b) Calculate the threshold voltage V_T for that gate metal. (**1 Point**)
c) We'll call the device a long-channel one if the gate length is at least 10X the maximum depletion depth under the gate. Given that the channel doping is N_A, find the critical gate length L_g above which the device is long-channel according to our definition. (**2 Points**)
d) Calculate the electric field component E(y) pointing along the channel at a distance y from the source end at a drain bias of V_{DS} [$<V_{DS}(sat)$] and a gate bias of V_{GS} [$>V_T$]. (**3 Points**)
e) Write down an expression for the total channel electric field $\mathbf{E}(x, y)=E(x)\mathbf{x}+E(y)\mathbf{y}$ under the gate at x=0. (**1.5 Point**)
f) Sketch the net electric field at three points: y = 0, $L_g/2$, & $0.9xL_g$. Explain where breakdown is expected to occur in the channel at high bias conditions. (**1 Point**)