EE566 Solid State Devices

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Dept of Electrical Engineering
University of Notre Dame
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Assignment 10

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Due: 05/04/2007

Reading
Chapter 9 of Muller/Kamins/Chan **(MKC).**

Problem 1: **(MOSFET Design)** (easy problem!)
An n-channel MOSFET has a $W/L=5$, a SiO_2 layer thickness t_{OX}=20nm, and electron mobility μ_n=600cm^2/Vs. You are to use it as a *controlled resistor*. Remember that the MOSFET has a normally OFF channel, which is opened when the gate voltage (V_G) is larger than a threshold voltage (V_T).

a) Sketch a figure of the MOSFET structure with labels of layers, doping, etc.
b) Calculate the free-electron sheet density in the channel Q_n/q required for the MOSFET channel resistance to be R=500Ω in the linear regime of MOSFET operation (i.e., low V_{DS}).
c) Using long-channel theory, find the excess gate voltage (i.e., V_G-V_T) required to produce the desired resistance under conditions of part b).

Problem 2 (Hysteresis in MOS capacitance-voltage measurements)
Problem **8.14**, MKC. Include the band-diagrams in each part of your table. Your solution to this problem will be helpful in the research of a graduate student of mine, who is observing large hysteresis in C-V plots in nanowire-based FETs.

Problem 3 (Electric field along the channel of a MOSFET)
Problem **9.18**, MKC. Comment, after drawing the electric field profile from the source to drain region, why in current short gate-length MOSFETs, a lightly-doped-drain (LDD) halo implant is employed to enhance device performance. You can view the LDD MOSFET process flow at the following website -
http://www.ee.mnsu.edu/~khaliq/archive/ee5480/modules/lightly.html

Problem 4 (CMOS improvements with scaling)
Problem **9.16**, MKC. Explain the rationale behind the "constant-field scaling" paradigm.

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Problem 5 (Subthreshold leakage currents)

Subthreshold leakage current flowing between the source and the drain is a major source of static power dissipation in MOSFET digital logic circuits.

a) Show that the subthreshold leakage current varies with the gate voltage as

$$I_{DS} \approx I_0 e^{\frac{\eta q V_{GS}}{kT}}, \quad \text{where}$$

$$\eta = \frac{1}{1+3t_{ox}/x_{depl}}$$

b) Plot the inverse subthreshold slope $S = \ln 10 \cdot \left(kT/\eta q\right)$ for various ITRS technology nodes.

c) Explain why a low S is ideal for digital applications. What is the minimum S at room temperature? Explain why as gate lengths get scaled down further, S will increase unless proper care is taken in the design of the MOSFETs.

d) Recently, there have been some proposals of new device architectures to reduce S from the minimum values obtainable in traditional MOSFET design. Do some research and comment on these approaches. (Your best resource might be Dr. Seabaugh, but don't tell him I told you so!)

Problem 6 (**Short channel effects in MOSFETs**)

Explain briefly, using sketches and band diagrams, how short-channel-effect (SCE) changes the device performance as compared to a long-channel MOSFET. You should comment upon such effects as Drain-Induced Barrier Lowering (DIBL), subsurface punchthrough, mobility degradation, carrier velocity in the channel, and the effects on V_T, I_{Dsat}, and the speed f_T of the MOSFET.

NO more assignments!!!