

PROBLEM 1

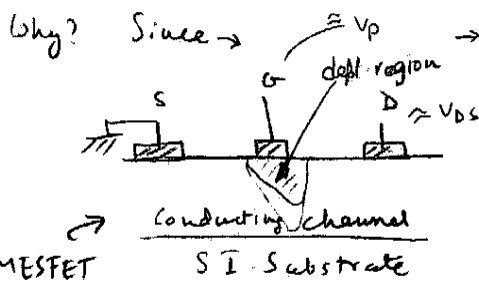
(a) Small bandgap \Rightarrow Advantage
 Small m^* , high μ
 \Rightarrow high speeds

Disadvantage
 - low on/off ratios
 - Temperature sensitive
 - V_{TH} very low, hard to distinguish between 'on' + off

Semi^c CNT $E_g \propto \frac{1}{\text{diameter}}$
 ∞ Graphene sheet \rightarrow No Gap!

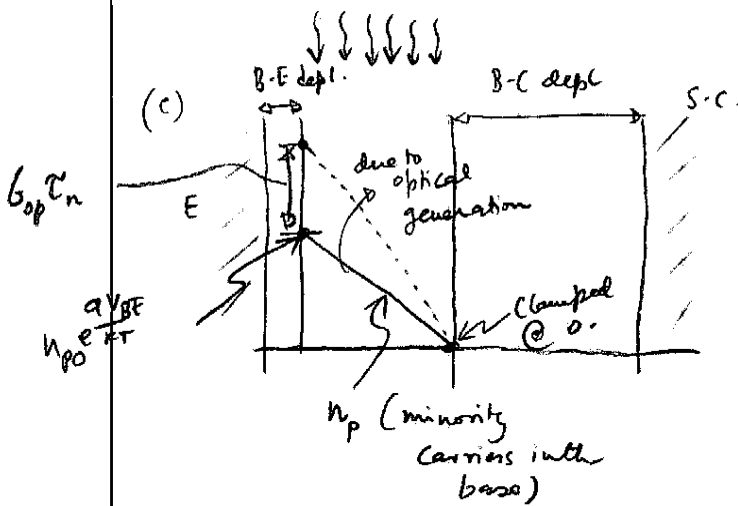
(b)

The Drain+end of the gate is the most susceptible to breakdown



Why? Since \rightarrow a voltage of $\sim (|V_g| + |V_{ds}|)$ drops across this region as opposed to $|V_g|$ across the source-end \Rightarrow field is higher in the drain-end.

- Ways
- lightly-doped drain side ('LDD')
 - wide-bandgap semiconductor



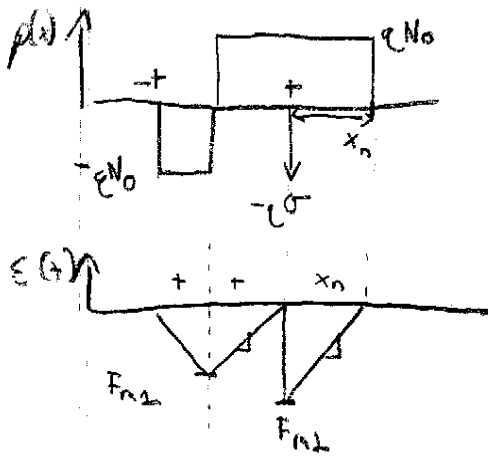
See figure on the left:

$\rightarrow I_C \uparrow$ since $n_p(x)$ has a larger slope.

$\rightarrow I_B \downarrow$ since holes that came from the base contact are now available due to optical generation.

$\Rightarrow \beta \uparrow$ since $\beta_0 = \frac{I_C^0}{I_B^0}$

$$\beta = \frac{I_C^0 + \Delta I_C \uparrow}{I_B^0 - \Delta I_B \downarrow} \uparrow$$



Charge Neutrality:

$$qN_0t + q\sigma = qN_0(t + x_n)$$

If $t = x_n = \frac{1}{3}W$ and $\sigma = \frac{1}{2}N_0 \cdot W$

$$qN_0 \cdot \frac{W}{3} + qN_0 \cdot \frac{W}{2} = qN_0 \left(\frac{W}{3} + \frac{W}{3} \right)$$

$$\frac{W}{3} + \frac{W}{2} \neq \frac{2W}{3}$$

- Solution Violates Charge Neutrality

$s = \sqrt{\frac{e_s kT}{e N_0}}$

Diode A: $W = \left[\frac{2\epsilon_s}{e} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (kT \ln \left(\frac{N_A N_D}{n_i^2} \right)) \right]^{1/2} = 2L_D \cdot \sqrt{\ln \left(\frac{N_A N_D}{n_i^2} \right)}$

Diode B:

Given: $E(x)$ goes to zero on junction side of σ

$$C_A = C_B \quad \frac{\epsilon_s}{W_A} = \frac{\epsilon_s}{W_B} \quad \therefore W_A = W_B$$

So:

$$2t + x_n = W_A = 2L_D \sqrt{\ln \left(\frac{N_A N_D}{n_i^2} \right)}$$

From charge neutrality:

$$\sigma = N_0 x_n$$

Built in Voltage:

$$F_{m2} = e \frac{N_0 t}{\epsilon_s} \quad F_{m2} = \frac{q N_0 x_n}{\epsilon_s} = \frac{q \sigma}{\epsilon_s}$$

$$V_{D,B} = \frac{1}{2} F_{m2} t + \frac{1}{2} F_{m1} t + \frac{1}{2} F_{m2} x_n$$

$$= \frac{1}{\epsilon_s} \left[q N_0 t^2 + \frac{1}{2} q N_0 x_n^2 \right]$$

If the two built in voltages are equal:

$$\frac{kT}{e} \ln \left(\frac{N_0^2}{n_i^2} \right) = \frac{q N_0 t^2}{\epsilon_s} + \frac{1}{2} \frac{N_0 x_n^2}{\epsilon_s}$$

$$\frac{\epsilon_s kT}{e N_0} \ln \left(\frac{N_0^2}{n_i^2} \right) = t^2 + \frac{1}{2} x_n^2$$

$$\frac{1}{4} W_A^2 = t^2 + \frac{1}{2} (W_A - 2t)^2$$

$$\frac{1}{4} W_A^2 = t^2 + \frac{1}{2} W_A^2 - 2t \cdot W_A + 2t^2$$

$$0 = 3t^2 - 2t \cdot W_A + \frac{1}{4} W_A^2$$

$$t = \frac{W}{2} \text{ or } t = \frac{W}{6}$$

fractional width, no width.

if $t = \frac{W}{2}$ $\sigma = 0$, Diode A case

If $t = \frac{W}{6}$:

$$W = 2t + x_n \quad \text{so} \quad x_n = \frac{2}{3}W$$

$$\sigma = N_0 x_n = \frac{2}{3}N_0 W$$

Checking Charge Neutrality:

$$qN_0 t + q\sigma = qN_0(t + x_n)$$

$$qN_0\left(\frac{W}{6}\right) + q\left(\frac{2}{3}N_0 W\right) = qN_0\left(\frac{W}{6} + \frac{2}{3}W\right)$$

$$\frac{W}{6} + \frac{2}{3}W = \frac{W}{6} + \frac{2}{3}W$$

Charge Neutrality Satisfied.

PROBLEM 3

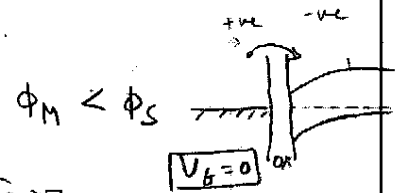
(a) To calculate V_{TH} , first get V_{FB} .

$$V_{FB} = q(\phi_M - \phi_S) = q[\phi_M - (q\psi_s + E_c - E_F)]$$

$$V_{FB} = -0.54 \text{ eV}$$

negative!

$$\frac{(E_c - E_v) + (E_B - E_F)}{2} \approx \frac{E_g}{2} \approx 0.55 \text{ eV} \quad q\psi_B = kT \ln\left(\frac{N_A}{n_i}\right) = 0.44 \text{ eV}$$



If V_{FB} was zero, the threshold voltage would be -

$$V_{TH}^0 = 2\psi_B + \frac{\sqrt{2qE_s N_A} (2\psi_B)}{C_{ox}}$$

$$= 2(0.44) + 0.98 = 1.86 \text{ Volt}$$

Since there is already band bending @ $V_G = 0$, the threshold voltage taking the flat-band voltage into account,

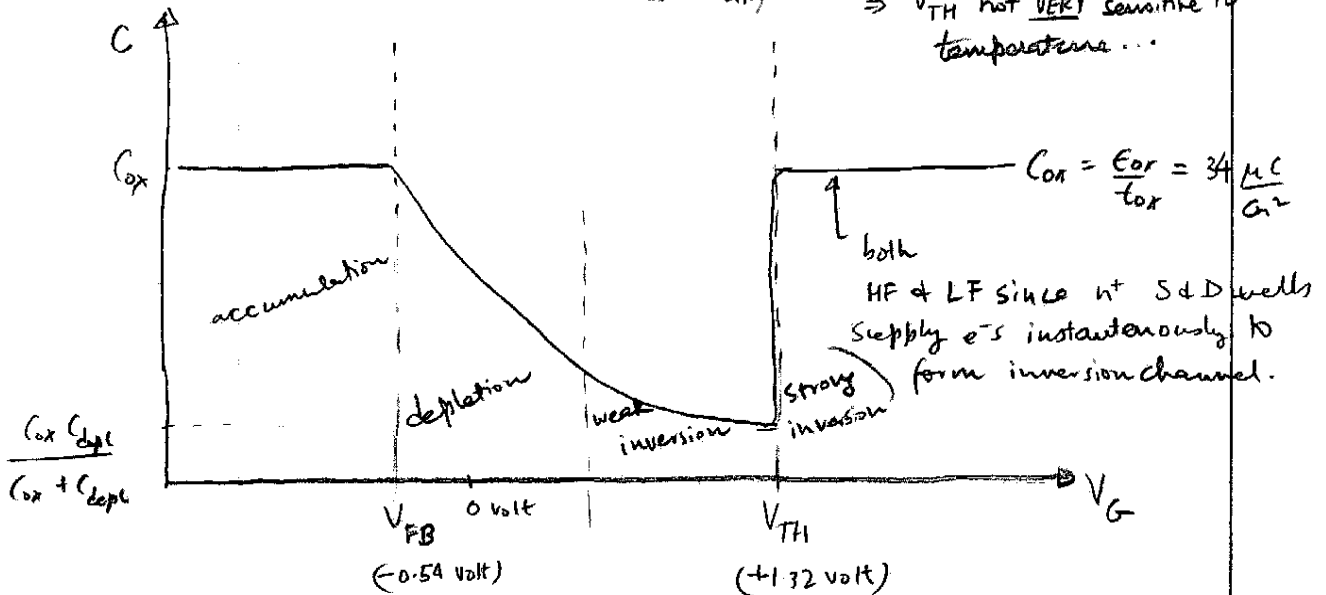
$$V_{TH} = V_{TH}^0 - |V_{FB}| = 1.86 - 0.54$$

$$V_{TH} = 1.32 \text{ Volt}$$

(b) Depends strongly on $\psi_B = RT \ln\left(\frac{N_A}{n_i}\right) \approx kT \left(\frac{-E_D}{kT} + \frac{E_D}{2kT}\right) \propto T^0$ to first order.

$\Rightarrow V_{TH}$ not VERY sensitive to temperature...

(c)



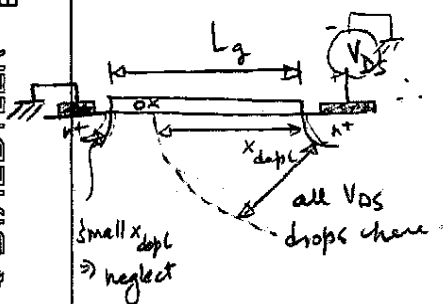
Prob 3, contd.---

(d) Most of V_{DS} drops in the reverse-biased Drain-channel n^+p junction, on the p -side.

\therefore If the gate length is larger than L_g^{\min} , where

$$\frac{q N_A (L_g^{\min})^2}{2 \epsilon_s} \approx V_{DS} = 100 \text{ Volt, } q \text{ should be safe.}$$

$$L_g^{\min} \approx \sqrt{\frac{2 \epsilon_s V_{DS}}{q N_A}} \approx 800 \text{ nm} \\ \approx 0.8 \mu\text{m}$$



$$\boxed{L_g > 1 \mu\text{m}} \text{ should do the job}$$

(e) No, this is a long-channel MOSFET, since

$$F_{\text{vertical}} \sim \frac{V_{GS}}{t_{ox}} \quad F_{\text{horizontal}} \sim \frac{V_{DS}}{L_g}$$

$$\text{long-channel} \Rightarrow F_{\text{horizontal}} \ll F_{\text{vertical}}$$

$$\frac{V_{DS}}{L_g} \ll \frac{V_{GS}}{t_{ox}}$$

$$\left(\frac{V_{DS}}{V_{GS}} \right) \ll \frac{L_g}{t_{ox}}$$

$$\text{Under normal operation, } \frac{V_{DS}}{V_{GS}} \approx 1 \quad \frac{L_g}{t_{ox}} = \frac{1800 \text{ nm}}{10 \text{ nm}} = 180$$

$$\frac{V_{DS}}{V_{GS}} \approx 1 \quad \therefore 1 \ll 180 \text{ is satisfied.}$$