
EE566 Solid State Devices

Spring 2007
Dept of Electrical Engineering
University of Notre Dame
Instructor: Debdeep Jena (djena@nd.edu, x8835)

Final Exam (2 Hours, 25 Points)

05/11/2007

Problem 1 (6 Points)

- a) Recently, carbon nanotubes & graphene sheets are being considered as possible materials for making MOSFET-like devices. One issue that frequently comes up is that these materials typically have very small bandgaps (much smaller than silicon). List *two disadvantages* and *two advantages* of using a narrow-bandgap material instead of silicon for MOSFET design. Assume that there are no “real-life” problems in device fabrication, and answer purely in terms of the device performance. **(2 Points)**
- b) Under high current flow conditions, which region in a MESFET is most susceptible to breakdown? Give *two ways* to increase the breakdown voltage of a MESFET. **(2 Points)**
- c) What will happen to the gain of a bipolar transistor if I shine light and generate electron-hole pairs only in the quasi-neutral base region? Assume that the relative change in minority-carrier density due to optical generation far exceeds the change in majority carrier density, and that the device is biased in the forward active mode. **(2 Points)**

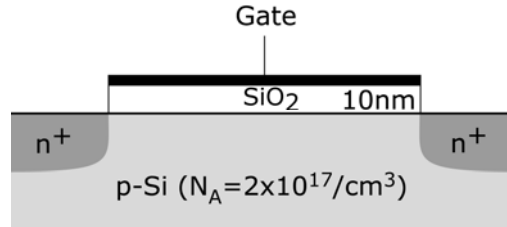
Problem 2: A strange p-n junction (7 Points)

Two p-n junction diodes A and B are fabricated on a semiconductor wafer. The semiconductor has an intrinsic carrier density n_i . The intentional doping in both n- and p-regions of the p-n junctions equal $N_A=N_D=N_0$. However, during ion implantation for isolation of the two diodes, negatively charged ions of sheet density σ incorporate a distance t from the metallurgical junction region in the *n-type side* of diode B. No such ions enter diode A. Neglect Gummel correction.

- a) Express the total depletion region thickness W in diode A in terms of n_i , N_0 , and the Debye length L_D in the intentionally doped regions of the semiconductors. (The Debye length in a doped region is given by $L_D = \sqrt{\epsilon_s kT / q^2 N}$, where N is the doping). **(1 Point)**
- b) Assume that the extra incorporated ions in diode B are inside the n-type depletion region of B. From two known facts, you will find the two unknowns - the sheet doping density σ , and the thickness t .
First known fact: The electric field drops to ZERO on the junction side of the plane of the sheet charge in diode B.
Second known fact: The zero-bias junction capacitances of diodes A and B are exactly the same.
Find σ in terms of N_0 and W , and t in terms of W . Draw the charge-field-band diagrams as you go along (you can't solve the problem without them!). **(6 Points)**

-----CONTINUED ON NEXT PAGE-----

Problem 3: MOSFET design (12 Points)



Consider the MOSFET shown above.

Assume a gate metal with a work function of 4.5eV, the n⁺ regions are degenerately doped ($N_D=N_C$), and that there are no charges in the oxide layer. Use the following material parameters for your calculations. Remember to draw relevant sketches.

Si: $n_i(300K) = 10^{10}/\text{cm}^3$.
 $q\chi_{\text{Si}}=4.05\text{eV}$
 $E_g=1.1\text{eV}$

SiO₂: $q\chi_{\text{ox}}=0.95\text{eV}$
 $E_g=8.0\text{eV}$

- Calculate the threshold voltage V_{th} at 300K. **(2 Points)**
- Comment* how it would change if the temperature is lowered to 77K (do not calculate!). **(1 Point)**
- Sketch the low- and high-frequency C-V curves if the voltage is applied between the metal gate, and to an ohmic contact to the p-substrate. Label everything of importance (capacitance values, V_{FB} , V_{th}), and explain. **(3 points)**
- When $V_{\text{gs}} = V_{\text{FB}}$, I want to prevent *drain-source punchthrough* for $V_{\text{ds}}=100$ Volt. Find the gate length so that I am safe. Make reasonable approximations, and assume that the gate oxide can sustain very large fields. **(5 points)**
- Does the device at such gate lengths suffer from short-channel effects? **(1 point)**