
EE566 Solid State Devices

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Dept of Electrical Engineering

University of Notre Dame

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Assignment 8

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Reading

Chapters 5, 6 & 7 of Textbook.

Problem 1: (Kirk effect at high Injection)

This problem is based on the HBT structure used in Assignment 7, Problem 3. Use constants for GaAs at 300K.

- Calculate the current density for the onset of Kirk effect, J_{kirk} . Assume a collector-base reverse bias of $V_{BC}=4\text{V}$ olt.
- Plot the base-widening (in nm) as a function of the current density for $J_C > J_{kirk}$.
- Comment on how Kirk effect harms the device performance, and how to deal with the problem.

Problem 2 (Collector Transit time in a Bipolar Transistor)

Show that the collector transit time in a HBT (or BJT) is given by $\tau_c = W_C / 2v_{sat}$, where W_C is the collector thickness, and v_{sat} is the saturation drift velocity at which all carriers are assumed to be moving. Cite any references you study for proving this. Why can you assume saturation velocity in the collector instead of $v = \mu E$?

Problem 3: (Current in a Mott-Diode)

In class, I derived the current density in a Schottky-diode of barrier height $q\Phi_B$ to be

$$J = J_0 [\exp(qV_a / kT) - 1].$$

I mentioned that the constant J_0 is given by $J_0 = A^* T^2 \exp(-q\Phi_B / kT)$, where

$$A^* = \frac{4\pi q m^* k_B^2}{h^3} \approx 120 \left(\frac{m^*}{m_0} \right) \frac{A}{\text{cm}^2 \text{K}}$$

is the effective Richardson's constant. You will now verify this result.

- Derive this result assuming that the current is ENTIRELY due to thermionic-emission. You might need to read up the textbook (chapter 5) for doing that.

Answer the following *qualitatively* with help of sketches -

- The derivation holds for *both* a Schottky and a Mott-diode – why?
- What would happen to the current-voltage characteristic of the Schottky diodes if I shine light with photon energy larger than semiconductor bandgap?

Problem 4: (Survey of ITRS – the road trip...)

The future of the semiconductor industry (chip, memory, electronic component manufacturers) is guided by a (or THE!) roadmap – the so called International Technology Roadmap for Semiconductors (*ITRS*). Your job in this problem is to assemble your own version of Moore's law – (futuristic) predictions of the path along which the semiconductor (& solid-state devices) industry is headed.

You are to collect data for your own use later – plot the recent past (starting late 90s), current, and projected values for MOSFET (or CMOS) scaling – a) gate lengths, b) gate oxide thicknesses, c) packing densities, d) supply voltages (V_{DD}), e) threshold voltages, f) doping densities, g) speeds, h) static and i) dynamic power dissipation for each *node* (3 or 2-year cycle). Write a small paragraph on any additional information (such as major international players, problems/hindrances ahead with interconnects, lithography, solutions, new and emerging technologies etc) that you find interesting. Make generous use of resources available on the web – the ITRS website at <http://public.itrs.net> is a good start. Use other websites (such as Intel, IBM, TSMC etc) and of course Google to put together your graphs and paragraphs. This could be time-consuming, but I want you to get introduced to the real world of solid state devices based on silicon by this exercise.

p.s. This question seems straight out of a business school final exam!