
EE566 Solid State Devices

Spring 2006

Dept of Electrical Engineering

University of Notre Dame

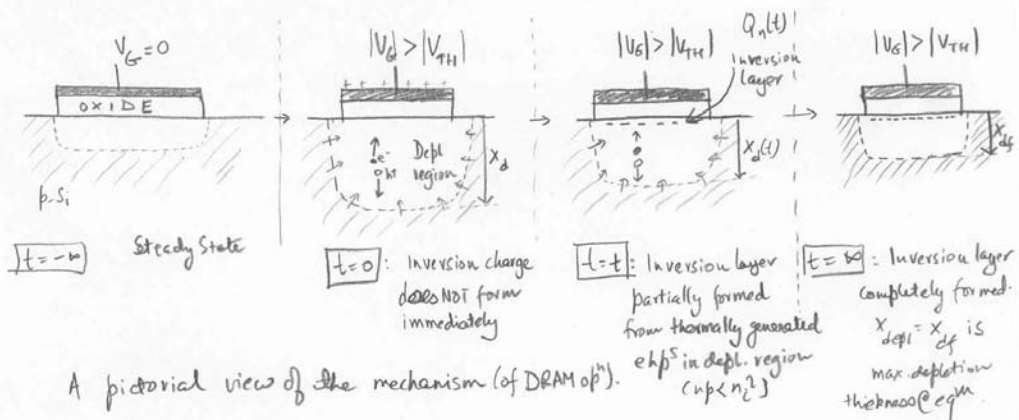
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Assignment 10 **SOLUTIONS**

Problem 1: Solutions

Page 139 of the handouts (class notes).

Problem 2: Solution



$$\frac{dQ_n}{dt} = -\frac{q n_i (x_d - x_{d\infty})}{2\epsilon_0} \rightarrow \text{use this, + simple charge conservation}$$

$$Q_n(t) + q N_A x_d(t) = |Q_G|$$

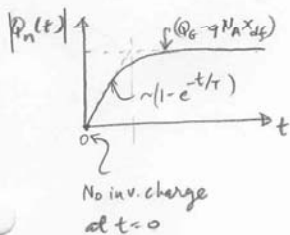
get in eliminate $x_d(t)$

$$(a) \quad Q_n + \underbrace{\left(\frac{2\epsilon_0 N_A}{n_i}\right)}_T \frac{dQ_n}{dt} = -[Q_G - q N_A x_{d\infty}]$$

$$(b) \quad \text{Solve: } \int_{Q_n(0)=0}^{Q_n(t)} \frac{dQ_n}{(Q_n + Q_G - q N_A x_{d\infty})} = - \int_{t=0}^t \frac{dt}{T}$$

$$\ln\left(\frac{Q_n(t) + Q_G - q N_A x_{d\infty}}{Q_G - q N_A x_{d\infty}}\right) = -t/T$$

$$\Rightarrow Q_n(t) = -(Q_G - q N_A x_{d\infty}) (1 - e^{-t/T})$$

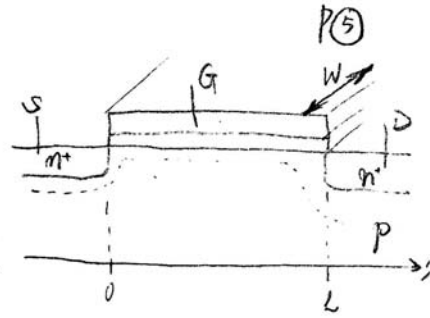


$$T = \frac{2\epsilon_0 N_A}{n_i} = (2 \times 10^{-6} \text{ s}) \times \left(\frac{10^{15} / \text{cm}^3}{10^{10} / \text{cm}^3}\right) \approx \boxed{0.2 \text{ seconds}}$$

Since the time req^d to form the layer is in the order of seconds, one can come back to the MOS capacitor after many clock cycles & find what had been stored there before \Rightarrow it is a memory...

Problem 3: Solution

Problem 3 Solutions: (by Sunny)



$$(a) \quad V_{TH} = V_{fb} + 2\psi_F + \frac{1}{C_{ox}} \sqrt{4\epsilon_s \epsilon_{Si} q N_A \psi_F}$$

$$\psi_F = \frac{kT}{q} \ln \frac{N_A}{n_i} = 0.026V \ln \frac{5 \times 10^{16} \text{ cm}^{-3}}{1.5 \times 10^{10} \text{ cm}^{-3}} \approx 0.4V$$

$$C_{ox} = \frac{\epsilon_{SiO_2}}{t_{ox}} = \frac{4 \times 8.85 \times 10^{-14} \text{ F/cm}}{500 \times 10^{-8} \text{ cm}} = 7.1 \times 10^{-8} \text{ F/cm}^2$$

$$\Rightarrow V_{TH} = -0.5V + 2 \times 0.4V + \frac{\sqrt{4 \times 12 \times 8.85 \times 10^{-14} \text{ F/cm} \times 1.6 \times 10^{-19} \text{ Coul} \times 5 \times 10^{16} \text{ cm}^{-3} \times 0.4V}}{7.1 \times 10^{-8} \text{ F/cm}^2}$$

$$\Rightarrow V_{TH} \approx 1.94V$$

Note that $\epsilon_{SiO_2} \approx 4$ & $\epsilon_{Si} = 12$ are used

(b) When $V_G = V_{TH} + 1.5V$, $V_{DS} = 1.0V$, NMOS is at linear region:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH} - \frac{1}{2} V_{DS}) V_{DS} \right]$$

$$= 600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \cdot 7.1 \times 10^{-8} \text{ F/cm}^2 \cdot \frac{50 \mu\text{m}}{1.5 \mu\text{m}} \left[(1.5V - \frac{1.0V}{2}) \cdot 1.0V \right]$$

$$= 1.42 \text{ mA} \quad (\text{Some } \mu\text{ you get } 1.38 \text{ mA when more accurate } \epsilon_{Si} \text{ \& } \epsilon_{SiO_2} \text{ are used})$$

(c) Since the device is in linear regime, the electrons are not moving at V_{sat} :

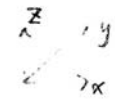
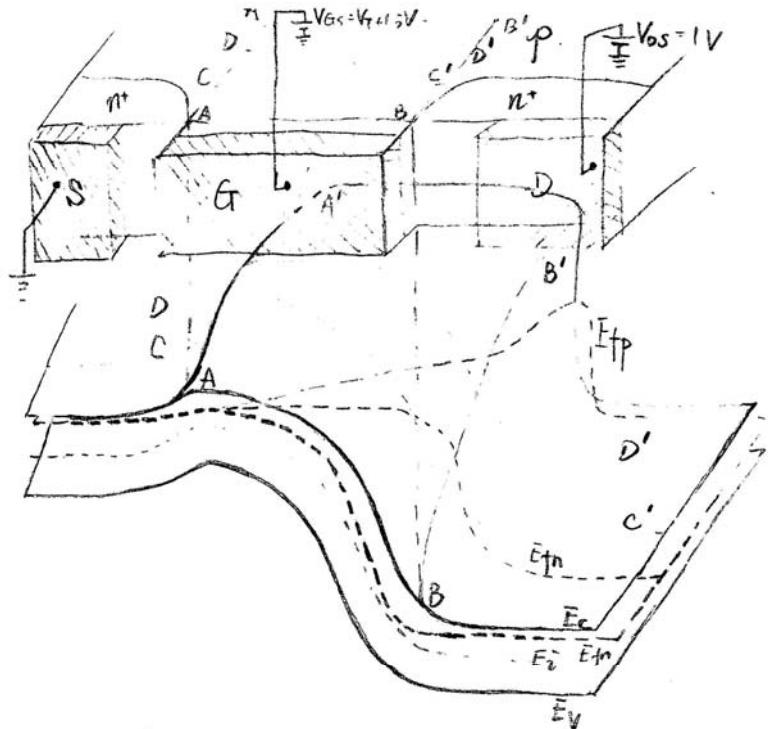
$$I_{DS} \Big|_{\text{source}} = I_{DS} \Big|_{\text{drain}}$$

$$V_{\text{source}} \cdot n_{\text{source}} = V_{\text{drain}} \cdot n_{\text{drain}}$$

$$\Rightarrow \frac{V_{\text{source}}}{V_{\text{drain}}} = \frac{Q_{i, \text{drain}}}{Q_{i, \text{source}}} \approx \frac{C_{ox}(V_{GD} - V_{TH})}{C_{ox}(V_{GS} - V_{TH})} = \frac{V_{GD} - V_{TH}}{V_{GS} - V_{TH}} = \frac{V_{T+1.5V} - 1.0V - V_T}{V_{T+1.5V} - V_T} = \frac{0.5V}{1.5V} = \frac{1}{3}$$

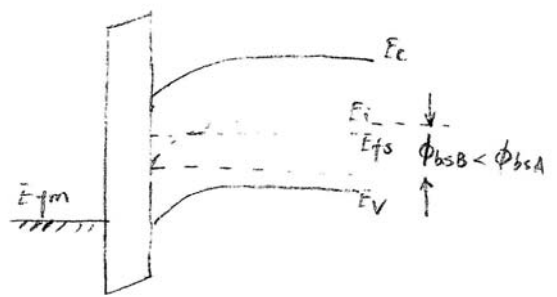
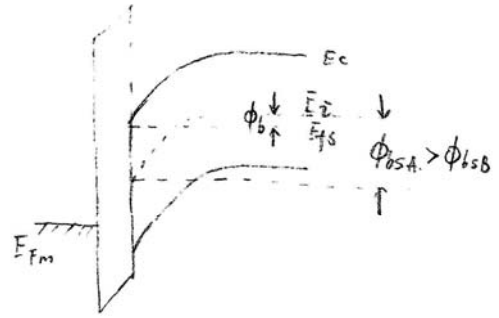
Here we use $C_{ox} \Delta V$ to approximate the inversion carriers. Because most of the inversion carriers are produced after strong inversion. And at that time the differential capacitance is almost C_{ox} .

The banddiagram is shown on next page.



Cross section AA'

Cross section BB'



Pass strong inversion, also, inverted more than BB' (drain)

Pass strong inversion, but band bending less than AA' (source)

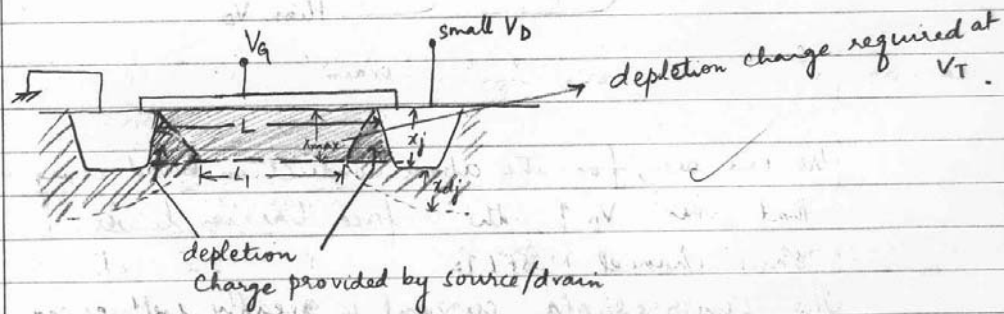
Cross section AA' & BB' (in y direction), and CC' & DD' (in x direction) are shown in the figure above.

Problem 4: Solution

Problem 4 - ASSIGNMENT 1 D - SOLN BY ANJALI.

Short Channel Effects are:-

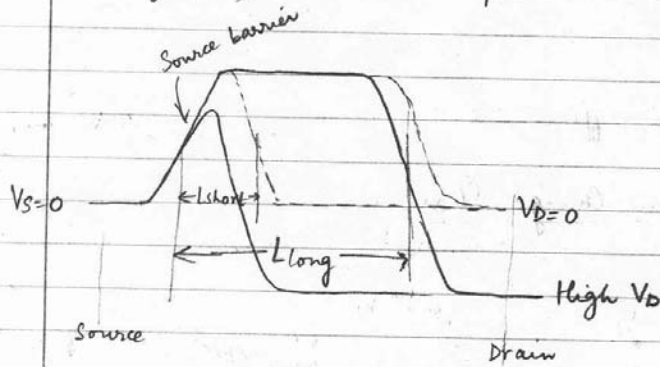
(i) Source-Drain Charge Sharing:-



The fixed substrate depletion charge $Q_d = -q N_a x_{dmax} W L$. We see 2 pieces of the rectangular charge region that are also parts of the source and drain p-n junctions. Therefore, no gate voltage is required to deplete the mobile charge from these regions.

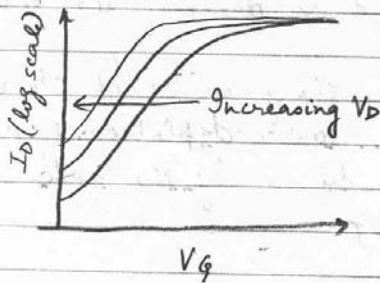
Because, some of the bulk charge in short channel MOSFETs is supplied by the drain-source depletion regions, the amount that must be induced by the gate decreases, consequently reducing V_T .

(ii) Drain Induced Barrier Lowering (DIBL) This effect refers to the influence of V_D on ϕ_s (the barrier to e^- flow at the np junction near the oxide surface at the source). The density of e^- entering the channel increases exponentially when the barrier is lowered linearly. In LONG channel MOSFETs only V_{GS} lowers ϕ_s . However, with short channel lengths even a high-enough Drain voltage (V_D) can lower ϕ_s .



We can see, from the above conduction band diagram, that when $V_D \uparrow$, the surface barrier lowers for short channel MOSFETs.

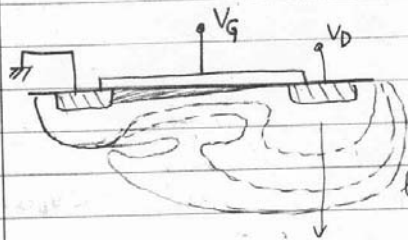
The subthreshold current is greatly influenced by DIBL, and ^{while} in long-channel Mosfets, the subthreshold current is independent of V_D , In S-C MOSFETS, it varies with V_D .



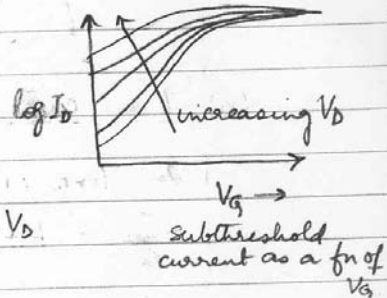
Thus, at a given V_G , if $V_D \uparrow$, $I_D \uparrow$.

(iii) Sub-Surface Punchthrough

This effect refers to the influence of V_D on the source n-p junction e^- barrier, in the substrate, away from the surface. The surface p region in NMOS is more heavily doped than the bulk, making it possible at high V_D for the drain-substrate depletion region to short with the source-substrate depletion region.



higher and higher V_D



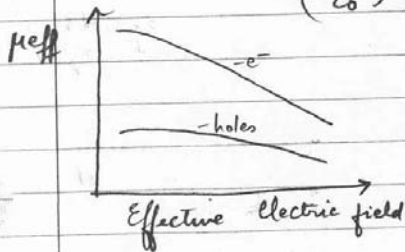
Subthreshold current as a fn of V_G

This leads to unacceptably high leakage currents in normally OFF devices

(iv) Mobility Degradation

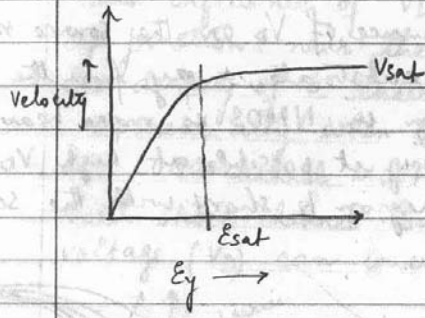
Mobility degradation can be expressed by the following equation

$$\mu_{eff} = \frac{\mu_0}{1 + \left(\frac{E_{eff}}{E_0}\right)^2}, \text{ as } E_{eff} \uparrow, \mu_{eff} \downarrow$$



This is a concern for both long and short channel MOSFETs. But more so, for short channel MOSFETs because the power supply voltage is not scaled as much as suggested by constant field scaling. Hence, $E_{eff} \uparrow, \mu_{eff} \downarrow$

(v) Velocity Saturation



At lower field, velocity $\propto E$.
But, in short-channel MOSFETs, fields reach very high values, and carrier velocities approach a limiting value.

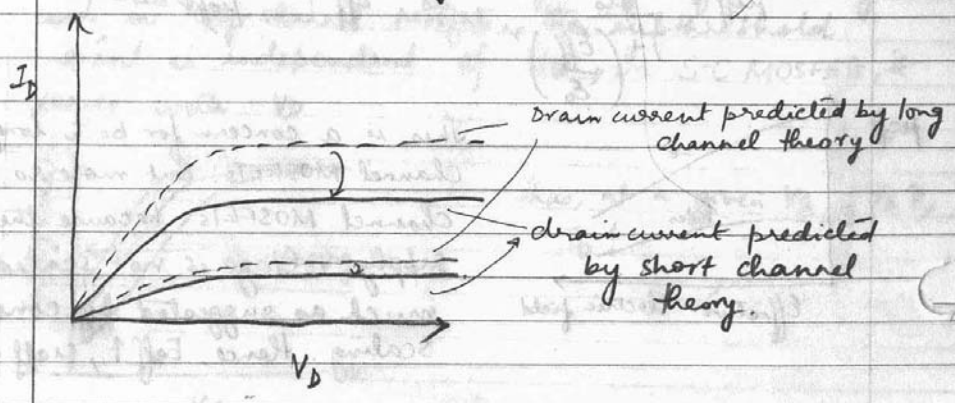
(vi) Drain current

In long channel MOSFETs, we have,

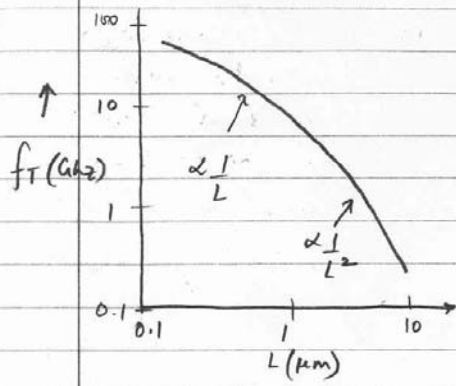
$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right] \text{ till } V_D < V_{sat}$$

$$I_{Dsat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_G - V_T)^2$$

But in short channel MOSFETs, the relation is not so simple. Reducing the channel length from $2\mu\text{m}$ to $0.02\mu\text{m}$, will not increase the drain current by 100 times. All the short-channel effects come into play, making the gain smaller.



(vii) Speed



Thus, we see that the speed of MOSFETs changes from $\frac{1}{L}$ dependence to $\frac{1}{L^2}$ dependence in the short-channel regime.