EE566 Solid State Devices

Spring 2006
Dept of Electrical Engineering
University of Notre Dame
Instructor: Debdeep Jena (djena@nd.edu, x8835)

Final Exam
05/11/2006

Time allotted: 2 hours

Problem 1 (5 Points)

a) You are required to form an ohmic contact to semiconductor A, which is doped p-type. You find that no matter what metal you try, it forms a Schottky contact with A. Then, you come across a paper that reports that semiconductor B, which is lattice matched to A, has a broken band offset with A, and forms an n-type ohmic contact easily. Explain with a band diagram why it would be worthwhile to try out degenerately n-type doped B as a possible candidate for making an ohmic contact to p-doped semiconductor A. (**3 Points**)

b) Recently, it has been observed that semiconductors that have high electron affinities such as ZnO and InN have a thin layer of very high density electron gas at the surface when in contact with other low electron affinity materials. Explain with a band diagram why it is expected. (**2 Pts**)

VERY IMPORTANT NOTE: For the following problems, give complete algebraic solutions first, and then substitute the numerical values.

Problem 2: HEMT Physics (7 Points)

Gate metal

InGaAs, t_1=5nm, N_D=$1x10^{17}/cm^3$, ΔE_C= - 0.1eV

AlGaAs, t_2=50nm, N_D=$5x10^{17}/cm^3$, ΔE_C= + 0.23eV

AlGaAs, t_3=10nm, Undoped, ΔE_C= + 0.23eV

GaAs undoped

Find the threshold voltage for the HEMT layer structure shown above. Assume that Φ_B=0.5V at the Schottky gate, and that E_C-E_F=0eV in the undoped GaAs layer at threshold. All band-offsets given are with respect to the conduction band edge of GaAs. Assume that the dielectric constants of InGaAs and AlGaAs are the same as that of GaAs (ε_{GaAs}=13.1ε_0). Draw the charge – field - conduction band diagram at threshold. Is it an enhancement mode or depletion mode device? (contd…)

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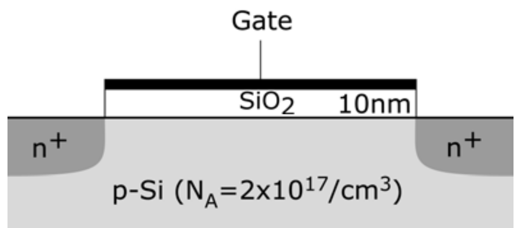
Problem 3: MOSFET Design (13 Points)



Consider the MOSFET shown above.

a) Calculate the threshold voltage V_T at 300K. Assume that the gate metal has a work function of 4.5eV. Use the following material parameters for your calculations -
Si: $n_i(300K) = 10^{10}/cm^3$, $q\chi_{Si}$=4.05eV, E_g=1.12eV, $\varepsilon_{Si}=11.7\varepsilon_0$, $N_C=10^{19}/cm^3$, $N_V=3x10^{19}/cm^3$.
SiO_2: $q\chi_{ox}$=0.95eV, E_g=8.0eV, $\varepsilon_{ox}=3.9\varepsilon_0$. (**3 Points**)

b) Assuming that the source and drain wells are degenerately doped ($N_D=N_C$), find the junction depths of the source- (& drain-) body p-n junctions when the source, drain, and the body are all grounded. Assume one-sided n^+-p junctions, and that the entire potential drop denoted by ϕ occurs in the p-Si body. Call this depth x_{j0}. (**2 Points**)

Now consider a situation when for the above MOSFET, $V_G=V_{FB}$. Explain why the MOSFET *should not conduct* under this condition irrespective of the drain bias (the source & body are grounded). However, if the gate length is not designed properly, electrons can flow from the source to the drain by the punchthrough mechanism as the drain bias increases (similar to the case in a bipolar transistor).

c) Explain with the aid of sketches what I mean by the above paragraph. Sketch the depletion region in the entire MOSFET when $V_G=V_{FB}$, accompanied by band diagrams to explain the phenomena. When is the punchthrough phenomenon severe – for long or short gate lengths? (**4 Points**)

d) Say your customer requires you to design the MOSFET such that when $V_G=V_{FB}$, the drain should withstand a bias of $V_{DS}=25*\phi$ (see part b) before punchthrough occurs. Design a gate length L for the customer. Express L in terms of x_{j0}, V_{DS}, and ϕ. (**4 Points**)