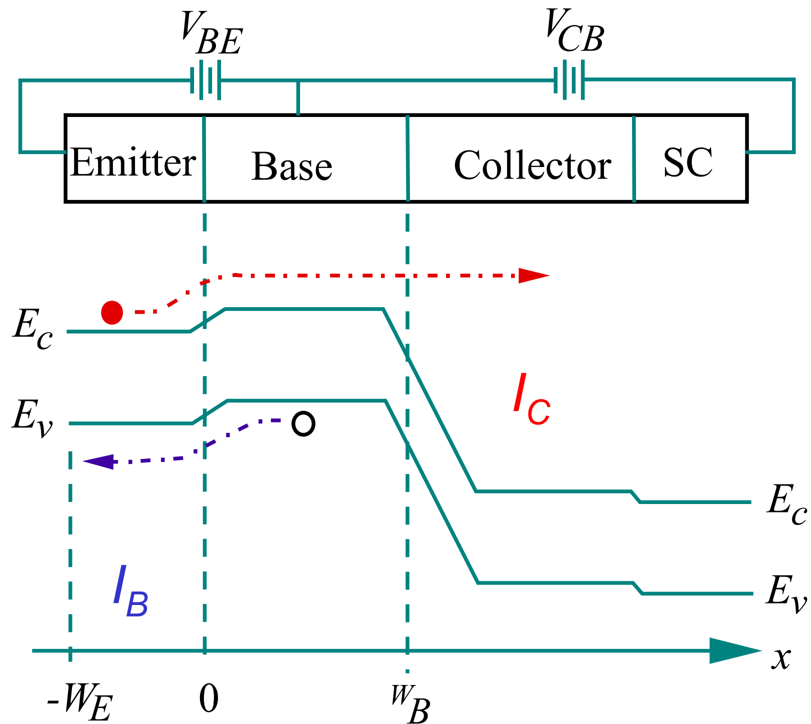
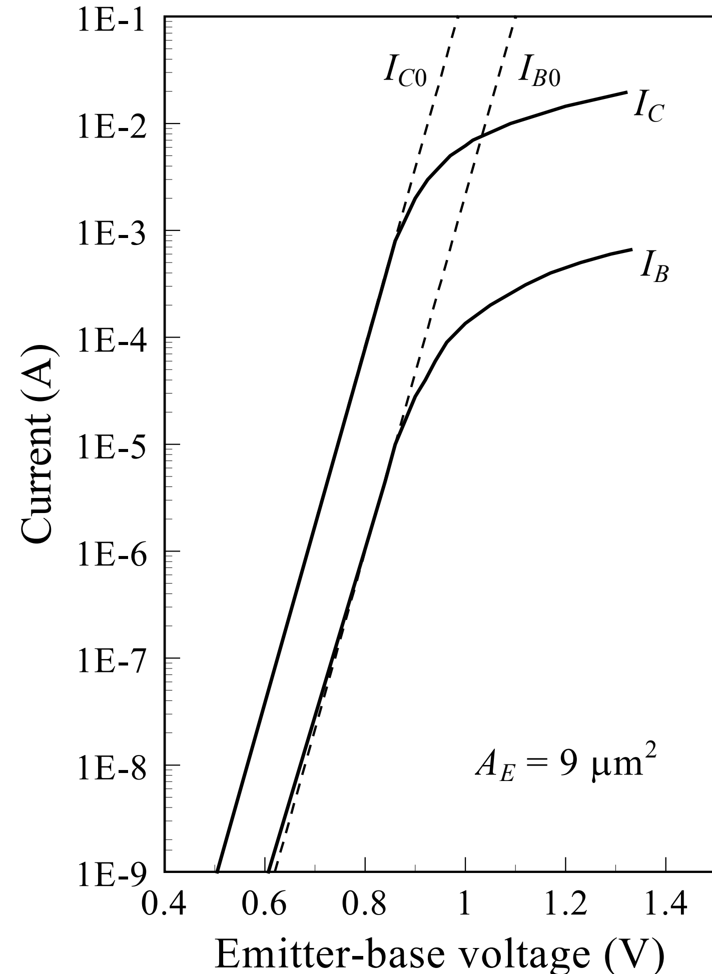
Bipolar Fundamentals

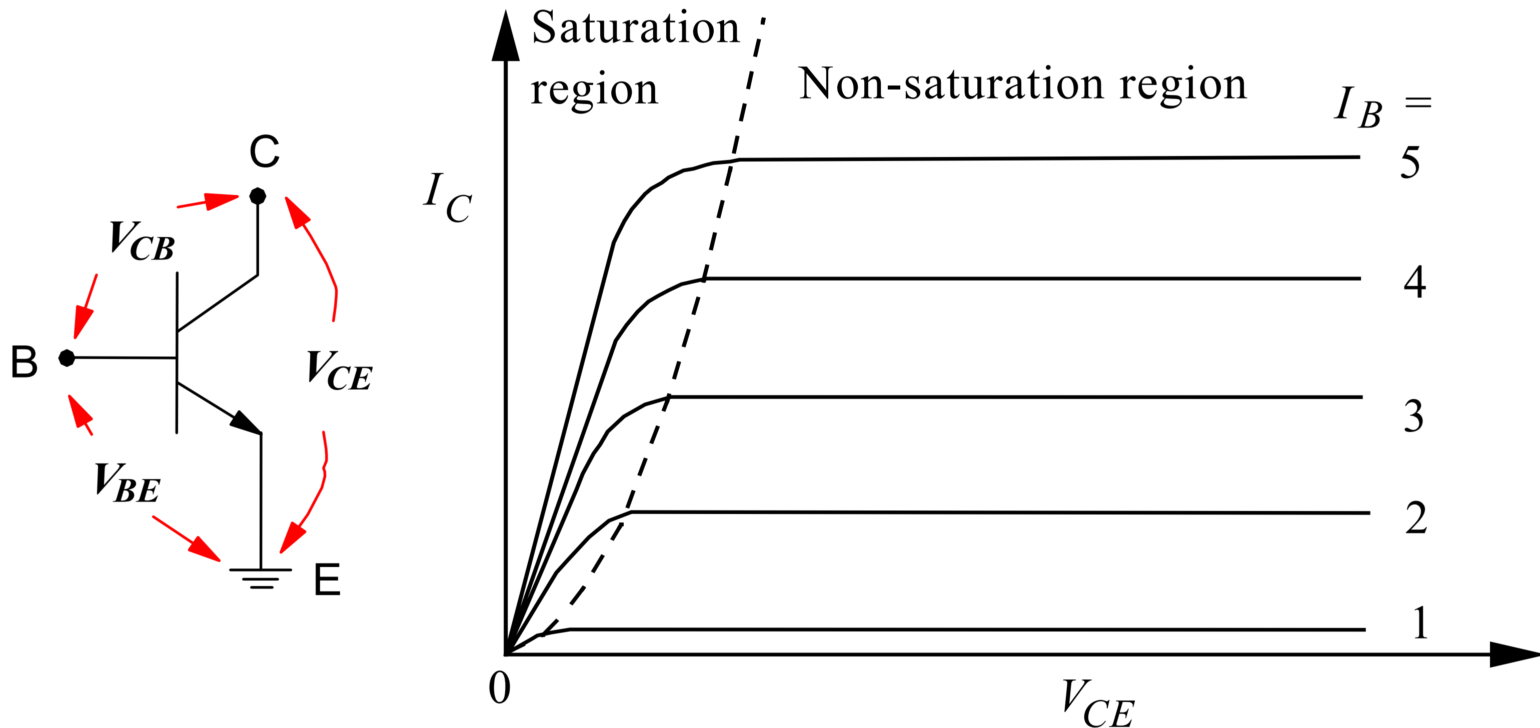




- Base current = holes injected from base into emitter.
- Collector current = electrons injected from emitter into base.

Current Gain $\beta = I_C/I_B$

Ideal I-V Characteristics



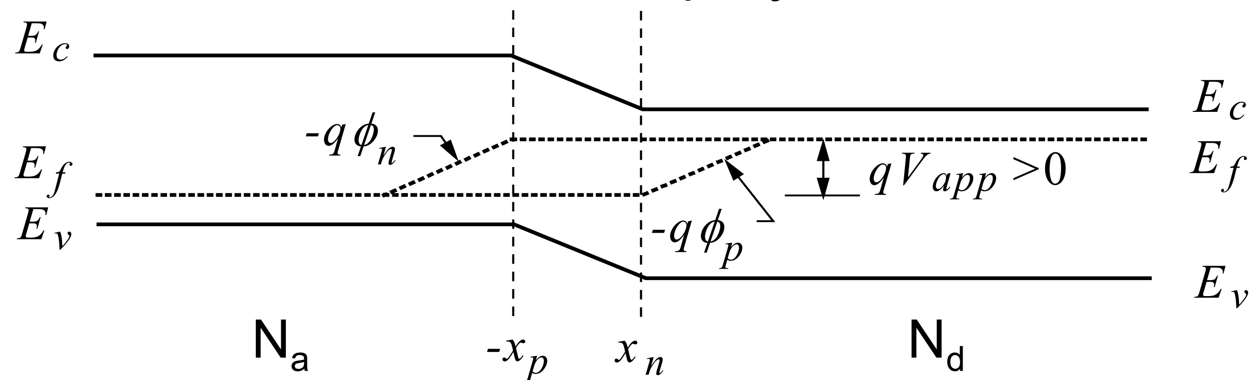
- Saturation region: $V_{CE} < V_{BE}$
  -- both E-B diode and C-B diode are forward biased

- Non-saturation region: $V_{CE} > V_{BE}$
  -- E-B diode forward biased, C-B diode reverse biased

Quasi-Fermi Level

Non-equilibrium: $pn = n_i^2 \exp\left[q(\phi_p - \phi_n)/kT\right]$

A forward biased p-n junction:



Excess electrons: $n_p(x=-x_p)=(n_i^2/N_a)\exp(qV_{app}/kT)$

Excess holes: $p_n(x=x_n)=(n_i^2/N_d)\exp(qV_{app}/kT)$

So collector current is inversely proportional to base doping,

And base current is inversely proportional to emitter doping.

Excess Electrons in the p-Region

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} - R_n + G_n = 0 \qquad J_n = -qn\mu_n\left(\frac{d\psi}{dx} - \frac{kT}{qn}\frac{dn}{dx}\right) = \mu_n kT\frac{dn}{dx} \qquad R_n - G_n = \frac{n - n_0}{\tau_n}$$

$$\frac{d^2 n_p}{dx^2} - \frac{n_p - n_{p0}}{L_n^2} = 0,$$

where $L_n \equiv \sqrt{\tau_n D_n} = \sqrt{\frac{kT\mu_n\tau_n}{q}}$ is the minority carrier diffusion length.

Boundary conditions:

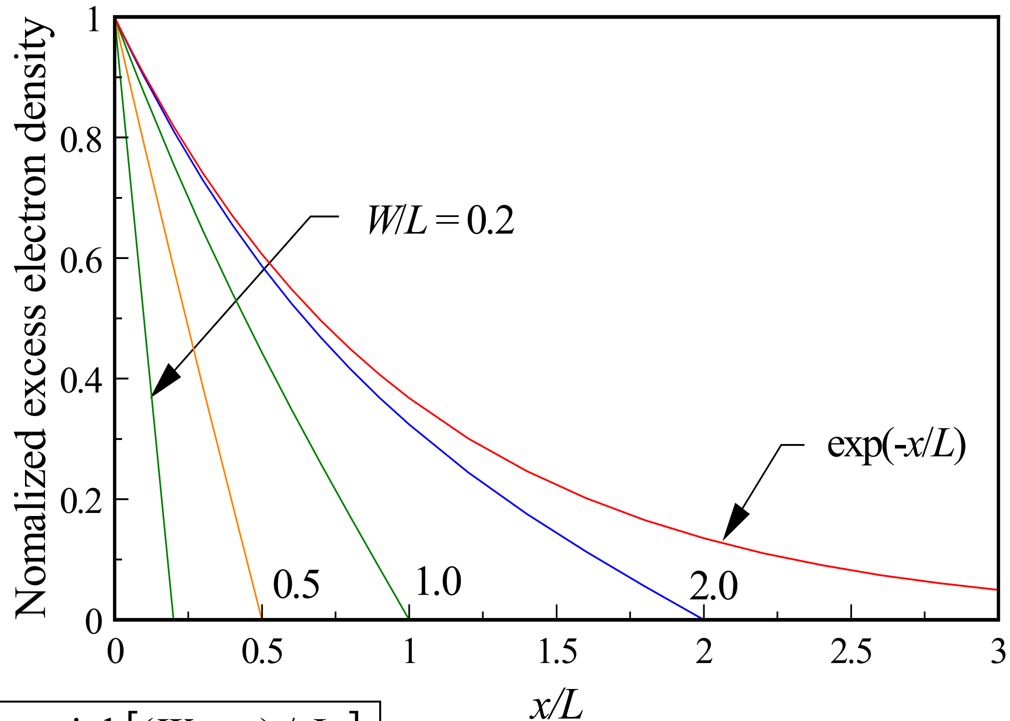
$n_p = n_{p0}\exp\left(qV_{app}/kT\right)$

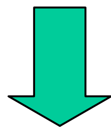
at x=0,

and

$n_p = n_{p0}$

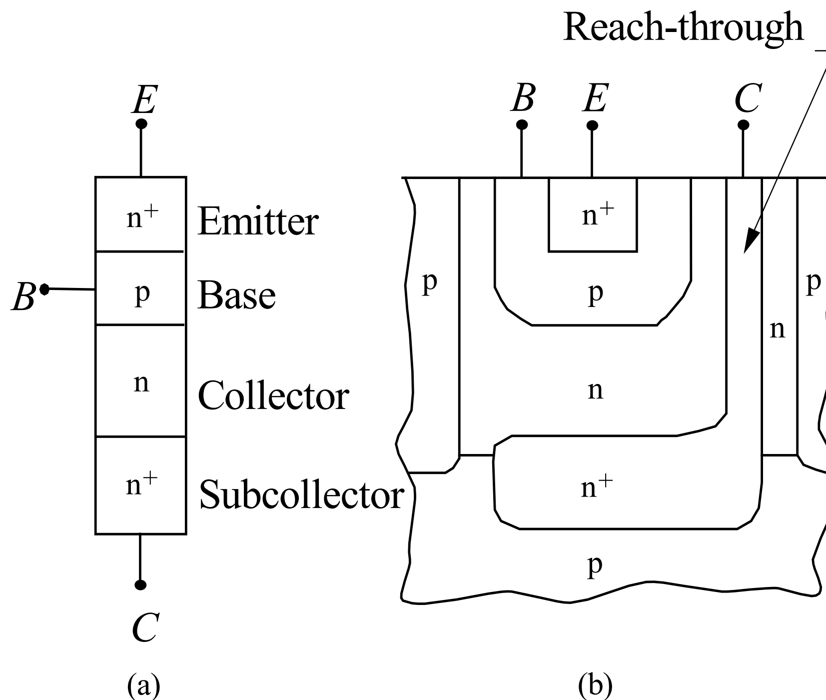
at x=W (ohmic contact).





$$n_p - n_{p0} = n_{p0}\left[\exp(qV_{app}/kT) - 1\right]\frac{\sinh\left[(W-x)/L_n\right]}{\sinh(W/L_n)}.$$

Bipolar Design Considerations

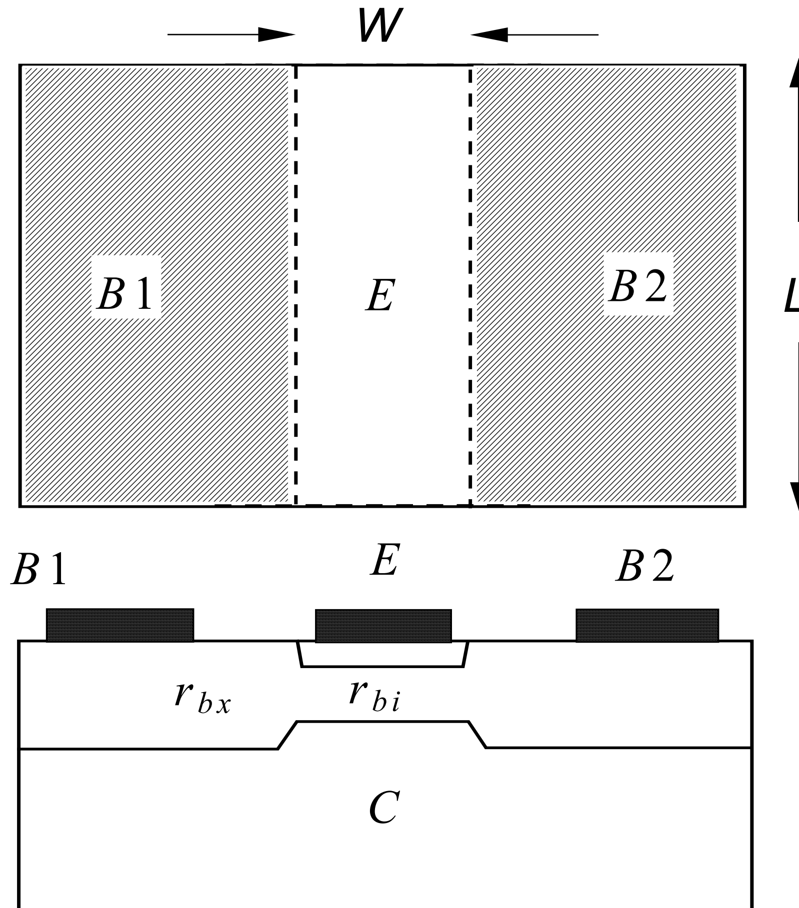


- **Base:**
  --Thin base means higher current gain and smaller stored charge, therefore higher performance.
  --Doping must be high enough to keep base resistance low and avoid E-C punchthrough.

- **Emitter:**
  --Doping as high as possible.
  --Deep emitter gives higher current gain, but difficult to control thin base width.

- **Collector:**
  --Higher collector doping reduces base widening.
  --Higher doping also means higher B-C capacitance.
  --Need highly doped sub-C to minimize resistance.

Intrinsic-Base Resistance



- Intrinsic base sheet resistance

$$R_{Sbi} = \left(q \int_0^{W_B} p_p(x) \mu_p(x) dx \right)^{-1}$$

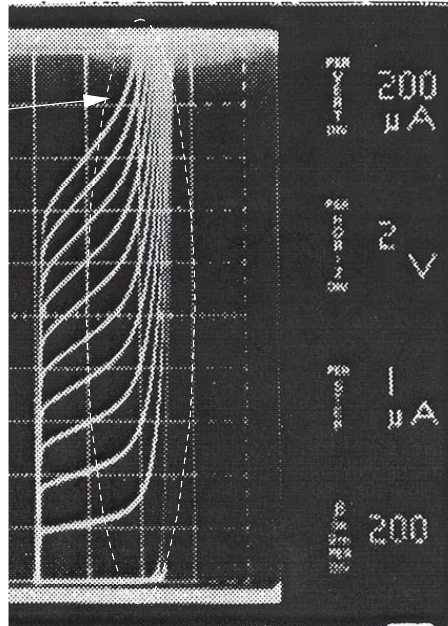
- One base contact only

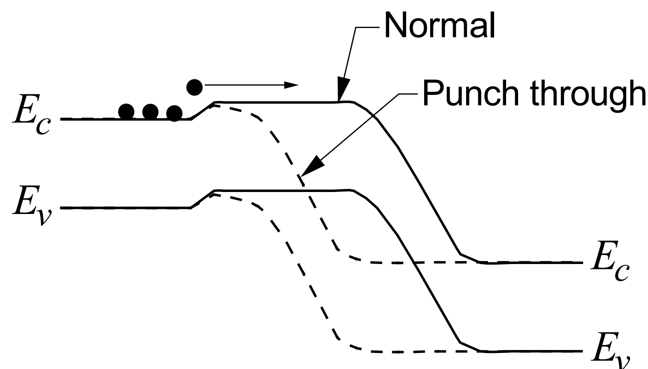
$$r_{bi} = \frac{1}{3} \left(\frac{W}{L} \right) R_{Sbi}$$

- Two-sided base contact

$$r_{bi} = \frac{1}{12} \left(\frac{W}{L} \right) R_{Sbi}$$

Emitter-Collector Punchthrough



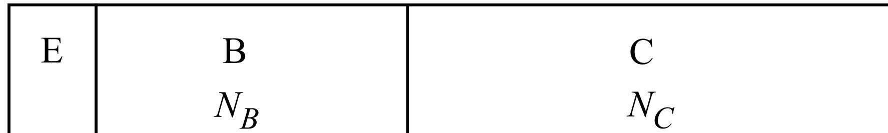


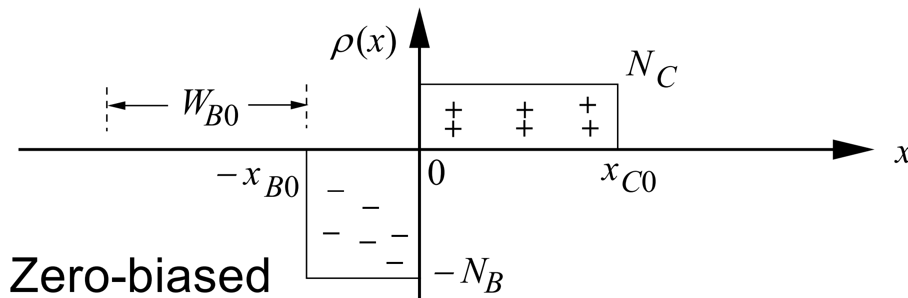
- E-C punchthrough when base width becomes so small that V_{BC} starts to affect the potential barrier of E-B diode. (like drain-induced barrier lowering in MOSFET.)
- When operated near punchthrough, collector current is no longer controlled by V_{BE}.
- Depletion-layer width of a one-sided n$^+$-p diode,

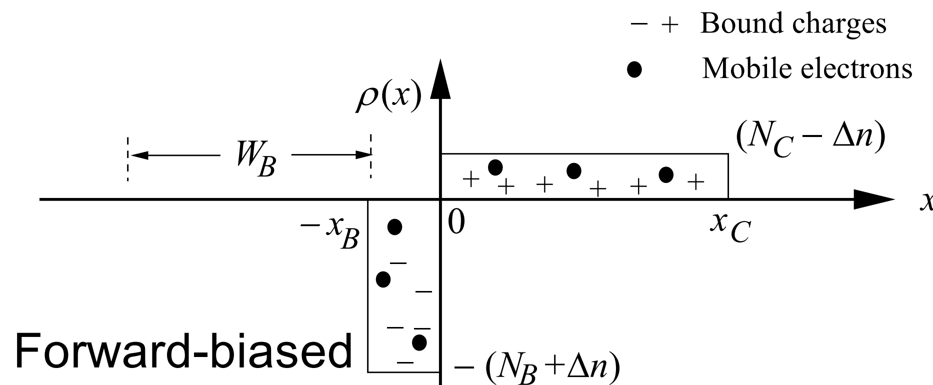
$$W_d = \sqrt{\frac{2\varepsilon_{si}(\psi_{bi} \pm V_{app})}{qN_a}}$$

- To avoid punchthrough as the base width is reduced, the base doping N_B should be increased as $N_B \propto (W_B)^{-2}$.

Base Widening at Low/High Currents





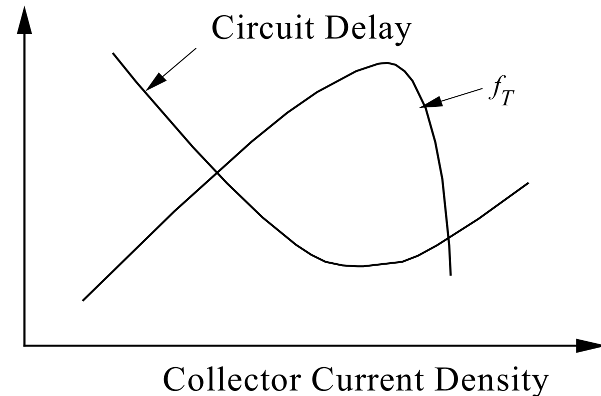


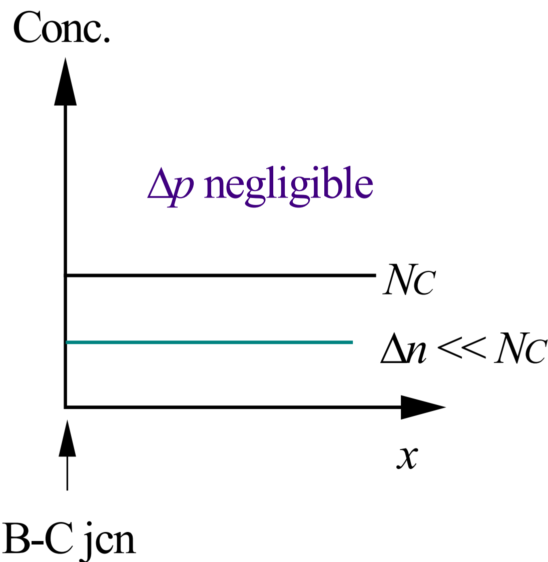
- Low currents:
Mobile electrons adds to space charge in base-collector diode space-charge region. Electric field in B-C junction is reduced.

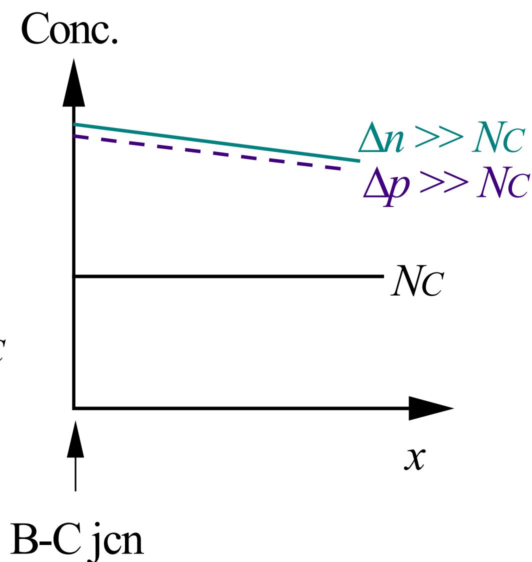
- High currents:
When electron concentration entering collector region is larger than N_C, quasi-neutrality requires that $\Delta p \sim \Delta n > N_C$. The excess hole distribution in collector becomes an "extension" of the p-type base, causing "base widening".

Base Widening and Collector Design

- Performance degrades rapidly with current when collector current density is large enough to cause significant base widening.

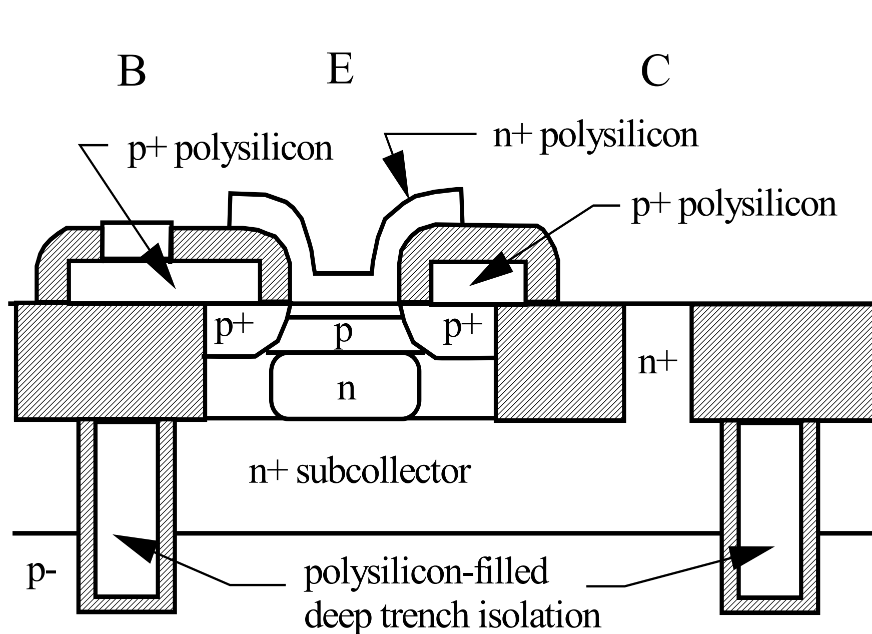


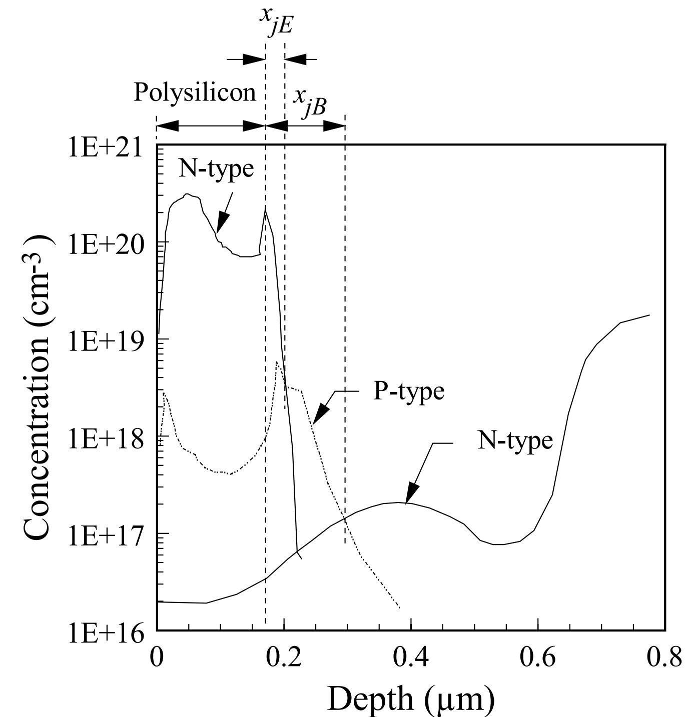




- Maximum J_C without significant base widening is ~ $0.3qv_{sat}N_C$.

Polysilicon Emitter Bipolar Transistor





$$I_B = [qA_E D_{pE} n_{ieE}^2 / N_E W_E] \exp(qV_{BE}/kT)$$

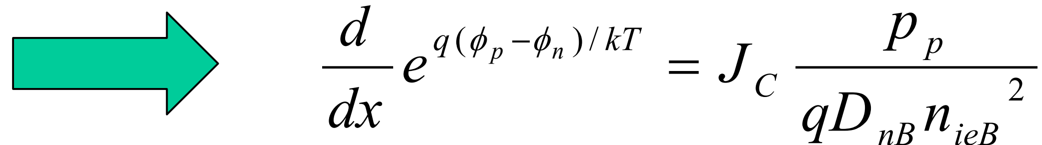
$$I_C = [qA_E D_{nB} n_{ieB}^2 / N_B W_B] \exp(qV_{BE}/kT)$$

$$\beta_0 = \frac{n_{ieB}^2}{n_{ieE}^2} \frac{D_{nB}}{D_{pE}} \frac{N_E W_E}{N_B W_B}$$

Source: Tak Ning, IBM

General Expression for Collector Current

$$J_n(x) = -qn_p\mu_n \frac{d\phi_n}{dx} = -q\mu_n \frac{n_{ieB}^{\;\;2}}{p_p} e^{q(\phi_p - \phi_n)/kT} \frac{d\phi_n}{dx} = \text{constant}$$



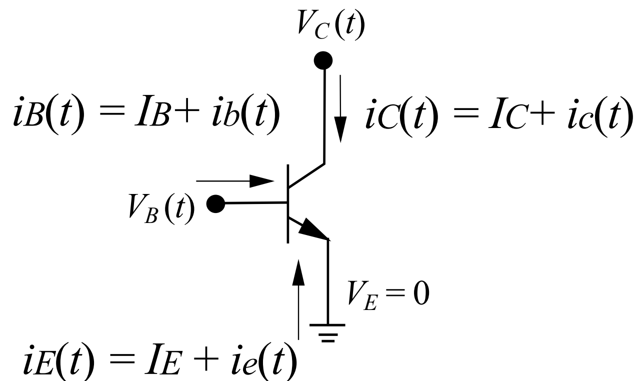
$$\frac{d}{dx} e^{q(\phi_p - \phi_n)/kT} = J_C \frac{p_p}{qD_{nB} n_{ieB}^{\;\;2}}$$

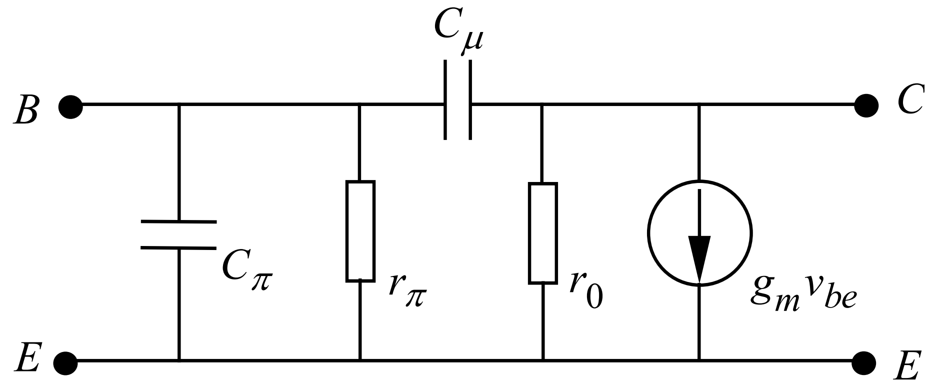
Since $e^{q(\phi_p - \phi_n)/kT} \Big|_0^{W_B} = e^{qV_{BE}/kT}$, integration yields

$$J_C = J_{C0} \exp(qV_{BE}/kT)$$

where $$J_{C0} = \frac{q}{\int_0^{W_B} \frac{p_p(x)}{D_{nB}(x) n_{ieB}^2(x)} dx}$$

Small-Signal Equivalent Circuit

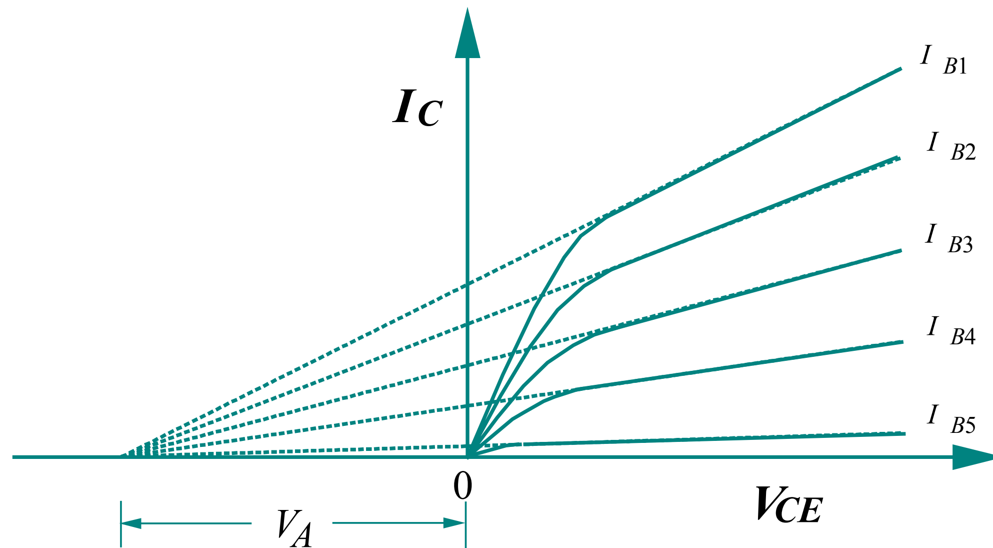




(parasitic resistances neglected)

- Transconductance g_m relates i_c to v_{be}: $g_m = \partial I_C/\partial V_{BE} = qI_C/kT$
- Input resistance r_π relates i_b to v_{be}: $r_\pi = \partial V_{BE}/\partial I_B = kT/qI_B = \beta_0/g_m$
- Output resistance r_0 relates i_c to v_{ce}: $r_0 = \partial V_{CE}/\partial I_C = V_A/I_C$
- Base-collector depletion capacitance: $C_\mu = C_{dBC}$
- Capacitance of emitter-base diode: $C_\pi = C_{dBE} + C_{DE}$

Early Voltage



As V_C increases, the base-collector depletion layer widens so the base width decreases and I_c increases.

$$V_A \approx I_C \left(\frac{\partial I_C}{\partial V_{CE}} \right)^{-1}$$

$$V_A \approx \frac{qD_{nB}(W_B)n_{ieB}^2(W_B)}{C_{dBC}} \int_0^{W_B} \frac{N_B(x)}{D_{nB}(x)n_{ieB}^2(x)} dx \approx \frac{Q_{pB}}{C_{dBC}}$$

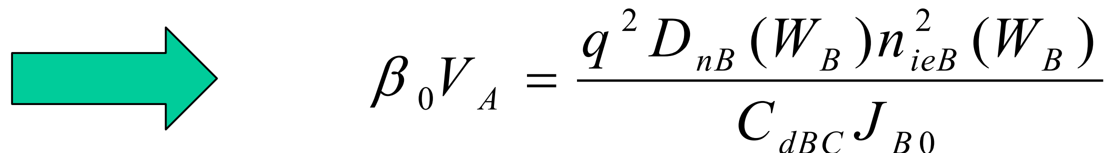
where $C_{dBC} \equiv -dQ_{pB} / dV_{CB}$ and $Q_{pB} = q\int_0^{W_B} p_p(x)dx$

Source: Tak Ning, IBM

The βV_A Product

$$V_A \approx \frac{qD_{nB}(W_B)n_{ieB}^2(W_B)}{C_{dBC}} \int_0^{W_B} \frac{N_B(x)}{D_{nB}(x)n_{ieB}^2(x)} dx$$

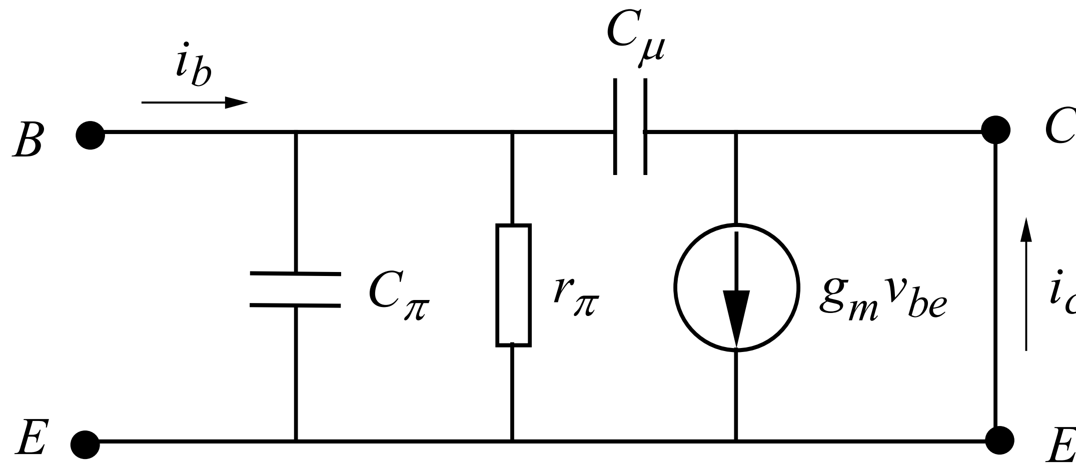
Since $\beta_0 = J_{C0}/J_{B0}$ and $J_{C0} = \dfrac{q}{\displaystyle\int_0^{W_B} \frac{p_p(x)}{D_{nB}(x)n_{ieB}^2(x)} dx}$



$$\beta_0 V_A = \frac{q^2 D_{nB}(W_B)n_{ieB}^2(W_B)}{C_{dBC} J_{B0}}$$

- ❑ βV_A product is a commonly used figure of merit in analog circuits.
- ❑ βV_A product depends on base doping profile only indirectly through the n_{ieB} term.
- ❑ Typical βV_A ~ 4000 V (V_A ~ 40, β ~ 100)

Current Gain Cutoff Frequency, f_T



f_T = transition frequency at which short-circuit load, small-signal current gain drops to unity.

$$i_c = g_m v_{be} - j\omega C_\mu v_{be}$$

$$i_b = \left(\frac{1}{r_\pi} + j\omega C_\pi + j\omega C_\mu \right) v_{be}$$

$$\beta(\omega) = \frac{i_c}{i_b}$$

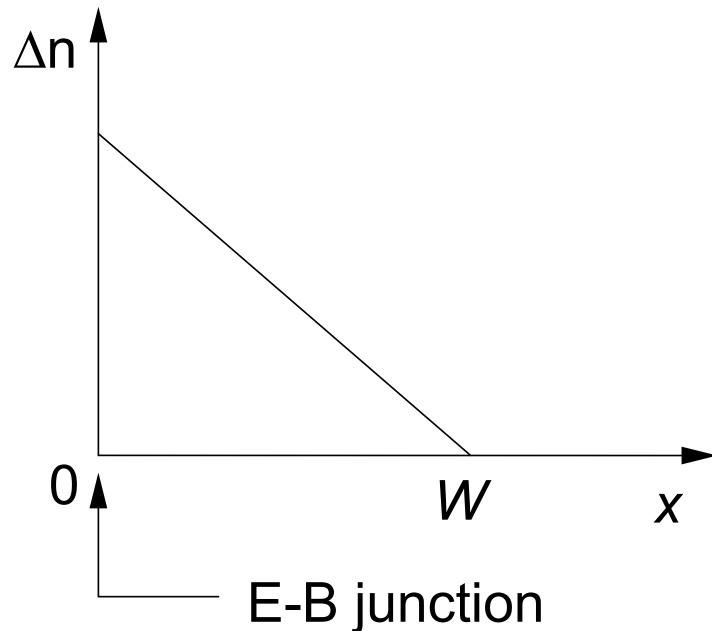
Neglecting parasitic resistances:

$$\frac{1}{2\pi f_T} = \tau_F + \frac{kT}{qI_C}(C_{dBE} + C_{dBC})$$

$$\tau_F = (t_B + t_E + t_{BE} + t_{BC})$$

Base Transit Time

Assume narrow base:



- Electron current in base is constant.

$J_n = qD_n(d\Delta n/dx) = -qD_n\Delta n(0)/W$

- Total excess charge in base

$Q_B = q\Delta n(\mathrm{o})W/2$

- Base transit time t_B given by

$t_B \equiv Q_B/J_n = W^2/2D_n$

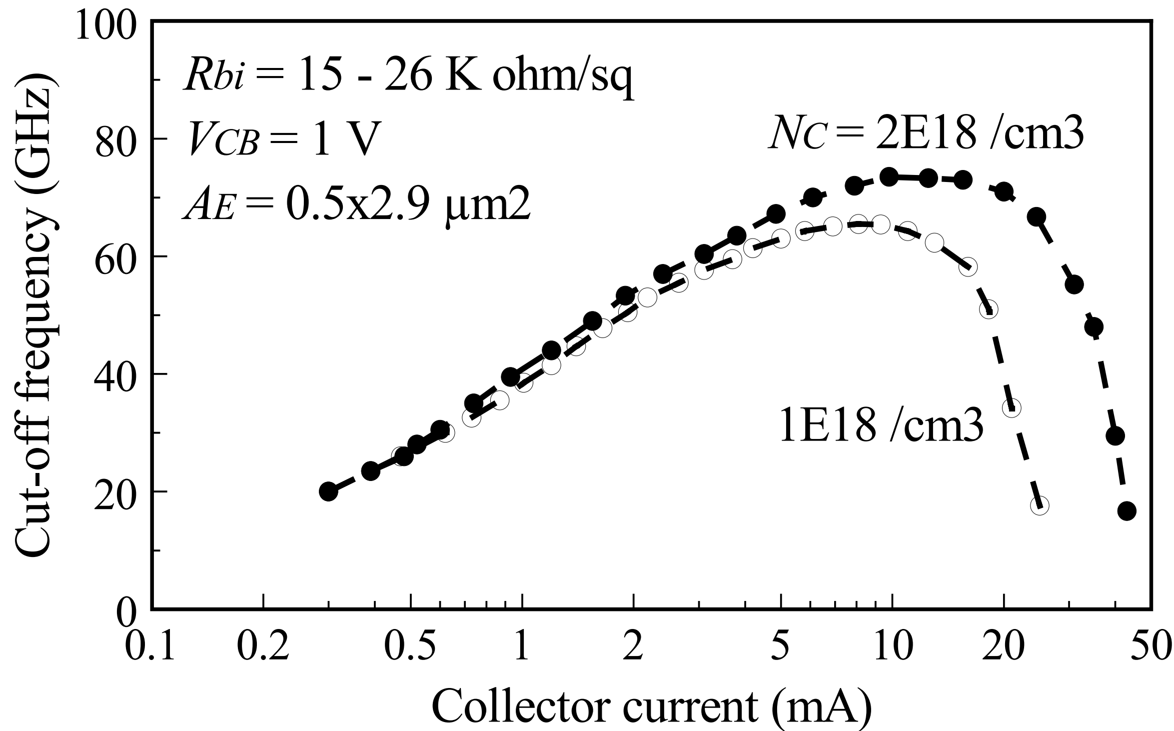
- For W_B = 100 nm, N_B = 2E18 cm^{-3},

$t_B = (W_B)^2 q/2D_{nB} \sim 6$ ps.

$$Q_B = -q\int_0^{W_B} n_p(x)dx \qquad J_C = qD_{nB}\frac{n_{ieB}^2}{p_p}\frac{d}{dx}\left(\frac{n_p p_p}{n_{ieB}^2}\right)$$

$$t_B = \int_0^{W_B}\frac{n_{ieB}^2(x)}{p_p(x)}\int_x^{W_B}\frac{p_p(x')}{D_{nB}(x')n_{ieB}^2(x')}dx'dx$$

Collector Design Trade-off



Reference: E.F. Crabbe *et al*., 1993 IEDM

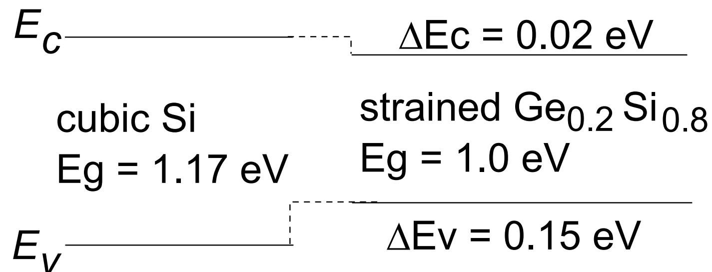
However, higher N_C means

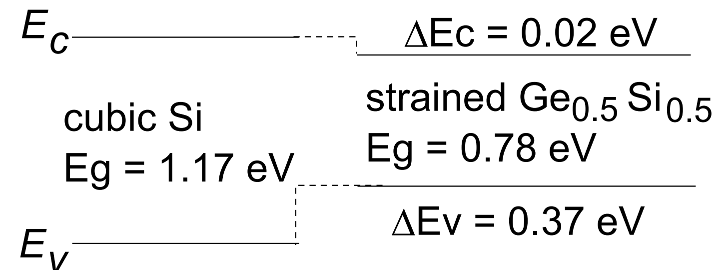
- High C_{dBC}
- Low B-C breakdown voltage
- Small V_A

$$V_A \approx \frac{Q_{pB}}{C_{dBC}}$$

SiGe Bipolar

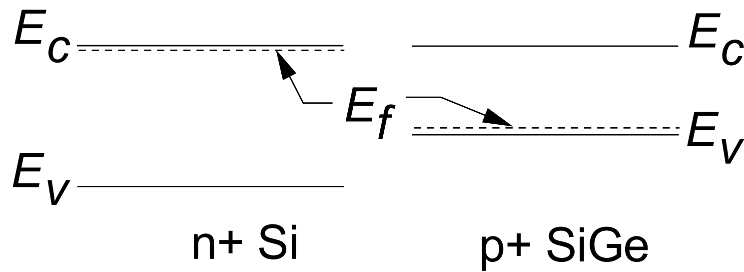
- $E_g(\text{Si}) \approx 1.12$ eV
- $E_g(\text{Ge}) \approx 0.66$ eV
- Incorporation of Ge into Si reduces bandgap of the alloy.

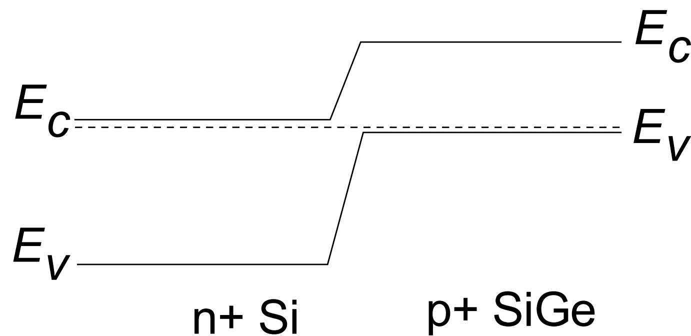


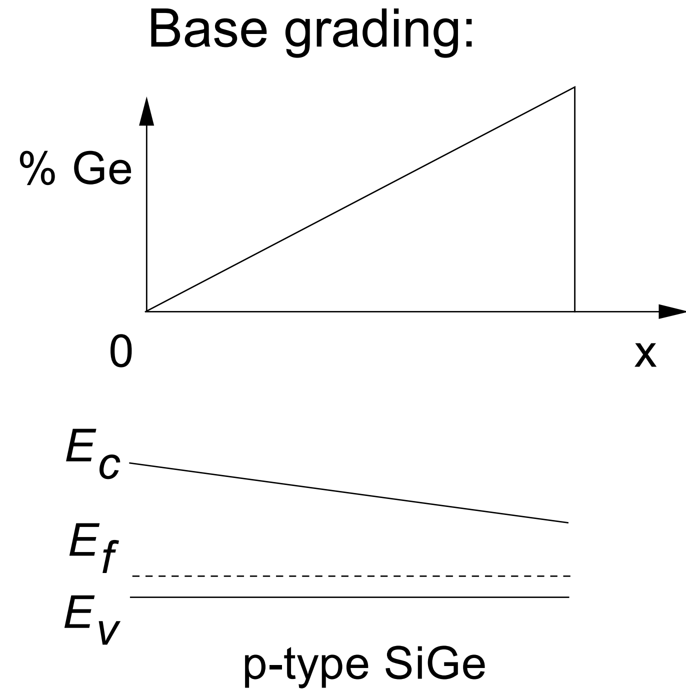


After R. People, IEEE J. QE, QE-22, p. 1696 (1986)

npn Transistor with SiGe Base

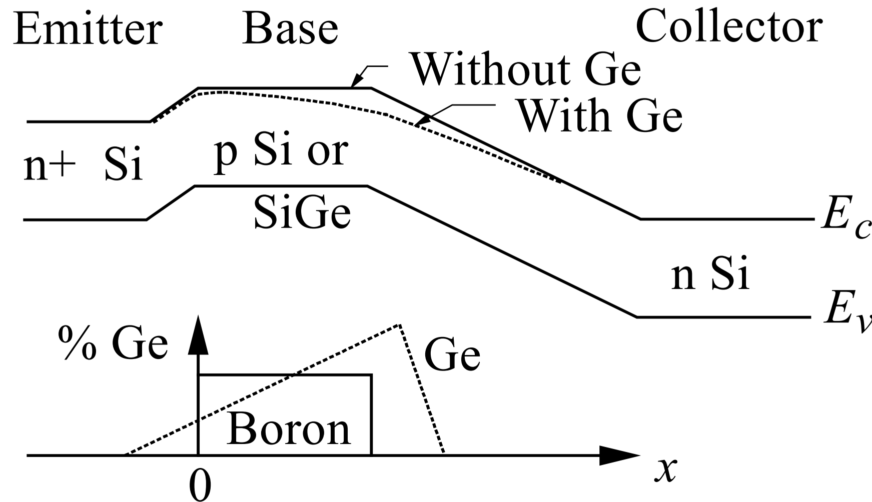






- Barrier for hole injection into n+ Si has not changed, i.e., no effect on base current.
- Barrier for electron injection into p+ SiGe is lowered by the ΔE_g in SiGe, which increases collector current.

Graded SiGe Base



$J_C = J_{C0}\exp(qV_{BE}/kT)$

$$J_{C0} = \frac{q}{\int_0^{W_B} \frac{p_p(x)}{D_{nB}(x) n_{ieB}^2(x)} dx}$$

$$p_0(\Delta E_g) n_0(\Delta E_g) \equiv n_{ie}^2 = n_i^2 \exp(\Delta E_g / kT)$$

$$n_{ieB}^2(\text{SiGe}) = n_{ieB}^2(\text{Si}) \exp\left(\frac{\Delta E_{g,SiGe}}{kT} \frac{x}{W_B} \right)$$

$$\boxed{\frac{J_{C0}(\text{SiGe})}{J_{C0}(\text{Si})} = \frac{\beta(\text{SiGe})}{\beta(\text{Si})} = \frac{\Delta E_{g,SiGe} / kT}{1 - \exp\left(-\Delta E_{g,SiGe} / kT\right)}}$$

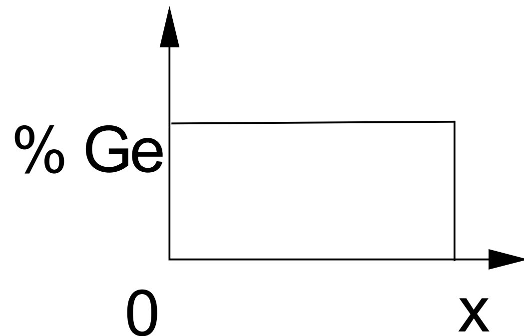
Source: Tak Ning, IBM

Early Voltage: SiGe Base

$$V_A \approx \frac{qD_{nB}(W_B)n_{ieB}^2(W_B)}{C_{dBC}} \int_0^{W_B} \frac{N_B(x)}{D_{nB}(x)n_{ieB}^2(x)} dx$$

$$\frac{V_A(\mathrm{SiGe})}{V_A(\mathrm{Si})} = \frac{kT}{\Delta E_{g,SiGe}} \left[\exp\left(\Delta E_{g,SiGe} / kT \right) - 1 \right]$$

Figure of merit: βV_A product: $$\frac{\beta(\mathrm{SiGe})V_A(\mathrm{SiGe})}{\beta(\mathrm{Si})V_A(\mathrm{Si})} = \exp\left(\Delta E_{g,SiGe} / kT \right)$$



For uniform Ge distribution:

$\beta_0(\mathrm{SiGe}) = \beta_0(\mathrm{Si})\exp(\Delta E_g/kT)$

But no change in Early voltage.

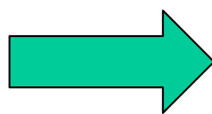
$\Rightarrow \beta V_A(\mathrm{SiGe})/ \beta V_A(\mathrm{Si}) = \exp(\Delta E_g/kT)$

Same as the linearly graded base.

Base Transit Time

$t_B \equiv |Q_B| / |J_C|$ where $Q_B = -q\int_0^{W_B} n_p(x)dx$

$$n_p(x) = \frac{n_{ieB}^2}{p_p} e^{q(\phi_p - \phi_n)/kT} = \frac{J_C}{q} \frac{n_{ieB}^2(x)}{p_p(x)} \int_x^{W_B} \frac{p_p(x')}{D_{nB}(x') n_{ieB}^2(x')} dx'$$



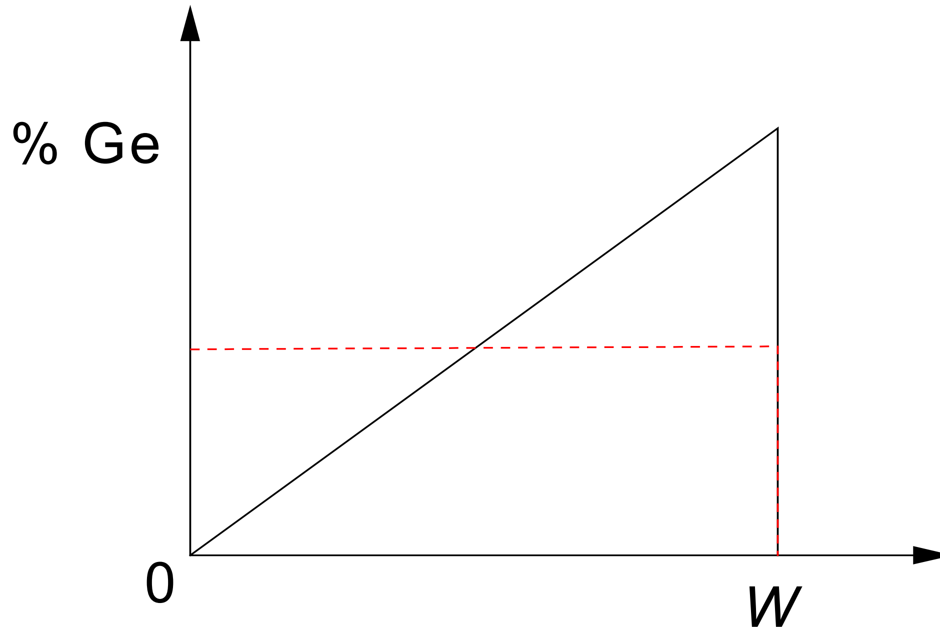
$$t_B = \int_0^{W_B} \frac{n_{ieB}^2(x)}{p_p(x)} \int_x^{W_B} \frac{p_p(x')}{D_{nB}(x') n_{ieB}^2(x')} dx' dx$$

$$\frac{t_B(\mathrm{SiGe})}{t_B(\mathrm{Si})} = \frac{2kT}{\Delta E_{g,SiGe}} \left[1 - \frac{kT}{\Delta E_{g,SiGe}} \left(1 - \exp\left(-\Delta E_{g,SiGe} / kT \right) \right) \right]$$

For uniform Ge distribution, no change in base transit time.

Source: Tak Ning, IBM

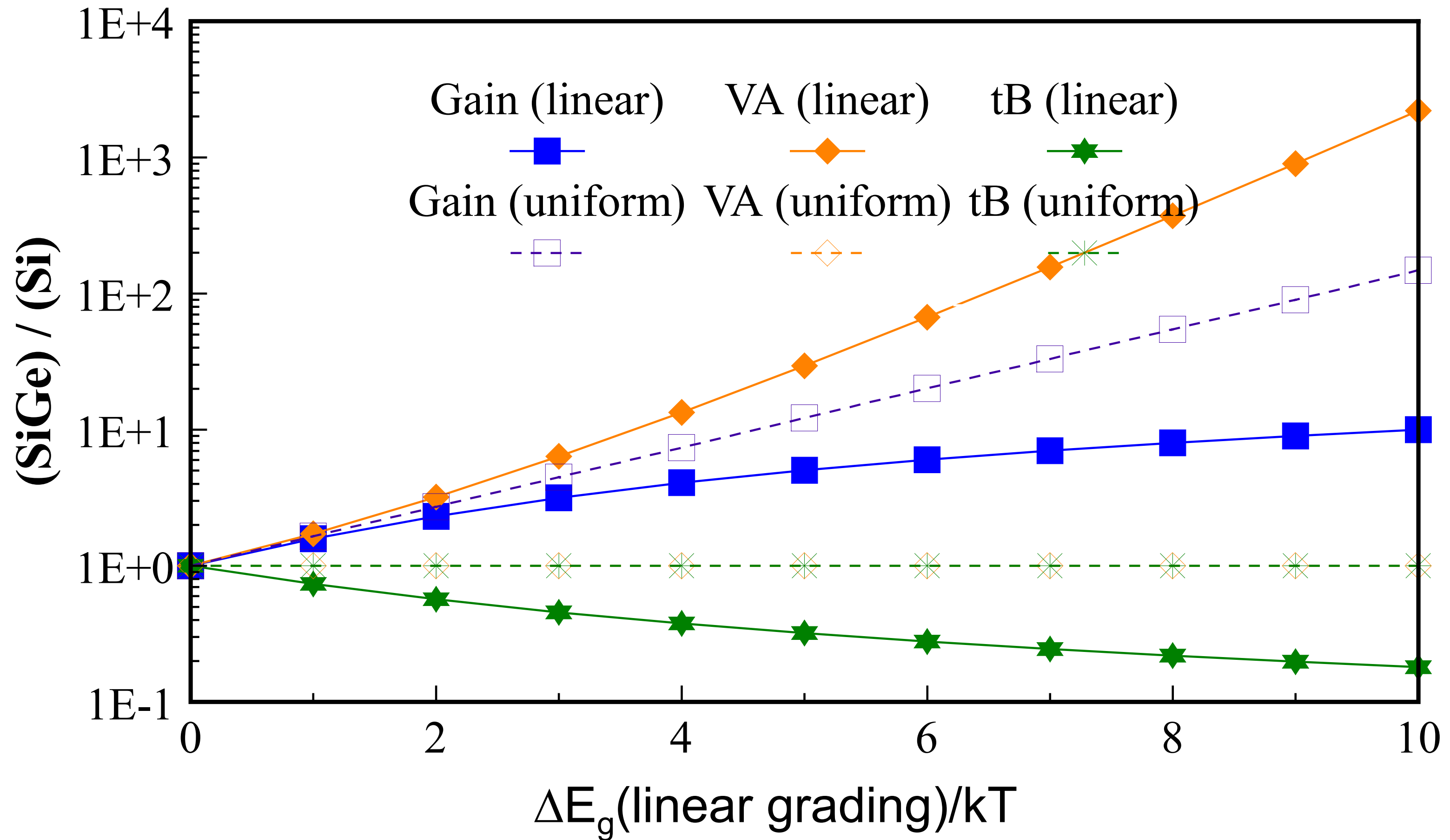
Comparison of Uniform and Linearly Graded Ge Profiles (same total Ge)



- Assume amount of bandgap narrowing is proportional to Ge concentration.

- For the **same amount of total integrated Ge** in the base layer, ΔE_g(linear grading) = $2\Delta E_g$(uniform).

Comparison of Uniform and Linearly Graded Ge Profiles (same total Ge)



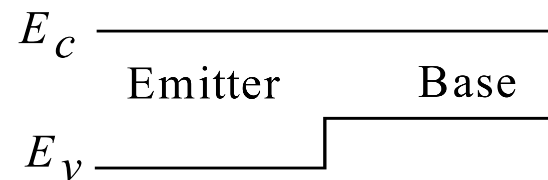
Source: Tak Ning, IBM

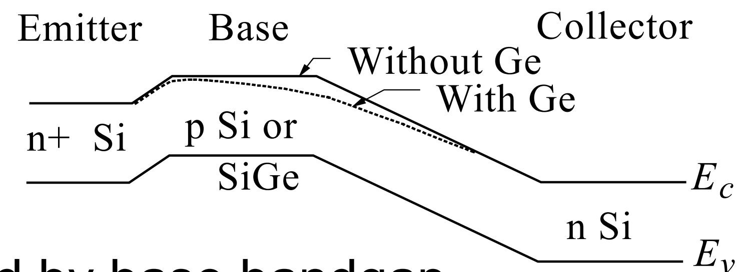
Any Merit with Uniformly Narrow Base Bandgap?

- Current gain improvement can be very large.
- No change in other device parameters.
- The large current gain can be traded off for much smaller base resistance.
  - -- Early voltage is increased.
  - -- However, increase in intrinsic base doping concentration will increase C_{dBE}.
- The large current gain cannot be used to reduce emitter doping concentration (like in compound-semiconductor HBT's), without regineering the polysilicon emitter process.

Heterojunction Bipolar Transistor?

- Traditional heterojunction emitter:
  - Emitter bandgap larger than the base bandgap at the E-B junction.
  - Base current suppressed by the large hole injection barrier.
  - Emitter doping concentration can be very low.
  - C_{dBE} much smaller than non-heterojunction emitter transistor.
  - Collector current not affected.





- SiGe-base bipolar as an HBT:
  - Emitter parameters not affected by base bandgap engineering.
  - Base current not affected. No change in C_{dBE}.
  - Graded SiGe base bipolar not an HBT in traditional sense.

Source: Tak Ning, IBM

SiGe ECL Delays

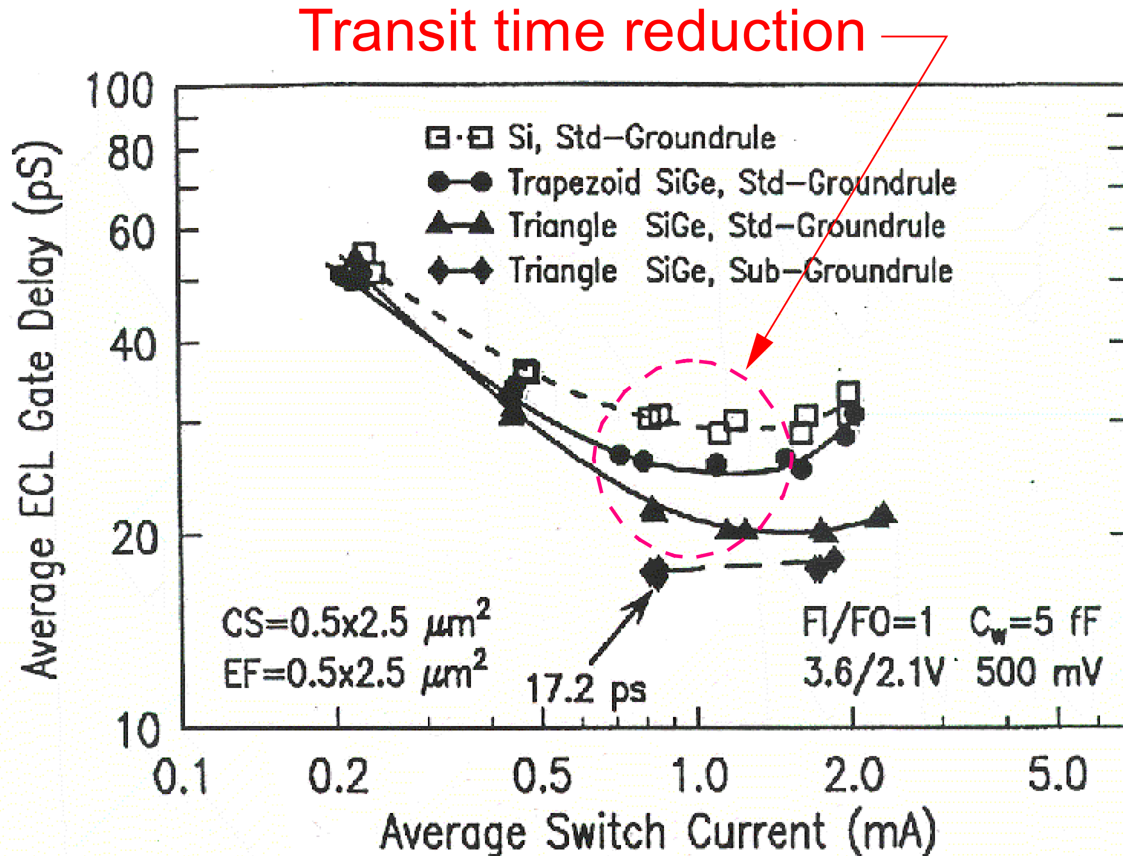
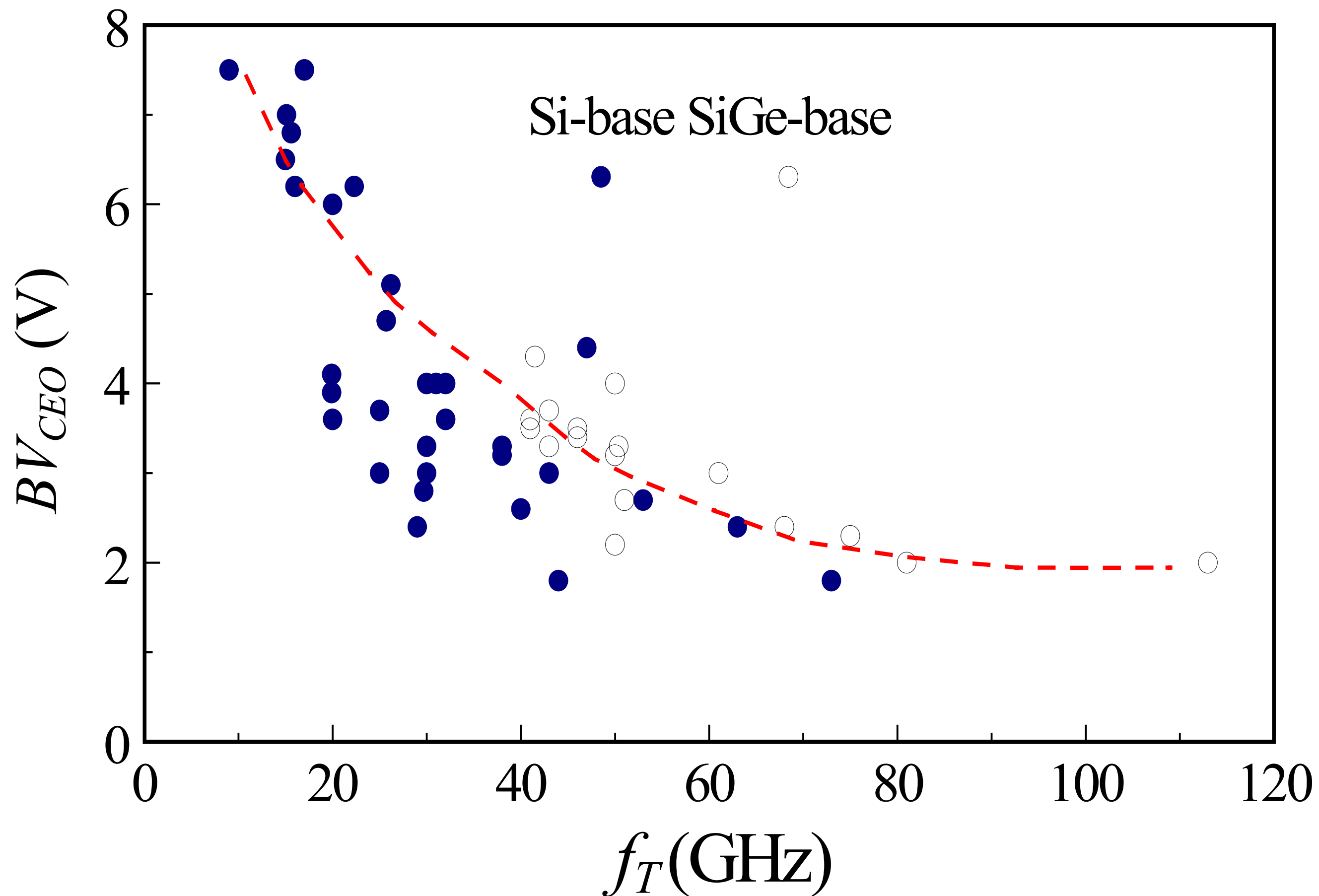


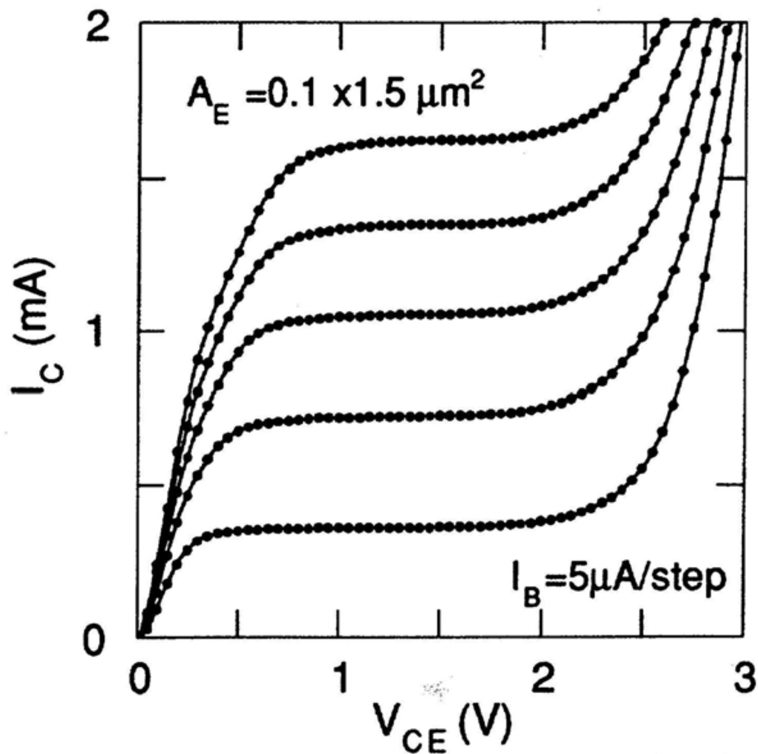
Fig. 13. ECL Ring Oscillator delays for the Trapezoid, and triangle Ge-profile SiGe-HBTs, and the Si-BJT. All have medium implanted collector profiles and the Triangle SiGe-HBT includes a sub-ground-rule transistor layout.

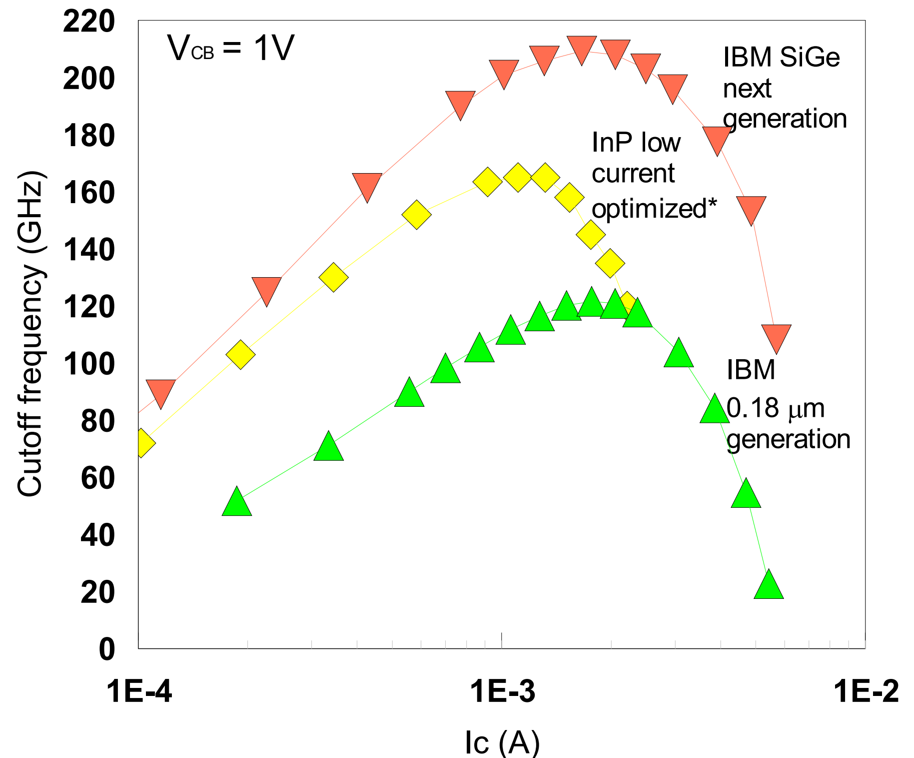
Reference: Harame et al., IEEE Trans. ED 42, p. 455 (1995)

Maximum f_T Limited by B-C Breakdown



SiGe-Base Bipolar Transistor





* Electron Device Letters Jan 2001

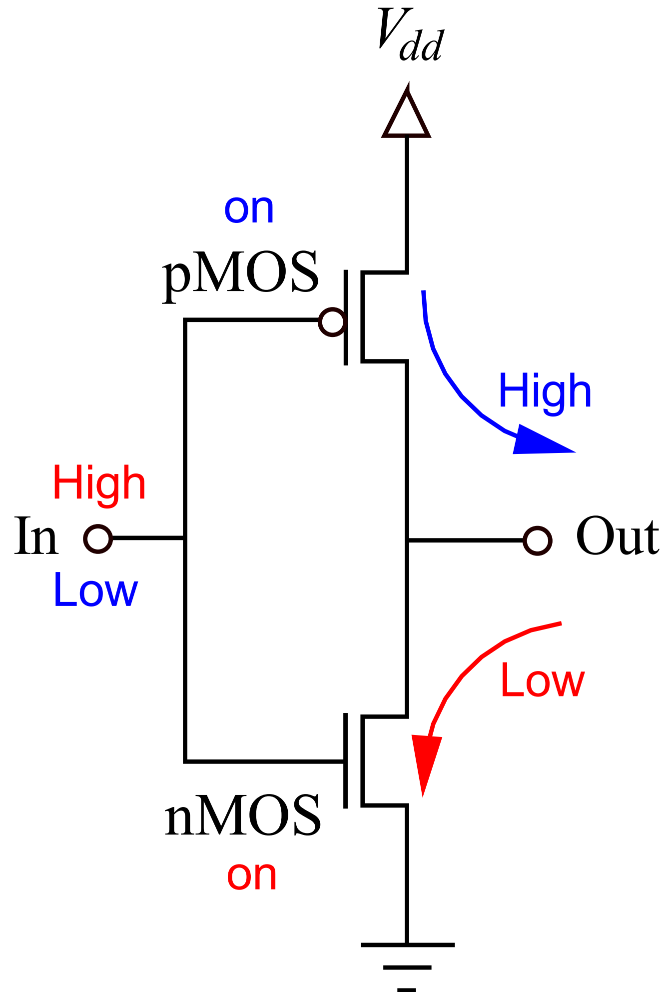
After K. Washio et al., 1997 IEDM

Bipolar and MOSFET Comparison

Bipolar	MOSFET
$I_C = I_{C0}\exp(qV_{BE}/kT)$	$I_{ds} = (1/2)\mu C_{ox}(W/L)(V_g - V_t)^2$ or $I_{ds} = C_{ox}Wv_{sat}(V_g - V_t)$
$g_m = I_C/(kT/q)$	$g_m = 2I_{ds}/(V_g - V_t)$ or $I_{ds}/(V_g - V_t)$
$C_{BE} = \tau_t qI_C/kT$	$C_g = C_{ox}WL + 2C_{ov}W$
$f_T = 1/2\pi\,\tau_t$	$f_T = v_{sat}/2\pi L$ (intrinsic)

Transit time $\tau_t \sim 0.1\text{-}1$ ps

The Magic of CMOS Circuit



- Negligible standby power dissipation.
- Focus all power budget to switching events.
- Key to VLSI integration with low activity factors.
- The only known circuit with such properties.

VLSI Density and Feature Size vs. Time