EE566 Solid State Devices

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Dept of Electrical Engineering
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Assignment 8
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Reading
Chapters 7 and 8 of Muller/Kamins/Chan **(MKC).**

Problem 1 (High-injection effect I- Degradation of Transistor gain)
Problem 7.9, **MKC**.

Problem 2 (High-injection effect II - Kirk-Effect)
An *npn* HBT has a collector consisting of layers of two different materials - A and B. The electron velocity at high field in material A is v_{sat}, whereas that in material B is $v_{sat}/2$. It is also known that material A has a lower breakdown voltage than material B. The two layer thicknesses are the same $W_A=W_B=W_C/2$, where W_C is the total collector width. The (light) doping in the collector is N_{DC} throughout, and the doping in the subcollector is very high. Assume for this problem that the DC reverse bias voltage across the collector-base junction completely depletes the collector region.

- Consider the case when layer A is adjacent to the base.
  a) Draw the charge, electric field, and potential profiles when the Kirk-threshold current is reached.
  b) What is the Kirk-threshold current density J_{Kirk} of this transistor? How does it compare to a HBT with collector of thickness W_C is made entirely of material A?
  c) Derive, and sketch the variation of the effective base width as a function of the collector current J_C assuming the collector is made entirely of material A. Comment on the effects of the base pushout.
- Now consider layer B adjacent to the base.
  d) Repeat parts a) and b) .
  e) Compare the two cases. Which of the two cases will maximize the breakdown voltage under high injection conditions?

Problem 3 (Collector Transit time in a Bipolar Transistor)
Show that the collector transit time in a HBT (or BJT) is given by $\tau_C=W_C/2v_{sat}$, where W_C is the collector thickness, and v_{sat} is the saturation drift velocity at which all carriers are assumed to be moving. Cite any references you study for proving this. Why can you assume saturation velocity in the collector instead of $v=\mu E$? (See problem 7.10, MKC for a reference too - you don't have to solve it!).

Problem 4: (Survey of *ITRS* – the road trip…)
The future of the semiconductor industry (chip, memory, electronic component manufacturers) is guided by a (or THE!) roadmap – the so called **I**nternational **T**echnology **R**oadmap for **S**emiconductors (*ITRS*). Your job in this problem is to assemble your own version of Moore's law – (futuristic) predictions of the path along which the semiconductor (& solid-state devices) industry is headed.

You are to collect data for your own use later – plot the recent past (starting late 90s), current, and projected values for MOSFET (or CMOS) scaling – a) gate lengths, b) gate oxide thicknesses, c) packing densities, d) supply voltages (V_{DD}), e) threshold voltages, f) doping densities, g) speeds, h) static and i) dynamic power dissipation for each *node* (3 or 2-year cycle). Write a small paragraph on any additional information (such as major international players, problems/hindrances ahead with interconnects, lithography, solutions, new and emerging technologies etc) that you find interesting. Make generous use of resources available on the web – the ITRS website at http://public.itrs.net is a good start. Use other websites (such as Intel, IBM, TSMC etc) and of course Google to put together your graphs and paragraphs. This could be time-consuming, but I want you to get introduced to the real world of solid state devices based on silicon by this exercise.
p.s. This question seems straight out of a business school final exam!