EE566 Solid State Devices

Spring 2005
Dept of Electrical Engineering
University of Notre Dame
Instructor: Debdeep Jena (djena@nd.edu, x8835)

Assignment 10

SOLUTIONS

PROBLEM 1

ASSGN 10 - Soln by K. Wang

7.18 $\quad Q_n(y) = C_{ox}\cdot[V_G - V_T - V(y)]$

(a). $I_D = \mu_n C_{ox}\frac{W}{L}[(V_G - V_T - \frac{1}{2}V_D)V_D]$

$= W\, Q_n(y)\,\mu_n\frac{\partial V(y)}{\partial y} = W\, C_{ox}[V_G - V_T - V(y)]\,\mu_n\frac{\partial V(y)}{\partial y}$

$(V_G - V_T - \frac{1}{2}V_D)V_D = L\cdot[V_G - V_T - V(y)]\frac{\partial V(y)}{\partial y}$

$\int_0^y (V_G - V_T - \frac{1}{2}V_D)V_D\, dy = L\int_0^y (V_G - V_T - V(y))\, dV(y)$

$V(y=0) = 0$

S, D, V_D, n+, n+, y, x

$\therefore (V_G - V_T - \frac{1}{2}V_D)V_D\cdot y = L(V_G - V_T)V(y) - \frac{1}{2}V(y)^2$

$\frac{1}{2}V(y)^2 - (V_G - V_T)V(y) + \frac{1}{L}(V_G - V_T - \frac{1}{2}V_D)V_D\cdot y = 0$

$V(y) = (V_G - V_T) \pm\sqrt{(V_G - V_T)^2 - \frac{2}{L}(V_G - V_T - \frac{1}{2}V_D)V_D\, y}$

$E(y) = -\frac{\partial V(y)}{\partial y} = \pm\frac{\frac{2}{L}(V_G - V_T - \frac{1}{2}V_D)V_D}{2\left((V_G - V_T)^2 - \frac{2}{L}(V_G - V_T - \frac{1}{2}V_D)V_D\, y\right)^{\frac{1}{2}}}$

Since $V_D > 0$ so ~~to~~ the electric field is $-y$ direction

$E(y) = -\frac{(V_G - V_T - \frac{1}{2}V_D)V_D}{L[(V_G - V_T)^2 - \frac{2}{L}(V_G - V_T - \frac{1}{2}V_D)V_D\, y]^{\frac{1}{2}}}\,\hat{y}$

$V(y) = (V_G - V_T) - \sqrt{(V_G - V_T)^2 - \frac{2}{L}(V_G - V_T - \frac{1}{2}V_D)V_D\, y}$

(b). At the edge of saturation

$V_{D_{sat}} = V_G - V_T$

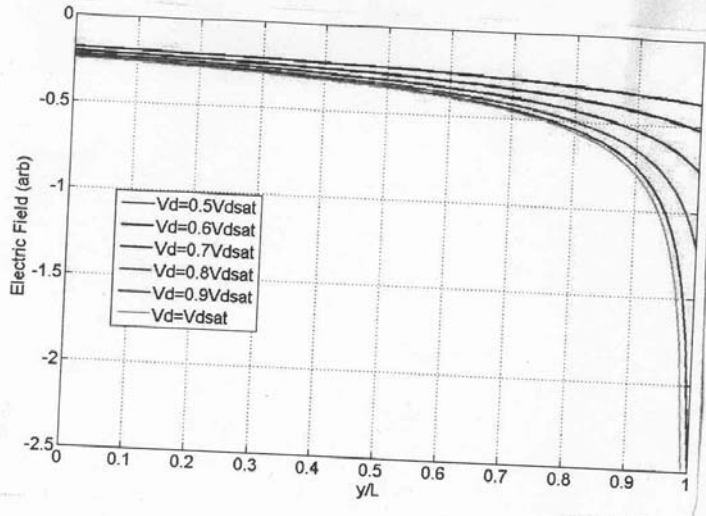
$E(y) = -\frac{(V_G - V_T - \frac{1}{2}(V_G - V_T))(V_G - V_T)}{L[(V_G - V_T)^2 - \frac{2}{L}(V_G - V_T - \frac{1}{2}(V_G - V_T))y(V_G - V_T)]^{\frac{1}{2}}}$

$V(y) = (V_G - V_T) - \sqrt{(V_G - V_T)^2 - \frac{2}{L}(V_G - V_T - \frac{1}{2}(V_G - V_T))(V_G - V_T)\, y}$

$$E(y) = -\frac{(V_G - V_T)}{2L\sqrt{1 - y/L}} = \frac{V_{Dsat}}{2\sqrt{L^2 - y \cdot L}}$$

$$V(y) = (V_G - V_T)\left(1 - \sqrt{1 - y/L}\right) = V_{Dsat}\left(1 - \sqrt{1 - y/L}\right)$$

(c)



As we see near the drain / channel interface, the electric field is very large because the carrier density is very low. With LDD, there will be a low dopant gradient so the electric field is reduce to minimize break down and hot - electron effect.

9.16

PROBLEM 2, ASSGN 10
Sol'n by K. WANG

$$E_{eff} = \frac{(V_G - V_T)}{6\,x_{ox}} + \frac{(V_T + V_Z)}{3\,x_{ox}} = \begin{cases} 0.556 \text{ MV/cm} & V_{DD} = 3.3\text{ V} & \text{NMOS} \\ 0.744 \text{ MV/cm} & V_{DD} = 5\text{ V} & \text{NMOS} \\ 0.4 \text{ MV/cm} & V_{DD} = 3.3\text{ V} & \text{PMOS} \\ 0.589 \text{ MV/cm} & V_{DD} = 5\text{ V} & \text{PMOS} \end{cases}$$

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff}/E_0)^{\nu}} = \begin{cases} 3.846\times10^2 \text{ cm}^2/\text{V.s} & V_{DD} = 3.3\text{ V} & \text{NMOS} \\ 3.07\times10^2 \text{ cm}^2/\text{V.s} & V_{DD} = 5\text{ V} & \text{NMOS} \\ 1.018\times10^2 \text{ cm}^2/\text{V.s} & V_{DD} = 3.3\text{ V} & \text{PMOS} \\ 86.9 \text{ cm}^2/\text{V.s} & V_{DD} = 5\text{ V} & \text{PMOS} \end{cases}$$

$$v_{sat} = \begin{cases} 8\times10^6 \text{ cm/s} & \text{electrons} \\ 6\times10^6 \text{ cm/s} & \text{holes} \end{cases}$$

$$E_{sat} = 2\frac{v_{sat}}{\mu_{eff}} = \begin{cases} 4.16\times10^4 \text{ V/cm} & V_{DD} = 3.3\text{ V} & \text{NMOS} \\ 5.21\times10^4 \text{ V/cm} & V_{DD} = 5\text{ V} & \text{NMOS} \\ 1.179\times10^5 \text{ V/cm} & V_{DD} = 3.3\text{ V} & \text{PMOS} \\ 1.38\times10^5 \text{ V/cm} & V_{DD} = 5\text{ V} & \text{PMOS} \end{cases}$$

$$V_{Dsat} = \frac{E_{sat} \cdot L_{eff}\,(V_G - V_T)}{E_{sat} L + (V_G - V_T)} \qquad C_{ox} = \frac{\epsilon}{d} = \frac{3.9 \times 8.854\times10^{-14}}{15\times10^{-7}} = 2.3\times10^{-7} \text{ F/cm}$$

$$I_{Dsat} = W C_{ox} (V_G - V_T - V_{Dsat})\, v_{sat}, \qquad g_{msat} = W v_{sat} C_{ox} \frac{(V_G - V_T)(V_G - V_T + 2E_{sat}L)}{(V_G - V_T + E_{sat}L)^2}$$

	NMOS		PMOS	
	$V_{DD} = 3.3$V	$V_{DD} = 5$V	$V_{DD} = 3.3$V	$V_{DD} = 5$V
$L = 0.5\,\mu m$	$V_{Dsat} = 1.1556$ V $I_{Dsat} = 26.6$ mA $g_{msat} = 14.78$ mA/V	$V_{Dsat} = 1.622$ V $I_{Dsat} = 49.315$ mA $g_{msat} = 15.8$ mA/V	$V_{Dsat} = 2.383$ V $I_{Dsat} = 22.3541$ mA $g_{msat} = 8.91$ mA/V	$V_{Dsat} = 3.1214$ V $I_{Dsat} = 35.6158$ mA $g_{sat} = 9.67$ mA/V
$L = 0.02\,\mu m$	$V_{Dsat} = 0.08$ V $I_{Dsat} = 46.398$ mA $g_{msat} = 18.399$ mA/V	$V_{Dsat} = 0.1617$ V $I_{Dsat} = 77.3166$ mA $g_{msat} = 18.406$ mA/V	$V_{Dsat} = 0.2227$ V $I_{Dsat} = 52.173$ mA $g_{msat} = 13.77$ mA/V	$V_{Dsat} = 0.2655$ V $I_{Dsat} = 75.09$ mA $g_{sat} = 13.78$ mA/V
I_D improvement	74.4%	56.78%	133.6%	110.83%

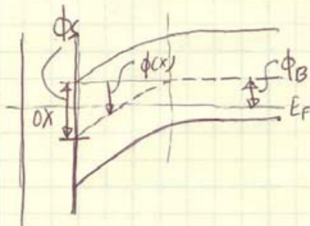
(continue on back of page)

The "constant-field scaling" is to reduce the size of the devices and passive elements in a manner such that internal electric field is remain constant

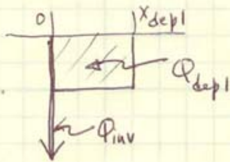
(May 2nd, 05). Debdeep Jena

ASSIGNMENT 10, PROBLEM 3 (a). (Soln is given in detail!).

In class, we had obtained the EXACT expression for the surface electric field, given by



$$|\mathcal{E}_S| = \sqrt{\frac{2kT N_A}{\epsilon_S}}\left[\left(e^{-\frac{q\phi_s}{kT}} + \frac{q\phi_s}{kT} - 1\right) + \frac{n_i^2}{N_A^2}\left(e^{\frac{q\phi_s}{kT}} - \frac{q\phi_s}{kT} - 1\right)\right]^{1/2}$$



Under sub-threshold condition (weak inversion),

$$\phi_B < \phi_s < 2\phi_B \Rightarrow \frac{q\phi_s}{kT} \gg 1$$

$$\Rightarrow |\mathcal{E}_s| \approx \sqrt{\frac{2kT N_A}{\epsilon_s}}\left[\frac{q\phi_s}{kT} + \frac{n_i^2}{N_A^2} e^{\frac{q\phi_s}{kT}}\right]^{1/2}$$

$$\Rightarrow Q_{s,tot} \approx \epsilon_s|\mathcal{E}_s| = Q_{depl} + Q_{inv}$$

Just under threshold, $|\phi_s - 2\phi_B| \ll 2\phi_B$, & $\underbrace{\phi_s < 2\phi_B}$ (-ve).

Also note that $\frac{n_i^2}{N_A^2} = e^{-\frac{2q\phi_B}{kT}}$

$$\Rightarrow Q_{S,tot} \approx \sqrt{2\epsilon_s kT N_A}\left[\underbrace{\frac{q\phi_s}{kT}}_{\gg 1} + \underbrace{e^{\frac{q(\phi_s - 2\phi_B)}{kT}}}_{\ll 1}\right]^{1/2}$$

$$= \sqrt{2q\epsilon_s N_A \phi_s}\left[1 + \frac{e^{\frac{q(\phi_s-2\phi_B)}{kT}}}{q\phi_s/kT}\right]^{1/2}$$

$$\approx \sqrt{2q\epsilon_s N_A\phi_s}\left[1 + \frac{1}{2}\frac{e^{\frac{q(\phi_s-2\phi_B)}{kT}}}{\frac{q\phi_s}{kT}}\right] \quad (\ll 1)$$

$$Q_{s,tot} \approx \underbrace{\sqrt{2q\epsilon_s N_A\phi_s}}_{Q_{depl}} + \underbrace{\sqrt{\frac{\epsilon_s q N_A}{2\phi_s}}\left(\frac{kT}{q}\right) e^{\frac{q(\phi_s-2\phi_B)}{kT}}}_{Q_{inv}}$$

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

Q_{depl} does not contribute to subthreshold current.

All subthreshold current is due to Q_{inv}.

We have derived before that

$$I_{DS} = \mu_{eff} \frac{W}{L} \int_0^{V_{DS}} |Q_{inv}(V)| \, dV \quad \text{— (a)}$$

$$Q_{inv} = \sqrt{\frac{\epsilon_s q N_A}{2\phi_s}} \left(\frac{kT}{q}\right) e^{\frac{q(\phi_s - 2\phi_B)}{kT}} \quad \text{for MOS capacitors}$$

With a Drain-source bias, $\phi_s \rightarrow \phi_s - V(y) = (\phi_s - V)$

$$\Rightarrow \quad Q_{inv}(V) = \sqrt{\frac{\epsilon_s q N_A}{2\phi_s}} \left(\frac{kT}{q}\right) e^{\frac{q(\phi_s - 2\phi_B - V)}{kT}}$$

From (a),

$$\Rightarrow \quad I_{DS} = \mu_{eff} \frac{W}{L} \sqrt{\frac{\epsilon_s q N_A}{2\phi_s}} \left(\frac{kT}{q}\right)^2 \underbrace{e^{-\frac{2q\phi_B}{kT}}}_{=\left(\frac{n_i}{N_A}\right)^2} e^{\frac{q\phi_s}{kT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right) \quad \text{(b)}$$

$$\phi_s = f(V_G) \rightarrow V_G = V_{FB} + \phi_s + \frac{\sqrt{2\epsilon_s q N_A \phi_s}}{C_{ox}}$$

Using the 'good' approximation,

$$\phi_s - 2\phi_B \approx \frac{V_G - V_T}{\left(1 + \frac{C_{depl}}{C_{ox}}\right)} = \eta(V_G - V_T)$$

(b) becomes →

$$I_{DS}(\text{Subthreshold}) \approx \underbrace{\mu_{eff} \frac{W}{L} \left(3 \cdot \frac{t_{ox}}{x_{depl}}\right) \left(\frac{kT}{q}\right)^2}_{I_{d0}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right) e^{\frac{q\eta(V_G - V_T)}{kT}}$$

$$\therefore \quad I_{DS}(V_{DS}, V_{GS}) \approx I_{d0} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right) e^{\frac{q\eta(V_{GS} - V_T)}{kT}}$$

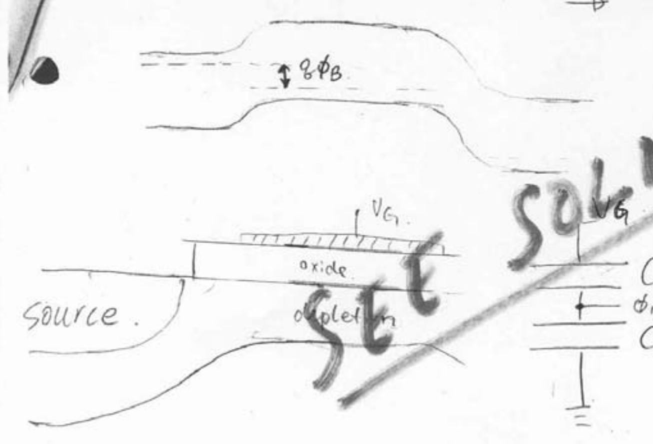
Subthreshold

Note: $I_{DS}(V_{DS} = 0, V_{GS}) = 0$, Very consistent.

P.3 (a) when $V_G < V_T$, the MOSFET is like a n-p-n BJT,

n p n → Explain Why? ... (See soln...)

$$I_D = I_{D0} \cdot \exp\left(\frac{q\phi_B}{kT}\right)$$



SEE SOLN'S

under the gate metal, the depletion layer in semiconductor acts as a capacitor.

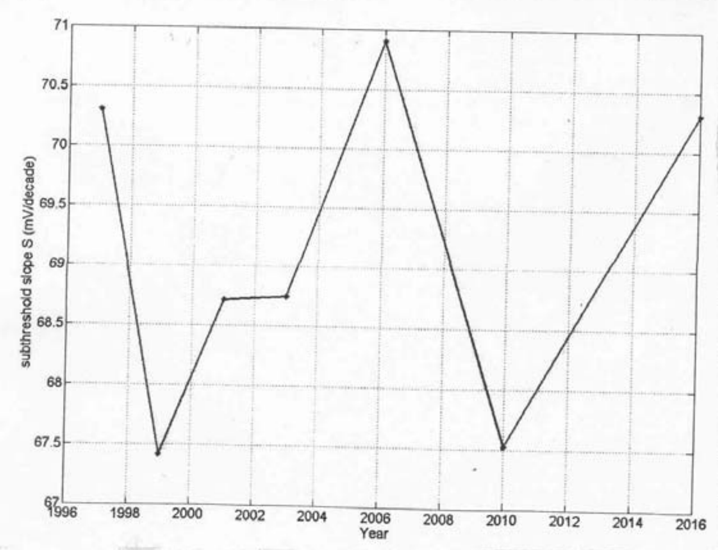
$$\phi_B = \frac{V_{GS}}{1 + C_{dep}/C_{ox}}$$

$$= \frac{V_{GS}}{1 + (\epsilon_S / x_{dep}) / (\epsilon_{SiO_2} / t_{ox})}$$

$$\frac{\epsilon_S}{\epsilon_{SiO_2}} \simeq 3, \quad \therefore \phi_B = \frac{V_{GS}}{1 + 3\frac{t_{ox}}{x_{dep}}}$$

$$\therefore I_{DS} \simeq I_{D0} \exp\frac{\eta q V_{GS}}{kT} \quad \text{where } \eta = \frac{1}{1 + 3\frac{t_{ox}}{x_{dep}}}.$$

(b)



S describes how the dark current changes with applied gate bias. At sub-threshold region, the source-drain current should be as small as possible. If we consider it as a npn BJT, changing the gate voltage is similar to change the barrier of emitter and base so

$$I \propto \exp\left(\frac{q V_{EB}}{kT}\right)$$

In this case, the minimus S is $\eta = 1$,

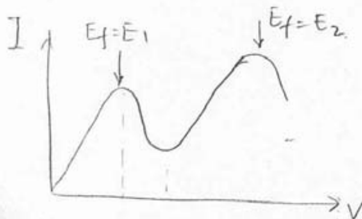
$S = \ln 10 \frac{kT}{q} = 60$ meV/decade.

For smaller S, we can "Turn on" and "Turn off" MOSFET more quickly, so good for digital application

If the gate length is decreased, in subthreshold region the MOSFET is like BJT, gate length is like Base width. The current is diffusion current so with smaller gate length, the current is increased.

(d) Tunnelling diode can improve S

In a tunnelling diode, when the fermi-level outside the quantum well is aligned the same with eigen state inside the well, the current will tunnel through, otherwise there is no current.

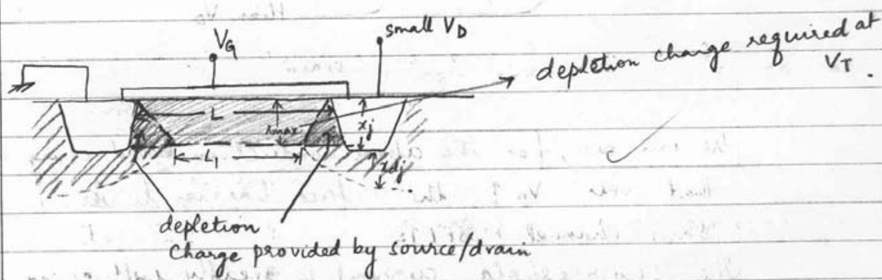


d) Tunnel transistors have lower sub-threshold currents and hence low S. Also, the vertical integration of submicron P-MOSFETs in 2 separate layers of SOI device islands fabricated using selective epitaxial growth and epitaxial lateral overgrowth of Si produces a PMOSFET with S as low as 65mV/dec [John Denton, Purdue]
Carbon nanotube FETs also seem to promise low S.

Problem 4 - ASSIGNMENT 1D - SOLN BY ANJALI.

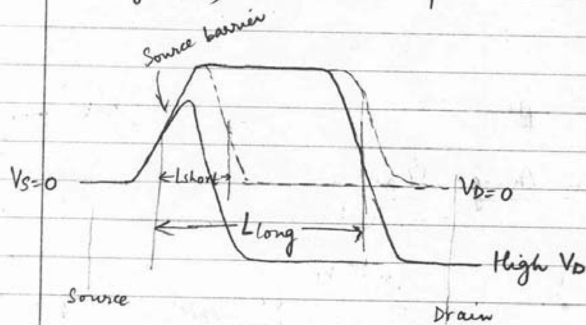
Short Channel Effects are:-

(i) Source - Drain Charge Sharing:-



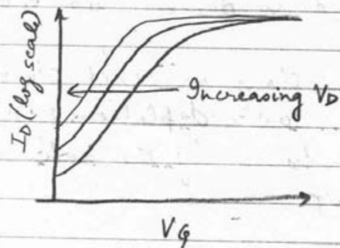
The fixed substrate depletion charge $Q_d = -qN_a x_{dmax} WL$.
We see 2 pieces of the rectangular charge region that are also parts of the source and drain p-n junctions. Therefore no gate voltage is required to deplete the mobile charge from these regions.
Because, some of the bulk charge in short channel MOSFETs is supplied by the drain-source depletion regions, the amount that must be induced by the gate decreases, consequently reducing V_T

(ii) Drain Induced Barrier Lowering (DIBL) This effect refers to the influence of V_D on ϕ_s (the barrier to e^- flow at the np junction near the oxide surface at the source). The density of e^- entering the channel increases exponentially when the barrier is lowered linearly. In LONG channel MOSFETs only V_{GS} lowers ϕ_s. However, with short channel lengths even a high-enough Drain voltage (V_D) can lower ϕ_s.



We can see, from the above conduction band diagram, that when $V_D \uparrow$, the surface barrier lowers for short channel MOSFETS.

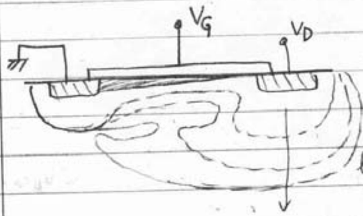
The subthreshold current is greatly influenced by DIBL, and while in long-channel Mosfets, the subthreshold current is independent of V_D, In S-C MOSFETs, it varies with V_D

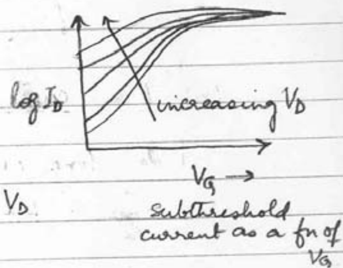


Thus, at a given V_G, if $V_D \uparrow$, $I_D \uparrow$.

(iii) Sub-Surface Punchthrough

This effect refers to the influence of V_D on the source n-p junction e^- barrier, in the substrate, away from the surface. The surface p region in NMOS is more heavily doped than the bulk, making it possible at high V_D for the drain-substrate depletion region to short with the source-substrate depletion region



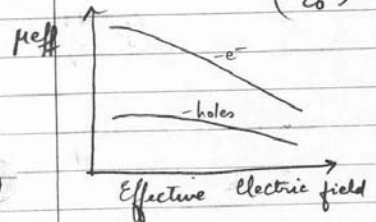


This leads to unacceptably high leakage currents in normally OFF Devices

(IV) Mobility Degradation

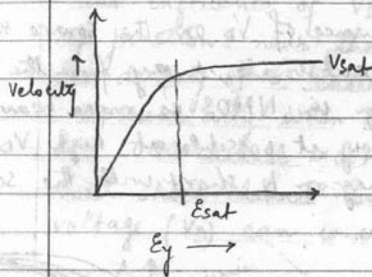
Mobility degradation can be expressed by the following equation

$$\mu_{eff} = \frac{\mu_0}{1+\left(\frac{E_{ff}}{\mathcal{E}_0}\right)^{\nu}} \quad , \text{as } E_{ff}\uparrow , \mu_{eff}\downarrow$$



This is a concern for both long and short channel MOSFETs. But more so, for short channel MOSFETs because the power supply voltage is not scaled as much as suggested by constant field scaling. Hence, $E_{eff}\uparrow$, $\mu_{eff}\downarrow$

(v) Velocity Saturation



At lower field, Velocity ∝ E.
But, in short-channel MOSFETs, fields reach very high values, and carrier velocities approach a limiting value.

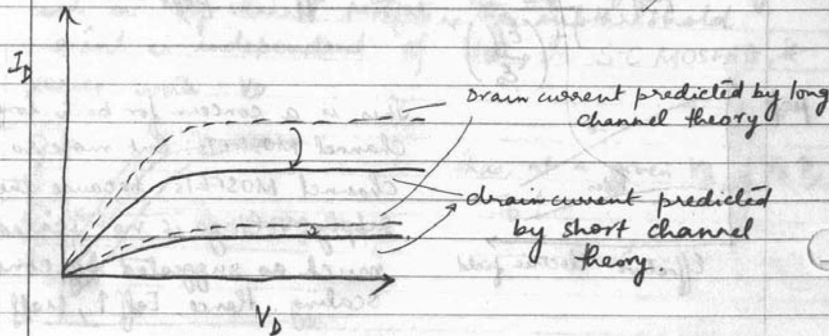
(vi) Drain current

In long channel MOSFETs, we have,

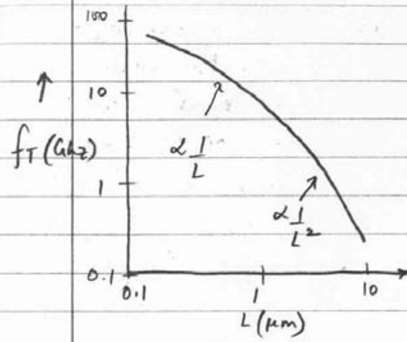
$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \quad \text{till } V_D < V_{Dsat}$$

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_G - V_T)^2$$

But in short channel MOSFETs, the relation is not so simple. Reducing the channel length from 2 μm to 0.02 μm, will not increase the drain current by 100 times. All the short-channel effects come into play, making the gain smaller.



(vii) Speed



Thus, we see that the speed of MOSFETs changes from $\frac{1}{L^2}$ dependence to $1/L$ dependence in the short-channel regime.