EE566 Solid State Devices

Spring 2005
Dept of Electrical Engineering
University of Notre Dame
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Assignment 10
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Due: 04/31/2005

Reading
Chapter 9 of Muller/Kamins/Chan **(MKC).**

Problem 1 (Electric field along the channel of a MOSFET)
Problem **9.18**, MKC. Comment, after drawing the electric field profile from the source to drain region, why in current short gate-length MOSFETs, a lightly-doped-drain (LDD) halo implant is employed to enhance device performance. You can view the LDD MOSFET process flow at the following website - http://www.ee.mnsu.edu/~khaliq/archive/ee5480/modules/lightly.html

Problem 2 (CMOS improvements with scaling)
Problem **9.16**, MKC. Explain the rationale behind the "constant-field scaling" paradigm.

Problem 3 (Subthreshold leakage currents)
Subthreshold leakage current flowing between the source and the drain is a major source of static power dissipation in MOSFET digital logic circuits.
a) Show that the subthreshold leakage current varies with the gate voltage as

$$I_{DS} \approx I_0 e^{\frac{\eta q V_{GS}}{kT}}, \quad \text{where}$$

$$\eta = \frac{1}{1 + 3t_{ox} / x_{depl}}$$

b) Plot the inverse subthreshold slope $S = \ln 10 \cdot (kT / \eta q)$ for various ITRS technology nodes.
c) Explain why a low S is ideal for digital applications. What is the minimum S at room temperature? Explain why as gate lengths get scaled down further, S will increase unless proper care is taken in the design of the MOSFETs.
d) Recently, there have been some proposals of new device architectures to reduce S from the minimum values obtainable in traditional MOSFET design. Do some research and comment on these approaches.

Problem 4 (Short channel effects in MOSFETs)
Explain briefly, using sketches and band diagrams, how short-channel-effect (SCE) changes the device performance as compared to a long-channel MOSFET. You should comment upon such effects as Drain-Induced Barrier Lowering (DIBL), subsurface punchthrough, mobility degradation, carrier velocity in the channel, and the effects on V_T, I_{Dsat}, and the speed f_T of the MOSFET.

NO more assignments!!!