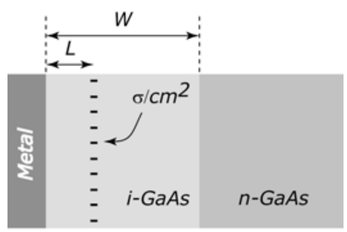
EE566 Solid State Devices

Spring 2005
Dept of Electrical Engineering
University of Notre Dame
Instructor: Debdeep Jena (djena@nd.edu, x8835)

1st Mid-Term Exam
02/18/2005

Problem (20 Points)



There was a glitch in the epitaxial growth of a Mott-barrier diode (*Metal-i-n*) made of GaAs. The n-GaAs is doped with N_D=4.7x10^{17}/cm^3 donors. An unscheduled short opening of the acceptor (Beryllium) source introduced a very thin sheet of acceptors of density σ=10^{11} /cm^2 a distance L=10nm from the surface. The thickness of the *i*-layer is W=80nm. After growth, metal (Aluminum) is deposited on the GaAs surface that results in a barrier height $q\Phi_B$=0.8eV. The resulting structure is depicted in the figure above. Assume that the sheet of acceptors is *totally* depleted. Solve everything analytically first before substituting numerical values.

a) What is the built-in voltage V_{bi} of the modified Mott-barrier diode?

b) Does the metal have zero, positive or negative charge at no applied bias? Justify.

c) Find the depletion region thickness x_d in the n-GaAs layer at zero bias in terms of all known quantities. If there was no acceptor sheet (σ=0 /cm^2) in the *i*-layer, what would be the depletion layer thickness x_{d0} in the n-GaAs layer?

d) From part c, how has the acceptor sheet changed the capacitance of the Mott-barrier diode?

e) Using parts a-c, sketch the band diagram at zero bias *as accurately as you can*.

f) From the band diagram in part e, qualitatively argue why the introduction of the acceptor sheet will result in a *lowering* of the current density when the applied forward bias V_a approaches V_{bi}.

NOTE:
Sketches, sketches with proper LABELS!! (wherever the situation demands). State your approximations clearly, and use your intuition to cut down on the math.
Data: GaAs (300K):
| E_g= 1.424eV | ε_s=12.9ε_0 | ε_0=8.85x10^{-14}F/cm^2 | N_C=4.7x10^{17}/cm^3 | $q\chi$=4.07eV |