
EE566 Solid State Devices

Spring 2005
Dept of Electrical Engineering
University of Notre Dame
Instructor: Debdeep Jena (djena@nd.edu, x8835)

Final Exam 05/04/2005

Time allotted: 2 hours

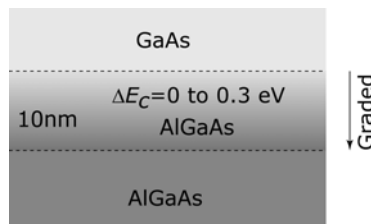
Problem 1 (5 Points)

Recently, organic semiconductors have become very popular for a variety of applications. It is well known that organic semiconductors have

- Very low dielectric constants,
- Weak intermolecular forces, implying very large thermal vibrations of atoms, and
- Narrow conduction-band widths (implying large effective masses).

Explain how these properties affect performance, if you were to make an organic FET.

Problem 2 (8 Points)



Consider the epitaxial GaAs-AlGaAs structure shown above. The 10nm AlGaAs layer is linearly graded. You have to cancel the quasi-electric field seen by ELECTRONS by adding UNIFORM n-type doping N_D in ALL layers.

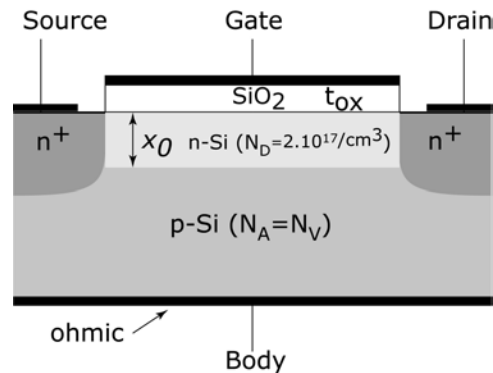
- Draw the band-diagram *before* doping. Identify the magnitude and location of the "quasi-electric" charges necessary for the quasi-electric field in the graded AlGaAs layer.
- Show that uniform doping results in "spikes" formed in the conduction band.
- Using an *exact* method, find the doping N_D that will lead to spikes of magnitude less than $2k_B T$.

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Problem 3 (12 Points)



Consider the so-called "buried-channel" MOSFET device structure shown above. Assume that the gate metal work function is $q\Phi_M = q\chi_{\text{Si}} + E_g$, where $q\chi_{\text{Si}}$ is the electron affinity and E_g is the bandgap of silicon. Your job in this problem is to design the device structure, such that it can be used *both* as a JFET and a MOSFET.

Important notes: Solve everything ALGEBRAICALLY first; all numerical substitutions should be in the FINAL step. Use material parameters from page 54 of the textbook. Neglect Gummel correction. Note that the p-Si layer is degenerately doped.

- Assuming x_0 is large, draw the charge-field-band diagram of the structure along the vertical axis under the gate. Assume that the gate and the body contacts are grounded. *Calculate* and label everything of interest - especially depletion lengths.
- Identify the location of the conducting channel of the transistor, indicate in a sketch. What are the advantages? How is it different from a conventional MOSFET?
- What should x_0 be so that the conducting channel width at $V_{DS}=0$ is $x_I=20\text{nm}$? Fix x_0 at this value for the rest of the problem.
- How will you use the device as a JFET? What will be the threshold voltage of the JFET? Is it enhancement mode or depletion mode?
- How will you use the device as a MOSFET? What is the threshold voltage? Is it enhancement mode or depletion mode? Compare the pros & cons of the two FET modes.