EE566 Solid State Devices

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Assignment 9
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Currents in Mott-Diodes, FETs, and Moore's Law

Problem 1: *Current in a Mott-Diode*
In class, I derived the current density in a Schottky-diode of barrier height $q\Phi_B$ to be

$$J = J_0[\exp(qV_a / kT) - 1].$$

I mentioned that the constant J_0 is given by $J_0 = A^* T^2 \exp(-q\Phi_B / kT)$, where

$$A^* = \frac{4\pi q m^* k_B^2}{h^3} \approx 120\left(\frac{m^*}{m_0}\right)\frac{A}{cm^2 K}$$

is the effective Richardson's constant. You will now verify this result.

a) Derive this result assuming that the current is ENTIRELY due to thermionic-emission. You might need to read up some semiconductor devices textbook for doing that.

Answer the following *qualitatively* with help of sketches -

b) The derivation holds for *both* a Schottky and a Mott-diode – why?
c) What would happen to the current-voltage characteristic of the Schottky diodes if I shine light with photon energy larger than semiconductor bandgap?

Problem 2: *MOSFET Design (Simple problem for practice-yes, it is THAT easy!)*
An n-channel MOSFET has a W/L=5, a SiO_2 layer thickness t_{OX}=20nm, and electron mobility μ_n=600cm^2/Vs. You are to use it as a *controlled resistor*. Remember that the MOSFET has a normally OFF channel, which is opened when the gate voltage (V_G) is larger than a threshold voltage (V_T).

a) Sketch a figure of the MOSFET structure with labels of layers, doping, etc.
b) Calculate the free-electron sheet density in the channel Q_n/q required for the MOSFET channel resistance to be R=500Ω in the linear regime of MOSFET operation (i.e., low V_{DS}).
c) Using long-channel theory, find the excess gate voltage (i.e., V_G-V_T) required to produce the desired resistance under conditions of part b).

Problem 3: Survey of *ITRS* – the road trip…
The future of the semiconductor industry (chip, memory, electronic component manufacturers) is guided by a (or THE!) roadmap – the so called **I**nternational **T**echnology **R**oadmap for **S**emiconductors (*ITRS*). Your job in this problem is to assemble your own version of Moore's law – (futuristic) predictions of the path along which the semiconductor (& solid-state devices) industry is headed.

You are to collect data for your own use later – plot the recent past (starting late 90s), current, and projected values for MOSFET (or CMOS) scaling – a) gate lengths, b) gate oxide thicknesses, c) packing densities, d) supply voltages (V_{DD}), e) threshold voltages, f) doping densities, g) speeds, h) static and i) dynamic power dissipation for each *node* (3 or 2-year cycle). Write a small paragraph on any additional information (such as major international players, problems/hindrances ahead with interconnects, lithography, solutions, new and emerging technologies etc) that you find interesting. Make generous use of resources available on the web – the ITRS website at http://public.itrs.net is a good start. Use other websites (such as Intel, IBM, TSMC etc) and of course Google to put together your graphs and paragraphs. This could be time-consuming, but I want you to get introduced to the real world of solid state devices based on silicon by this exercise.

p.s. This question seems straight out of a business school final exam!