EE566 Solid State Devices

Spring 2004
Dept of Electrical Engineering
University of Notre Dame
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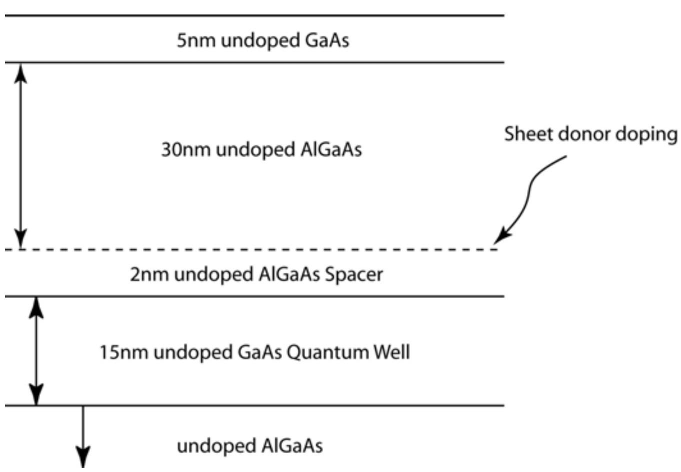
Assignment 10
Posted: 04/18/2004
Due: 04/26/2004

MESFETs, HEMTs, and MOSFETs

Problem 1: *MESFETs – 2-dimensional problem*
Derive and plot the two-dimensional potential profile in the depletion region under the gate of a MESFET with zero gate voltage, and drain-source bias high enough that the current I_{ds} is saturated. Plot the electric field and potential along the channel. Assume the MESFET channel to be long, such that gradual channel approximation holds near the source end. Explain everything you assume in the derivation. (Read and use the Grebene and Ghandhi paper).

Problem 2: *HEMTs – Design your own structure*
Consider the AlGaAs/GaAs (ΔE_C=0.25eV) HEMT layer structure shown. Assume that surface states pin the GaAs surface Fermi level 1eV below the conduction band. I require the sheet –density of the channel to be $n_s=10^{12}/cm^2$.

a) *Calculate* the sheet doping in the donor layer required to achieve that. Clearly draw the charge, field, and band diagrams. Verify with 1D Poisson. Note that the quantum well is triangular in shape.
b) Calculate the g_m vs V_{gs} curve for the HEMT, assuming v_{sat}(GaAs)=10^7cm/s, v_{sat}(AlGaAs)=2×10^6cm/s, gate length to be short, and V_{ds} is high, such that the saturated velocity model holds. Make any simplifying assumptions you think reasonable. Calculate the threshold voltage V_{th} required to deplete the channel.
c) Now, I want the quantum well to be flat instead of triangular. Design that for me.
d) Why would anyone need a flat quantum well? Are there any disadvantages?



Problem 3: *MOS – Capacitor*
This problem is of utmost importance in understanding MOS capacitance-voltage behavior, as well as DRAM operation. Consider that a MOS system on p-type silicon (doping N_A) is biased to deep depletion by the sudden deposition of a total charge Q_G on the gate at time $t=0$. Carrier generation in the space-charge region at the silicon surface results in a charging current for the channel charge Q_n according to the net generation rate equation $J_G=qn_ix_i/2\tau_0$, where x_i is the depletion region width, n_i the intrinsic carrier density, and τ_0 is the minority carrier (electron) lifetime (we have covered generation currents in class). This allows us to write

$$\frac{dQ_n}{dt} = -\frac{qn_i(x_d - x_{df})}{2\tau_0},$$

where x_d is the (time-dependent) depletion-region width at the surface, and x_{df} is the space-charge region width when thermal equilibrium is reached, i.e., when $x_d=x_{df}$ is reached, channel charging by generation goes to zero. (contd…)

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a) Show that the time evolution of Q_n is governed by the differential equation

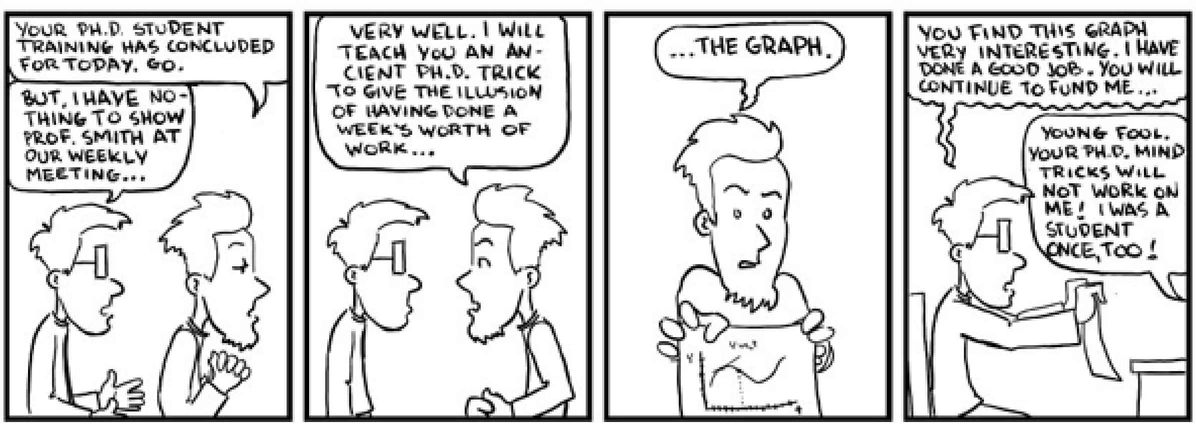
$$Q_n + \left(\frac{2\tau_0 N_A}{n_i}\right)\frac{dQ_n}{dt} = -[Q_G - qN_A x_{df}]$$

b) Solve this equation subject to $Q_n(t=0) = 0$, and thus show that the characteristic charging time required to form an inversion layer is of the order $T \sim \tau_0 \times (2N_A / n_i)$. Estimate this charging time for an acceptor doping $N_A=10^{15}/cm^3$. Can you explain why MOS capacitors are the building blocks of DRAMs from this example?

Problem 4: *MOSFETs – Currents*
Consider a MOSFET biased in *strong inversion* in the *linear* region.

a) Find expressions for the diffusion current $I_{diff}(x)$ and drift current $I_{drift}(x)$ at any point x along the channel.
b) Which current component dominates?

That's it! No more assignments!



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