

Microwave Performance of GaAs MOSFET With Wet Thermally Oxidized InAlP Gate Dielectric

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Abstract—This paper reports the first demonstration of a microwave-frequency operation of a GaAs MOSFET fabricated using a wet thermal oxidation of InAlP lattice-matched to GaAs to form a native-oxide gate insulator. Devices with 1- μm gate lengths exhibit a cutoff frequency (f_t) of 13.7 GHz and a maximum frequency of oscillation (f_{max}) of 37.6 GHz, as well as a peak extrinsic transconductance of 73.6 mS/mm. A low-leakage current density of 3.8×10^{-3} A/cm² at 1-V bias for an MOS capacitor demonstrates the good insulating properties of the \sim 11-nm thick native gate oxide.

Index Terms—Gallium arsenide, InAlP native oxide, microwave FETs, MOSFETs, oxidation.

I. INTRODUCTION

DUE TO THE wide array of high-electron mobility alloys of varying bandgaps that can be epitaxially grown on its surface and the availability of semi-insulating substrates, GaAs remains one of the most widely used semiconductors for high-speed optoelectronic applications and wireless communication systems. While Schottky gates are commonly used in high-speed GaAs-based transistors, the restricted forward bias (a few tenths of a volt) that can be applied without excessive gate leakage currents limits their power handling capability. A MISFET has the advantages over a Schottky-gate device that it can be operated with higher positive or negative voltages applied to its gate with very low-gate leakage current and that its input impedance can be extremely high, being essentially that of the insulator.

Since the electrical characteristics of native oxides of GaAs are far inferior to those of SiO₂ on Si, alternative insulators have long been pursued, including SiO₂ [1], SiON [2], Al₂O₃ [3], CaF₂ [4], GaS [5], P₃N₅ [6], and others [7], [8] to enable the preferred metal–insulator–semiconductor gate structure. In recent years, many deposited insulator/GaAs structures have been investigated, with a few yielding promising results [9]–[13]. Native-oxide films on GaAs can offer advantages of processing convenience and low cost. Wet thermal oxides of AlGaAs [14] have been studied but found to suffer from midgap traps caused by residual interfacial As [15]. These traps lead to increased interface recombination velocity [16], [17] and high-leakage currents [18], [19]. However, the wet thermal oxides of As-free In_{0.5}Al_{0.5}P (lattice matched to GaAs) have been found to

Manuscript received December 15, 2005; revised February 13, 2006. This work was supported by the Air Force Office of Scientific Research under Grant No. AF-F49620-01-1-0331. The review of this letter was arranged by Editor J. del Alamo.

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Digital Object Identifier 10.1109/LED.2006.872898

possess excellent insulating [20]–[22] and interfacial properties [21], [23] and may provide a viable native oxide for III–V MOS devices. In this letter, we present the first demonstration of the microwave-frequency operation of a GaAs-based MOSFET using a native dielectric gate insulator formed through thermal oxidation. Record peak extrinsic transconductance for a native-oxide gate insulator GaAs channel MOSFET is reported.

II. DEVICE STRUCTURE AND FABRICATION

GaAs MOSFETs using an InAlP native oxide as the gate insulator are fabricated on a metal–organic chemical vapor deposition (MOCVD)-grown heterostructure [24] consisting of a GaAs buffer layer grown first on a semi-insulating GaAs substrate, followed by a 100-nm Si-doped GaAs channel layer ($N_d \sim 1 - 2 \times 10^{17}$ cm⁻³), a 4-nm undoped In_{0.5}Ga_{0.5}P oxidation stop layer, 15.7 nm of Si-doped ($N_d \sim 1 \times 10^{18}$ cm⁻³) In_{0.5}Al_{0.5}P lattice matched to GaAs and a 50-nm heavily Si-doped GaAs cap layer ($N_d > 2 \times 10^{18}$ cm⁻³).

Mesas for a device isolation are defined by an optical lithography and formed with several wet-etching steps. The GaAs cap and channel layers are etched by selective wet etching in a citric acid and hydrogen peroxide solution, and the InAlP and InGaP epilayers are etched using HCl. The gate regions of the MOSFETs are defined using the optical lithography, with the GaAs cap layer in the gate region selectively removed in a citric acid/hydrogen peroxide solution to expose the gate region for an oxidation step carried out at 440 °C for 30 min in water vapor. Details of the oxidation process have been published in [22]. The InAlP native-oxide thickness, measured via transmission electron microscopy (not shown), is 10.5 nm, with 5.3 nm of unoxidized InAlP remaining.

After oxidation, source and drain regions are defined and formed by thermal evaporation of AuGe (88% Au, 12% Ge)/Ni/Au, followed by rapid thermal annealing (optimized by utilizing the transmission line method) at 400 °C for 20 s in a nitrogen ambient. Cr/Au metal gates are deposited using thermal evaporation and liftoff.

III. RESULTS AND DISCUSSION

The fabricated 50 \times 2 (a unit gate width of 50 μm and two gate fingers) MOSFETs with a 1- μm gate length are characterized by measuring both the dc and microwave-frequency performance. As shown in Fig. 1, the typical drain-source saturation current (I_{ds}) of the fabricated devices is 12 mA (120 mA/mm). A transfer characteristic is shown in Fig. 2, with a maximum extrinsic transconductance ($g_{m,\text{max}}$) of 73.6 mS/mm measured

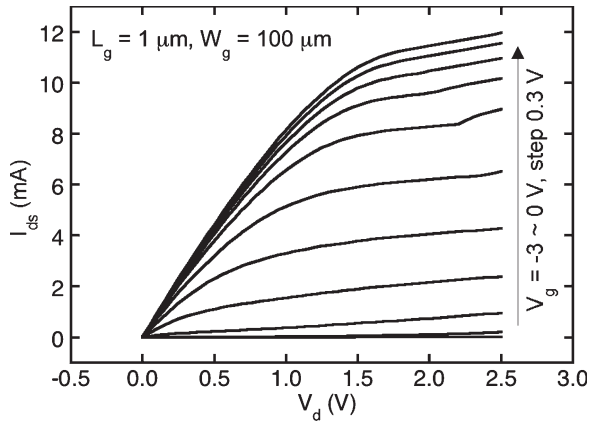


Fig. 1. Drain current as a function of drain voltage measured for a 50×2 (a unit gate width of $50 \mu\text{m}$ and two gate fingers), $1\text{-}\mu\text{m}$ gate length InAlP native-oxide GaAs MOSFET.

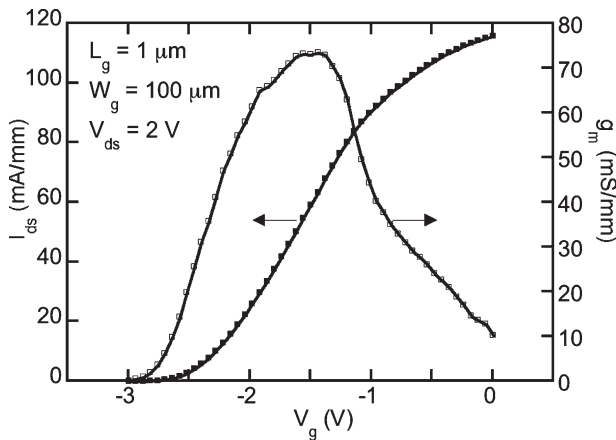


Fig. 2. Drain current I_{ds} and extrinsic transconductance g_m plotted versus gate bias voltage V_g for a $1\text{-}\mu\text{m}$ gate length InAlP native-oxide GaAs MOSFET biased in the saturation region at $V_{ds} = 2\text{ V}$.

at a drain voltage (V_{ds}) of 2 V and a gate voltage (V_{gs}) of -1.44 V . The dc characteristics of the $1\text{-}\mu\text{m}$ gate length device show a clear pinchoff and channel modulation with depletion-mode operation. The use here of local oxidation in the gate region, which allows the source and drain ohmic contacts to be placed atop the heavily doped GaAs cap layer/unoxidized InAlP, provides a substantial improvement in the channel access resistance over that in [26]. The measured current–voltage (I – V) characteristics are observed to be stable, and the device performance repeatable even after several months.

Microwave-frequency measurements are performed ON-wafer over the frequency range of 1–35 GHz. Shown in Fig. 3 are both the current gain h_{21} and maximum available gain (MAG) versus frequency from which are obtained a cutoff frequency (f_t) of 13.7 GHz, and a maximum frequency of oscillation (f_{max}) of 37.6 GHz. This microwave-frequency performance is comparable to that of other recently reported depletion-mode GaAs MOSFETs with similar gate lengths fabricated using an in situ deposited Ga_2O_3 (Gd_2O_3) gate dielectric layer [9] or an atomic layer deposited (ALD) Al_2O_3 gate dielectric layer [25].

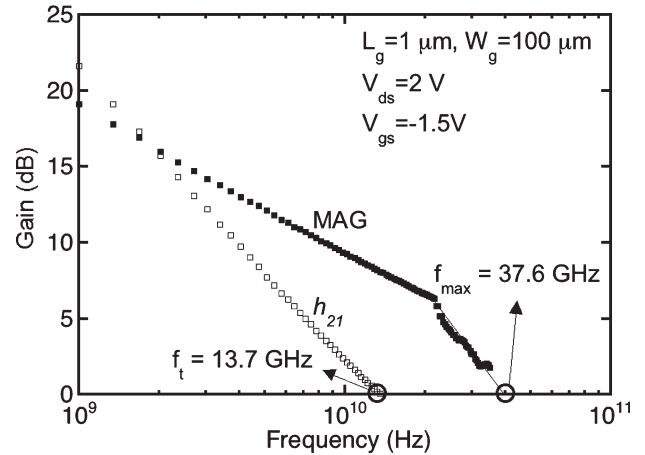


Fig. 3. Current gain h_{21} and MAG versus frequency measured for a $1\text{-}\mu\text{m}$ gate length InAlP native-oxide GaAs MOSFET with f_{max} and f_t estimated from the extrapolated data.

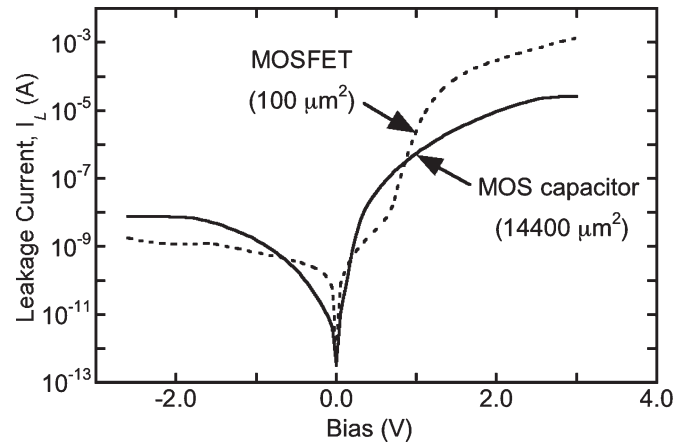


Fig. 4. Typical gate leakage current characteristics for InAlP native-oxide GaAs MOSFET and MOS capacitor devices. The gate area of the MOSFET is $100 \mu\text{m}^2$, and the top plate area of the MOS capacitor is $14400 \mu\text{m}^2$. For comparison with the MOS capacitor, the MOSFET is measured with $V_{ds} = 0\text{ V}$.

The InAlP native-oxide MOS device gate leakage characteristics are also measured. Fig. 4 shows the typical gate leakage current of an MOSFET ($1\text{-}\mu\text{m}$ gate length, $100 \mu\text{m}^2$ gate area) and an MOS capacitor ($14400 \mu\text{m}^2$ electrode area) fabricated on the same heterostructure using identical oxidation and metallization processes. A leakage current density of $3.8 \times 10^{-3}\text{ A/cm}^2$ at 1-V bias for the MOS capacitor demonstrates the good insulating properties of the InAlP native oxide. As in [26], the lower leakage current density of the MOS capacitors relative to the MOSFETs indicates a parasitic leakage path present where the gate metallization runs over the etched mesa edges of the FET structures. The gate leakage for the FET devices is reduced by a factor of 1200 in this paper, dropping at a 1-V bias from $3 \times 10^{-3}\text{ A}$ for the comparable 11-nm thick oxide of [26] to $2.5 \times 10^{-6}\text{ A}$ here, possibly due to improved mesa sidewall etching. Alternative device isolation processes such as use of an ion implantation can be employed to further reduce the gate leakage current in FET devices. Typical OFF-state gate-drain breakdown voltages of 11.5 V are measured on $1\text{-}\mu\text{m}$ gate length devices at a gate current density of 1 mA/mm.

Comparing to a Schottky-gate device, the gate leakage of Fig. 4 is much lower than the 2.5 A/cm^2 reverse saturation gate current of typical GaAs-based HEMTs fabricated in our lab.

IV. CONCLUSION

The microwave-frequency operation of GaAs-based MOSFETs using InAlP oxide as the gate insulator are reported for the first time, showing a cutoff frequency of 13.7 GHz and a maximum frequency of oscillation of 37.6 GHz. A low gate leakage current of $2.5 \mu\text{A}$ ($25 \mu\text{A/mm}$) at $+1\text{-V}$ bias is observed. The extrinsic transconductance of these $1\text{-}\mu\text{m}$ gate length devices exhibits a peak of 73.6 mS/mm . These results indicate that the wet thermal native oxide of InAlP lattice matched to GaAs is a potentially viable gate insulator for high-speed, high-power MIS devices.

REFERENCES

- [1] H. Becke, R. Hall, and J. White, "Gallium arsenide MOS transistors," *Solid State Electron.*, vol. 8, no. 10, pp. 813–818, 1965.
- [2] L. Messick, "GaAs-Si_xO_yN_z MISFET," *J. Appl. Phys.*, vol. 47, no. 12, pp. 5474–5475, Dec. 1976.
- [3] S. Yokoyama, K. Yukitomo, M. Hirose, Y. Osaka, A. Fischer, and K. Ploog, "GaAs MOS structures with Al₂O₃ grown by molecular-beam reaction," *Surf. Sci.*, vol. 86, pp. 835–840, Jul. 1979.
- [4] T. Waho and F. Yanagawa, "A GaAs MISFET using an MBE-grown CaF₂ gate insulator layer," *IEEE Electron Device Lett.*, vol. 9, no. 10, pp. 548–549, Oct. 1988.
- [5] P. P. Jenkins, A. N. Macinnes, M. Tabibazar, and A. R. Barron, "Gallium-arsenide transistors—Realization through a molecularly designed insulator," *Science*, vol. 263, no. 5154, pp. 1751–1753, Mar. 1994.
- [6] Y. H. Jeong, K. H. Choi, and S. K. Jo, "Sulfide treated GaAs MISFETs with gate insulator of photo-CVD grown P₃N₅ film," *IEEE Electron Device Lett.*, vol. 15, no. 7, pp. 251–253, Jul. 1994.
- [7] T. Mimura and M. Fukuta, "Status of the GaAs metal–oxide–semiconductor technology," *IEEE Trans. Electron Devices*, vol. ED-27, no. 6, pp. 1147–1155, Jun. 1980.
- [8] C. W. Wilmsen, *Physics and Chemistry of III–V Compound Semiconductor Interfaces*. New York: Plenum, 1985.
- [9] Y. C. Wang, M. Hong, J. M. Kuo, J. P. Mannaerts, J. Kwo, H. S. Tsai, J. J. Krajewski, Y. K. Chen, and A. Y. Cho, "Demonstration of submicron depletion-mode GaAs MOSFET's with negligible drain current drift and hysteresis," *IEEE Electron Device Lett.*, vol. 20, no. 9, pp. 457–459, Sep. 1999.
- [10] M. Passlack, J. K. Abrokwha, R. Droopad, Z. Y. Yu, C. Overgaard, S. I. Yi, M. Hale, J. Sexton, and A. C. Kummel, "Self-aligned GaAs p-channel enhancement mode MOS heterostructure field-effect transistor," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 508–510, Sep. 2002.
- [11] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H. J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, "GaAs with nanometer-thin dielectric grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 83, no. 1, pp. 180–182, Jul. 2003.
- [12] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H. J. L. Gossmann, M. Hong, K. K. Ng, and J. Bude, "Depletion-mode InGaAs with oxide gate dielectric grown by atomic-layer deposition," *Appl. Phys. Lett.*, vol. 84, no. 3, pp. 434–436, Jan. 2004.
- [13] M. Passlack, N. Medendorp, S. Zollner, R. Gregory, and D. Braddock, "Optical and electrical properties of amorphous Gd_xGa_{0.4-x}O_{0.6} films in Gd_xGa_{0.4-x}O_{0.6}/Ga₂O₃ gate dielectric stacks on GaAs," *Appl. Phys. Lett.*, vol. 84, no. 14, pp. 2521–2523, Apr. 2004.
- [14] J. M. Dallesasse, N. Holonyak, Jr., A. R. Sugg, T. A. Richard, and N. El-Zein, "Hydrolyzation oxidation of Al_xGa_{1-x}As-AlAs-GaAs quantum well heterostructures and superlattices," *Appl. Phys. Lett.*, vol. 57, no. 26, pp. 2844–2846, Dec. 1990.
- [15] P. Parikh, "Oxide based electronics on gallium arsenide," Ph.D. dissertation, Dept. of Elect. Comput. Eng., Univ. California, Santa Barbara, 1998.
- [16] S. S. Shi, E. L. Hu, J. P. Zhang, Y. I. Chang, P. Parikh, and U. Mishra, "Photoluminescence study of hydrogenated aluminum oxide–semiconductor interface," *Appl. Phys. Lett.*, vol. 70, no. 10, pp. 1293–1295, Mar. 1997.
- [17] M. R. Islam, R. D. Dupuis, A. P. Curtis, and G. E. Stillman, "Effects of thermally grown native oxides on the luminescence properties of compound semiconductors," *Appl. Phys. Lett.*, vol. 69, no. 7, pp. 946–948, Aug. 1996.
- [18] C. I. H. Ashby, J. P. Sullivan, P. P. Newcomer, N. A. Missert, H. Q. Hou, B. E. Hammons, M. J. Hafich, and A. G. Baca, "Wet oxidation of Al_xGa_{1-x}As: Temporal evolution of composition and microstructure and the implications for metal–insulator–semiconductor applications," *Appl. Phys. Lett.*, vol. 70, no. 18, pp. 2443–2445, May 1997.
- [19] E. I. Chen, N. Holonyak, Jr., and S. A. Maranowski, "Al_xGa_{1-x}As-GaAs metal–oxide–semiconductor field-effect transistors formed by lateral water vapor oxidation of AlAs," *Appl. Phys. Lett.*, vol. 66, no. 20, pp. 2688–2690, May 1995.
- [20] A. L. Holmes, "Compound semiconductor native oxide-based technologies for optical and electrical devices grown on GaAs substrates using MOCVD," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. Texas, Austin, 1999.
- [21] P. J. Barrios, D. C. Hall, G. L. Snider, T. H. Kosel, U. Chowdhury, and R. D. Dupuis, "Electrical properties of InAlP native oxides for GaAs-based MOS applications," in *Proc. SOTAPCO XXXIV, Electrochem. Soc.*, 2001, vol. 2001-1, pp. 258–264.
- [22] Y. Cao, J. Zhang, X. Li, T. H. Kosel, P. Fay, D. C. Hall, X. B. Zhang, R. D. Dupuis, J. B. Jasinski, and Z. Liliental-Weber, "Electrical properties of InAlP native oxides for metal–oxide–semiconductor device applications," *Appl. Phys. Lett.*, vol. 86, no. 6, pp. 0621051–0621053, 2005.
- [23] X. Li, Y. Cao, D. C. Hall, P. Fay, X. Zhang, and R. D. Dupuis, "Electrical characterization of native-oxide InAlP/GaAs metal–oxide–semiconductor heterostructures using impedance spectroscopy," *J. Appl. Phys.*, vol. 95, no. 8, pp. 4209–4212, Apr. 2004.
- [24] Heterostructure grown using LP-MOCVD by Epiworks, Inc., Champaign, IL.
- [25] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H. J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergeant, M. Hong, K. K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 209–211, Apr. 2003.
- [26] X. Li, Y. Cao, D. C. Hall, P. Fay, B. Han, A. Wibowo, and N. Pan, "GaAs MOSFET using InAlP native oxide as gate dielectric," *IEEE Electron Device Lett.*, vol. 25, no. 12, pp. 772–774, Dec. 2004.