Electrical properties of InAlP native oxides for metal–oxide–semiconductor device applications

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Data are presented on the insulating properties and capacitance–voltage characteristics of metal–oxide–semiconductor (MOS) device-thickness (below ~100 nm) native oxides formed by wet thermal oxidation of thin InAlP epilayers lattice matched to GaAs. Low leakage current densities of $J=1.4\times10^{-9}$ A/cm^2 and $J=8.7\times10^{-11}$ A/cm^2 are observed at an applied field of 1 MV/cm for MOS capacitors fabricated with 17 and 48 nm oxides, respectively. Transmission electron microscopy images show that the In-rich interfacial particles which exist in 110 nm oxides are absent in 17 nm oxide films. Quasistatic capacitance–voltage measurements of MOS capacitors fabricated on both *n*-type and *p*-type GaAs show that the InAlP oxide–GaAs interface is sufficiently free of traps to support inversion, indicating an unpinned Fermi level. These data suggest that InAlP native oxides may be a viable insulator for GaAs MOS device applications. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1861981]

Due to the wide array of high electron mobility alloys of varying band gaps that can be epitaxially grown on its surface, GaAs remains the most widely used semiconductor for high-speed electronic applications. While Schottky gates are commonly used in high-speed GaAs transistors, the restricted forward bias (a few tenths of a volt) that can be applied without excessive gate leakage currents limits their power handling capability. The electrical characteristics of native oxides of GaAs are far inferior to those of SiO_2 on Si, and an alternative insulator has long been pursued[1,2] to enable the preferred metal–insulator–semiconductor gate structure. Many deposited insulator/ GaAs structures have been investigated, although only a few have yielded promising results.[3–6] Native oxide films on GaAs can offer advantages of processing convenience and low cost. Wet thermal oxides of AlGaAs[7] have been studied but found to suffer from midgap traps caused by residual interfacial As.[8] These traps lead to increased interface recombination velocity[9,10] and high leakage currents.[11] However, the wet thermal oxides of *As-free* $In_{0.5}(Al_xGa_{1-x})_{0.5}P$ (lattice matched to GaAs)[10,12–21] have been found to possess excellent insulating[13,17,18] and interfacial properties[10,15,17,20] and may provide a viable native oxide for III–V metal–oxide–semiconductor (MOS) devices.[21]

In this letter, we report on the detailed electrical properties and microstructure of $In_{0.485}Al_{0.515}P$ native oxides scaled to reduced thicknesses more suitable for MOS device applications than the 110 nm oxides reported previously.[17,20] Current–voltage ($I-V$) measurements on MOS capacitors fabricated with oxides formed from thin InAlP epilayers show very low leakage current densities while capacitance–voltage ($C-V$) measurements indicate that the thin oxides support inversion. Transmission electron microscopy (TEM) images elucidate the microstructure of the InAlP native oxide of different thicknesses. We have elsewhere demonstrated a GaAs-based MOS field effect transistor using a thin (~10 nm) native oxide of $In_{0.485}Al_{0.515}P$ as the gate insulator.[21]

Samples are grown by metalorganic chemical vapor deposition. *N*-type heterostructures grown on Si-doped (2×10^{18} cm^{-3}) GaAs substrates consist of 500 nm of Si-doped (~10^{16} cm^{-3}) GaAs, an undoped $In_{0.485}Al_{0.515}P$ layer with one of three different thicknesses (63, 31, or 15 nm), and a 50-nm-thick undoped GaAs cap layer. The *p*-type heterostructures are grown on semi-insulating GaAs substrates, and consist of 1000 and 500 nm C-doped GaAs layers (2×10^{18} and 1×10^{17} cm^{-3}, respectively), an undoped $In_{0.485}Al_{0.515}P$ layer (63, 31, or 15 nm), and a 50 nm undoped GaAs cap layer.

The GaAs cap layers are removed by a 4:1 citric acid: 30% H_2O_2 selective etch before samples are thermally oxidized at 500 °C from the surface in a 2-in.-diam quartz tube furnace with 0.68 l/min of UHP N_2 bubbled through 95 °C H_2O. The 63, 31, and 15 nm InAlP layers are fully oxidized and expand upon oxidation (for 65, 30, and 15 min, respectively) to corresponding oxide thicknesses (obtained from TEM images) of 110±1.6, 48±1.7, and 17±1.1 nm, respectively. Variable-angle spectroscopic ellipsometry measurements show that the InAlP oxide has a real refractive index of ~1.58 for the wavelength range from 600 to 1700 nm and negligible absorption (imaginary index $k\leq10^{-3}$) with an onset of absorption below 600 nm indicating a band gap for the oxide (from a Tauc plot[22]) of ≥4.0 eV.[19]

MOS structures are fabricated by the evaporation of Cr/Au gate electrodes onto the oxide surface. $I-V$ measure-

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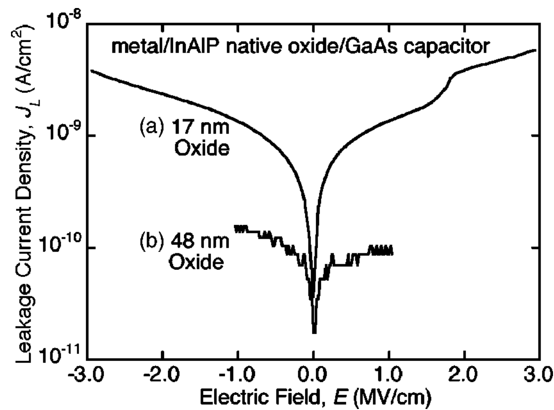

FIG. 1. Typical current density vs electric field curves for MOS capacitors with (a) 17-nm- and (b) 48-nm-thick InAlP native oxide films on *n*-type GaAs substrates. The capacitor contact area $A = 5.8 \times 10^{-4}$ cm^2. Sweep rate is 10 mV/s.

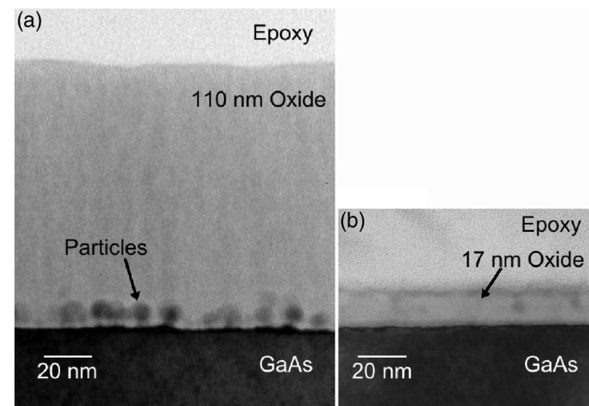

FIG. 2. Comparison of bright field TEM images of (a) 110-nm- and (b) 17-nm-thick InAlP wet thermal native oxide films. The particles clearly visible in (a) are not present anywhere in sample (b).

ments are carried out using an Agilent 4156C semiconductor parameter analyzer. Quasistatic and high-frequency (100 kHz) $C-V$ measurements are performed using a Keithley model 82 $C-V$ measurement system. All measurements are done at room temperature in a shielded probe station. All capacitors have a contact area of 240 μm $\times$ 240 μm (5.8×10^{-4} cm^2). TEM cross-sectional specimens were prepared by standard methods of mechanical prethinning (with dimple grinding or wedge polishing) followed by 2 kV Ar-ion milling.

Figure 1 shows leakage current density versus electric field for MOS capacitors fabricated with (a) 17 nm and (b) 48 nm oxide films on *n*-type GaAs. The jaggedness appearing in (b) results from the 10 fA resolution of the measurement instrumentation. The electric field is obtained by dividing the applied voltage by the measured oxide thickness. At a field of 1 MV/cm, the measured leakage current densities are 1.4×10^{-9} A/cm^2 for the 17 nm oxide and 8.7 $\times 10^{-11}$ A/cm^2 for the 48 nm oxide. Breakdown fields for all InAlP native oxides in this letter are in the 3–6 MV/cm range. Table I lists a comparison of these leakage current density and breakdown field results with other native and deposited oxides on GaAs. At the same field strength, the 48 nm InAlP oxide of Fig. 1(b) exhibits more than one order of magnitude less leakage than the 64 nm $Gd_{0.31}Ga_{0.1}O_{0.59}/Ga_2O_3$ dielectric stack of Ref. 6. Compared to other candidate insulator/ GaAs structures, InAlP native oxides clearly possess the excellent insulating properties needed for MOS device applications.

TABLE I. Comparison of the leakage current densities, J_L, at applied field of 1 MV/cm (except as noted) and breakdown fields, E_B, for various deposited and native oxide insulators and thicknesses, d, on GaAs. All devices are MOS capacitors except as noted.

Insulator	d(nm)	J_L(A/cm^2)	E_B(MV/cm)	Ref.
$Ga_2O_3(As_2O_3)$[a]	30	1.2×10^{-4}	5.3	25
$Gd_{0.31}Ga_{0.1}O_{0.59}/Ga_2O_3$	64	1×10^{-9}	3.5	6
Al_2O_3	8	9×10^{-8}	5	4
InAlP oxide	110	9×10^{-11}[b]	6.3	17
Al_2O_3[a]	16	$<10^{-4}$[c]	[d]	5
AlGaAs oxide	45	4.9×10^{-7}	3.8	26
$Ga_2O_3(As_2O_3)$	65	2×10^{-7}	4.7	27
InAlP oxide	48	8.7×10^{-11}	3–6	This work
InAlP oxide	17	1.4×10^{-9}	3–6	This work

[a]MOSFET.
[b]Maximum measurement voltage of 5 V(0.45 MV/cm).
[c]Range reported for voltages <3 V(<1.88 MV/cm).
[d]Not reported.

As shown in the bright-field TEM images of Fig. 2, dark particles exist near the oxide/ GaAs interface in the 110 nm oxide of Fig. 2(a), while no dark interfacial particles appear in the 17 nm oxide of Fig. 2(b). Such particles were also evident in TEM images of >100 nm oxides of $In_{0.5}(Al_{0.9}Ga_{0.1})_{0.5}P$ grown at 500–550 °C.[12] Figure 2(b) is representative of the entire observable area for this and a second wedge-polished cross section specimen, with the absence of particles also confirmed for plan-view specimens (not shown) in which possible loss of particles due to ion milling and electron beam interactions is suppressed by the fact that they are protected from the vacuum by the substrate and overlying oxide film. The interfacial particles in Fig. 2(a) are believed to be indium rich based on Z-contrast TEM images[19] and secondary ion mass spectrometry[12] and Auger depth profiling.[18] The size of the particles increases with the progressive consumption of the InAlP epilayer during oxidation.[19] We hypothesize that In, the heaviest element in the structure, outdiffuses more slowly than the other alloy constituents and hence accumulates near the interface during oxide growth, forming In-rich particles.

Figure 3 shows 100 kHz high-frequency (CH) and quasistatic (CQ) $C-V$ measurements for the 17 nm oxides on both *n*-type and *p*-type GaAs under standard microscope illumination as is required for wide band gap semiconductors due to the low thermal generation rate of electron–hole pairs.[23] The clear existence of three operational regimes—accumulation, depletion, and inversion—of these MOS structures for both *n*- and *p*-type samples indicates that the Fermi level is unpinned. Thicker oxides (48 and 110 nm) on both types of GaAs also show similar unpinned behavior (not shown). The frequency dispersion (offset between CQ and CH curves in accumulation) seen in Fig. 3 is commonly observed[2,23,24] in III–V MOS structures. While possibly attributable to a low resistivity interfacial region of the oxide which reduces the effective oxide thickness and thus increases the apparent capacitance at low measurement frequencies (Maxwell–Wagner effect[23]), it is in general not well understood. Using bias-dependent swept-frequency impedance spectroscopy, a total interface state density of 8

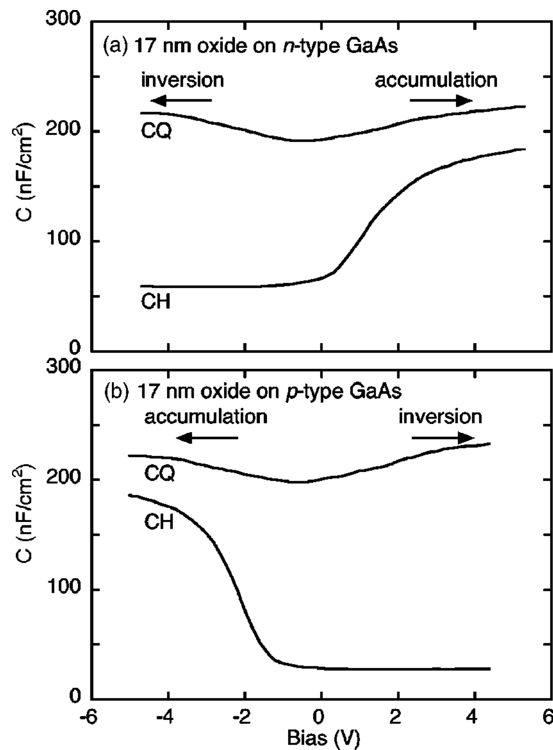

FIG. 3. High-frequency (CH, 100 kHz) and quasistatic (CQ) capacitance–voltage measurements for 17 nm native oxide of InAlP on (a) *n*-type and (b) *p*-type GaAs. Sweep rate is 50 mV/s. CQ data show inversion for both carrier types, indicating an unpinned Fermi level.

$\times 10^{11}$ cm^{-2} has previously been found for the 110 nm oxide on *n*-type GaAs.[20] The absence of particles in the interfacial region of the 17 nm oxide shown in Fig. 2(b) may lead to a still lower interface state density for thinner InAlP oxide films.

In summary, with their excellent insulating properties and unpinned Fermi level, the native oxides of InAlP show promise for the gate dielectric in GaAs MOS device applications. Interfacial particles observed for thicker InAlP oxide films are not present in the thinner 17 nm oxide films, and leakage current densities are lower at equivalent field strength than the best reported results for comparable deposited oxide films. Wet thermal growth of InAlP native oxide films potentially offers a simpler, lower cost manufacturing technology for GaAs MOS devices.

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