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Electrical characterization of native-oxide InAlP/GaAs metal-oxide-semiconductor heterostructures using impedance spectroscopy

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InAlP native oxide/GaAs metal-oxide-semiconductor (MOS) capacitors have been characterized using bias- and temperature-dependent swept-frequency impedance spectroscopy. An equivalent circuit model has been developed for these MOS capacitors that accurately fits the measured impedance over the full frequency range from 40 Hz to 10 MHz. From the bias dependence of the circuit model parameters, the distribution in energy of the interface states was found to be consistent with an exponential distribution, with a total interface state density of 8×10^{11} cm^{-2} and an average activation energy of 0.34 eV below the conduction band edge. The temperature dependence of the impedance spectra was also examined, and an activation energy of 0.44 eV from the conduction band edge was determined, in good agreement with the bias-dependent impedance measurements. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1669078]

INTRODUCTION

III–V compound semiconductor metal-semiconductor field-effect transistors and high electron mobility transistors are widely used in mobile communication systems and high-speed optoelectronic circuits. In these transistors, a Schottky contact is used as the gate electrode. However the use of Schottky gates can lead to excessive gate leakage current and also restrict the forward gate bias to only a few tenths of a volt, leading to limited power handling capability in power amplifier applications. In addition, the modest Schottky barrier height between common gate metals and *III–V* compound semiconductors typically results in depletion-mode operation. This leads to a need for multiple power supply voltages and results in increased circuit complexity. An attractive alternative approach is the use of a metal-insulator-semiconductor (MIS) gate structure. The inclusion of an insulator layer between the gate metal and semiconductor channel permits a much larger gate voltage swing, while preserving a very low gate leakage current. Metal-insulator-semiconductor field-effect transistors (MISFETs) are also promising for realizing true enhancement-mode field-effect transistor operation, which provides the advantages of using a single power supply voltage and simultaneously reducing standby power consumption.

To realize these potential advantages, practical MISFETs require a gate insulator with a large band gap and a high-quality insulator/semiconductor interface for efficient channel modulation. Over the past several decades, many MIS structures on *III–V* materials have been examined. Although the electrical quality of the GaAs-based MIS structures demonstrated to date is not as good as those obtained from the more mature SiO_2/Si system, some of them have yielded promising results for electronic device applications. For example, MISFETs have been demonstrated with gate insulators of Ga_2O_3 grown by molecular beam epitaxy,[1] oxidized GaAs prepared by ultraviolet and ozone treatment,[2] Al_2O_3 grown by atomic layer deposition,[3] and wet-thermally oxidized AlGaAs.[4,5] Thermal oxidation has potential advantages for MISFET fabrication because it offers substantial flexibility in device heterostructure design and fabrication processing. Previous research has shown that the native oxide of $In_{0.49}Al_{0.51}P$ lattice-matched to GaAs has a much lower leakage current density and higher dielectric strength than that of oxidized AlGaAs,[6,7] making it attractive for device applications if the interface state density can be controlled. In this article, the suitability of InAlP native oxide on GaAs for device applications is examined by characterizing the interface state properties of InAlP native oxide/GaAs metal-oxide-semiconductor (MOS) capacitors using bias- and temperature-dependent variable-frequency impedance spectroscopy.

DEVICE FABRICATION AND CHARACTERIZATION

InAlP native oxide/GaAs MOS capacitors were fabricated on a heterostructure grown by metalorganic vapor phase epitaxy. The heterostructure was grown on a n^+ GaAs substrate, and consists of 500 nm of Si-doped GaAs (1×10^{17} cm^{-3}), 63 nm of undoped InAlP lattice-matched to GaAs, and a 50 nm thick undoped GaAs cap layer. The InAlP layer was wet-oxidized for 60 min at 500 °C immediately after removing the GaAs cap layer by selective wet etching in a citric acid and hydrogen peroxide solution. De-

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tails of the fabrication process have been published previously.[6] During oxidation, the InAlP oxide volume expands by a factor of about 1.8 to a final oxide thickness of 114.6 nm, as measured by variable-angle spectroscopic ellipsometry. Thermally evaporated Cr/Au films were used as both the gate metal on the oxide surface as well as the backside ohmic contact to the n^+ substrate. Capacitors with areas from 130×130 to $340\times340\ \mu\text{m}^2$ have been fabricated.

The current-voltage characteristics of the MOS capacitors were measured with an Agilent 4155B semiconductor parameter analyzer. A typical leakage current density of $8.6\times10^{-10}\ \text{A/cm}^2$ at 5 V bias was obtained for these devices, demonstrating the good insulating quality of the InAlP thermal oxide.

To assess the oxide-semiconductor interface quality, the impedance of capacitors with different areas was measured on-wafer from 40 Hz to 10 MHz as a function of applied direct-current (dc) bias. The measurements were calibrated using full on-wafer open/short/load compensation, and a test signal level of 20 mV root-mean-square was used for all measurements to ensure a small-signal linear response. All measurements were performed in a dark, light-tight probing chamber.

Measured susceptance and conductance versus frequency curves at four selected dc bias voltages are shown in Fig. 1 for a typical InAlP oxide/GaAs device. Both the susceptance and conductance have been divided by angular frequency to accentuate the substantial deviation from pure linear capacitive behavior observed over this frequency range. Similar dispersive characteristics have previously been reported by other researchers on several different insulator-compound semiconductor structures.[8]

To assist in the interpretation of the measured results, we have developed an equivalent circuit model which is an extension of the commonly used model for MOS capacitors.[9] This model, shown in Fig. 2, extends the conventional MOS capacitor model by including an additional parallel *RC* circuit to model the behavior of an interfacial layer and interface states between the oxide and the semiconductor. The existence of such an interfacial layer between the oxide and the semiconductor has been verified for the InAlP oxide/GaAs interface by the observation of an interfacial precipitate region using transmission electron microscopy (TEM).[6] In this extended model C_{ox} is the oxide capacitance, C_s is the capacitance of the interfacial region between the oxide and the GaAs, and C_{sc} and G_{sc} are the capacitance and conductance, respectively, of the space charge region inside the GaAs. C_{it} and G_{it} are the frequency-dependent capacitance and conductance, respectively, due to the interface states.[9] The broad spectral features that are observed in impedance spectra have been reported to originate from an interface state density that is continuously distributed over the bandgap.[9] For oxides on GaAs, the interface state distribution is expected to have a distribution that decays approximately exponentially with energy away from the band edge.[10] Assuming an interface state distribution of the form

$$N_{\text{it}}(E)=g e^{-a(E_c-E)/kT} \tag{1}$$

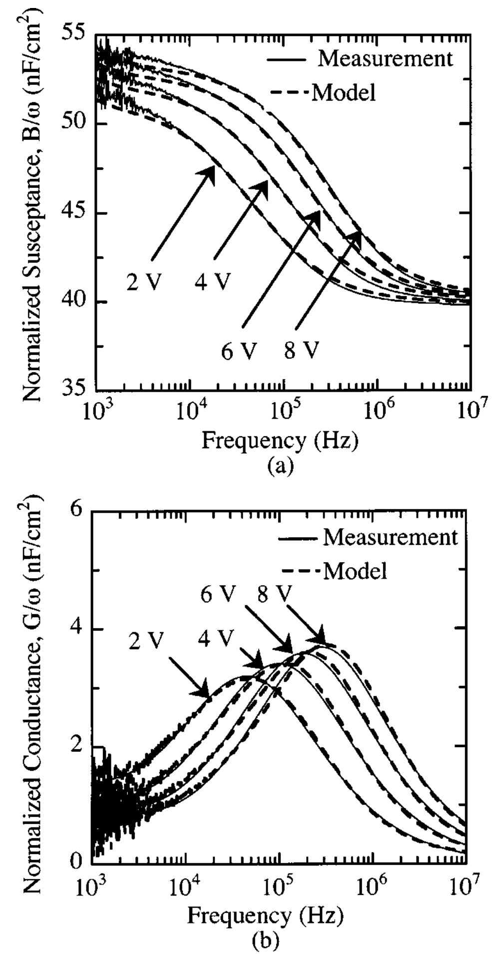

FIG. 1. Typical normalized measured and modeled susceptance and conductance vs frequency characteristics of an InAlP native oxide/GaAs MOS capacitor for several bias conditions at room temperature.

in the vicinity of the conduction band edge, one can show that the interface state capacitance and conductance in the equivalent circuit model are given by[11]

$$C_{\text{it}}=\frac{q}{\omega\tau_m}N_{\text{it}}(E_{\text{fn}})(1+\omega^2\tau_m^2)^{a/2}\tan^{-1}(\omega\tau_m), \tag{2}$$

$$\frac{G_{\text{it}}}{\omega}=\frac{q}{\omega\tau_m a}N_{\text{it}}(E_{\text{fn}})[(1+\omega^2\tau_m^2)^{a/2}-1], \tag{3}$$

where q is the electron charge, ω is angular frequency, and E_{fn} is the Fermi energy at the oxide/semiconductor interface. The capture time constant τ_m is given by $\tau_m=1/c_n n$, where c_n is the capture rate for electrons and n is the electron concentration at the oxide/semiconductor interface.

To find the circuit model parameters (and thus the interface state density and distribution parameters), the equivalent circuit shown in Fig. 2 combined with Eqs. (2) and (3) were fit to the measured impedance spectra using nonlinear least-squares curve fitting. The fits were performed with 33 bias voltages over the bias range of 0 to 8 V, covering depletion through accumulation of the oxide/GaAs interface. Good fits over the full frequency range and gate bias voltage range have been achieved, as shown in Fig. 1.

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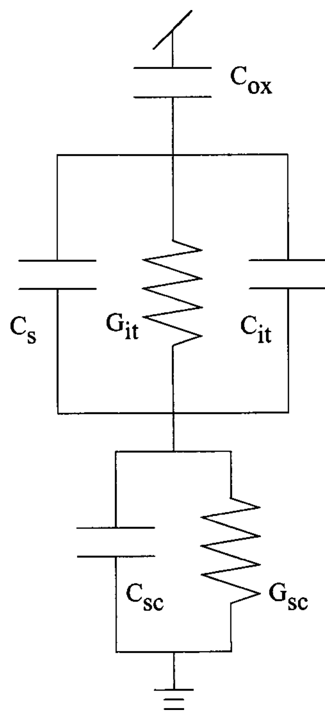

FIG. 2. Equivalent circuit including interfacial layer used to fit the measured electrical characteristics of InAlP native oxide/GaAs MOS capacitors.

Figure 3 shows the circuit model parameters C_{ox}, C_s, C_{sc}, and G_{sc}, obtained from the impedance spectra fitting as a function of bias voltage. C_{ox}, C_s, C_{sc}, and G_{sc} have been normalized with respect to capacitor area. As can be seen in Fig. 3, C_{ox} is constant throughout the voltage range as expected, and C_s is also nearly constant with bias voltage, indicating that the effective thickness of this interfacial layer is not bias dependent. Further, the large capacitance of C_s indicates it is a comparatively thin layer, consistent with TEM results.[6] Figures 3(c) and 3(d) show that both C_{sc} and G_{sc} increase when biased from depletion to accumulation as expected because of the decrease in the depletion layer thickness in the *n*-type GaAs. In addition, Fig. 3(b) shows that the capture time constant τ_m decreases when biased from depletion to accumulation due to the increase in the surface electron concentration, as expected. The interface-state distribution parameters g and a in Eqs. (1)–(3) are bias independent, with values of $6.1\times10^{12}\ \mathrm{cm}^{-2}$ and 0.196, respectively, determined from the fitting procedure. From Eq. (1) and the fitting parameters, the interface state density is computed by integrating $N_{\mathrm{it}}(E)$ over the band gap. The calculated total interface state density is $8\times10^{11}\ \mathrm{cm}^{-2}$, suggesting a relatively good oxide-semiconductor interface has been obtained. Since the interface states are distributed over the band gap rather than having a discrete energy level, the "effective" activation energy is the difference between the conduction band edge and the average energy of the population of occupied interface states. For N_{it} of the form in Eq. (1), the effective activation energy (average occupied level) can be expressed as

$$E_c - E_{\mathrm{activation}} = -\frac{kT}{a}\ln\left[\frac{1}{g}Q_{\mathrm{it,avg}}\right], \tag{4}$$

where

$$Q_{\mathrm{it,avg}} = \frac{1}{E_g}Q_{\mathrm{it,total}} = \frac{1}{E_g}\int_{E_v}^{E_c} N_{\mathrm{it}}\mathrm{f_n}(E)\,dE. \tag{5}$$

In these expressions, E_g is the band gap of GaAs and $\mathrm{f_n}(E)$ is the Fermi distribution function. Using the parameters ob-

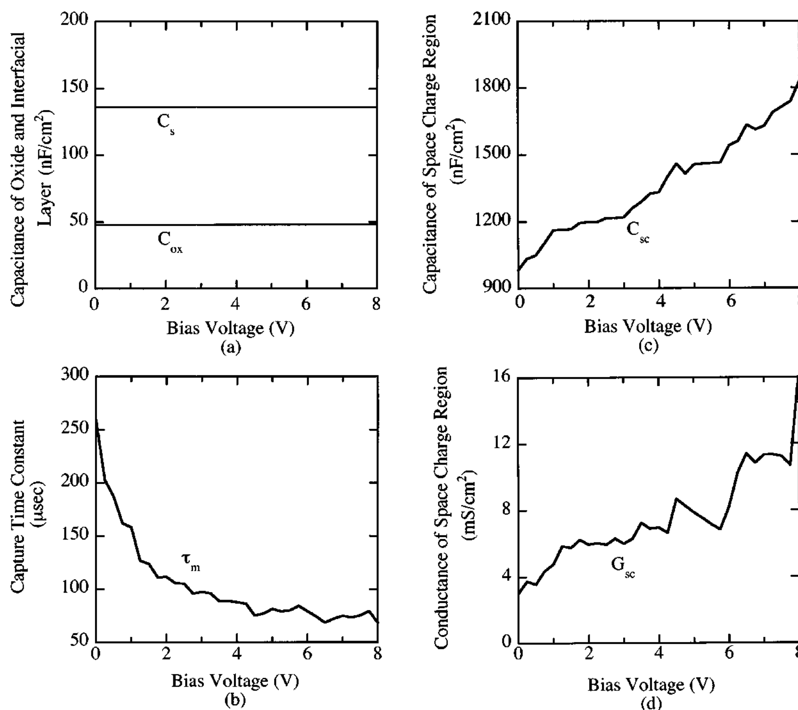

FIG. 3. Equivalent circuit model parameters as a function of applied bias voltage. (a) Capacitance of oxide C_{ox} and of interfacial region C_s, (b) capture time constant τ_m, (c) capacitance of space charge region C_{sc}, and (d) conductance of space charge region G_{sc}.

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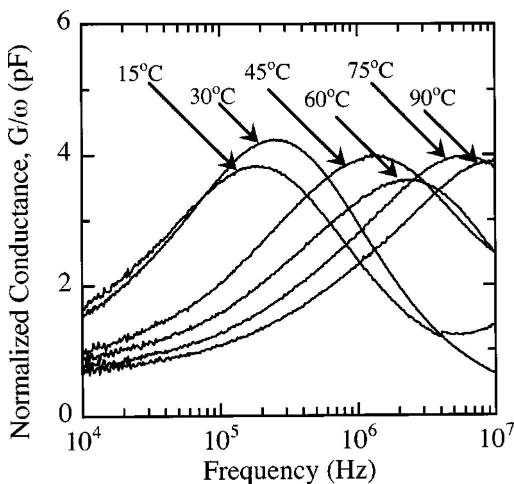

FIG. 4. Normalized conductance vs frequency curves as a function of temperature for an InAlP native oxide/GaAs MOS capacitor biased in accumulation (7 V).

tained from impedance spectroscopy measurements in Fig. 3, the effective activation energy is estimated to be 0.34 eV below the conduction band edge.

The impedance spectra of the MOS capacitors have also been measured at several different temperatures from 15 to 90 °C. The temperature dependence of the conductance is shown in Fig. 4 for a typical device biased in accumulation (applied bias voltage = 7 V). From Fig. 4, a clear shift in the frequency of the normalized conductance peak is observed. Figure 5 shows $\ln(T^2\tau)$ versus inverse temperature, where $\tau = 1/2\pi f_{\mathrm{peak}}$ and f_{peak} is the frequency of the conductance peak in the spectrum.[12] From the least-squares fit to this Arrhenius plot (correlation coefficient $r = 0.997$), we obtained an activation energy of 0.44 eV. This value is in good agreement with the result calculated above from room-temperature bias-dependent impedance measurements, showing that our extended equivalent circuit model with an exponential interface state distribution is consistent with both variable-bias and variable-temperature measurement results. We believe that the modest discrepancy in activation energy between these two methods arises from deviations in the actual interface distribution from a pure exponential form. The comparatively close agreement that is obtained, however, suggests that the overall trend of the interface state distribution is approximately exponential.

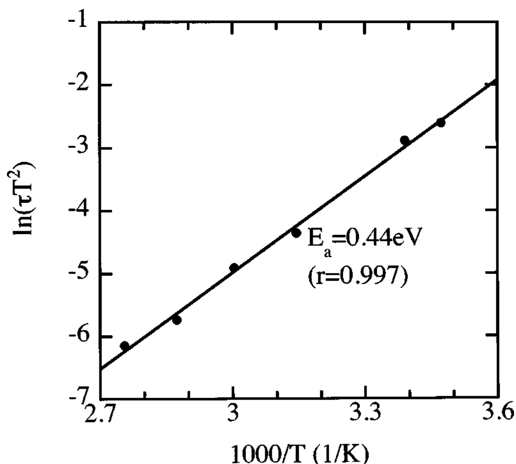

FIG. 5. Arrhenius plot of conductance peak frequency vs temperature for an InAlP native oxide/GaAs MOS capacitor biased in accumulation (7 V). The activation energy extracted from the slope is 0.44 eV.

CONCLUSION

In this article, we have demonstrated the suitability of impedance spectroscopy for the characterization of GaAs-based MOS capacitors with an InAlP native oxide as the gate insulator. An extended equivalent circuit model has been developed to model the measured electrical characteristics. This extended model is based on the conventional MOS capacitor model, but includes additional elements to account for the presence of an interfacial layer between the oxide and the semiconductor. The interface state distribution is estimated from bias- and temperature-dependent 40 Hz–10 MHz impedance measurements, revealing a relatively low total interface state density of $8 \times 10^{11}\ \mathrm{cm}^{-2}$. This suggests that the InAlP native oxide is a promising insulator for advanced MIS electronic device applications and merits further studies to optimize structure and process conditions that could further reduce the interface state density.

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