

GaAs MOSFET Using InAlP Native Oxide as Gate Dielectric

X. Li, Y. Cao, D. C. Hall, *Member, IEEE*, P. Fay, *Senior Member, IEEE*, B. Han, A. Wibowo, and N. Pan

Abstract—GaAs metal–oxide–semiconductor field-effect transistors (MOSFETs) using wet thermally oxidized InAlP as the gate insulator are reported for the first time. Leakage current measurements show that the 11-nm-thick native oxide grown from an $\text{In}_{0.49}\text{Al}_{0.51}\text{P}$ layer lattice-matched to GaAs has good insulating properties, with a measured leakage current density of $1.39 \times 10^{-7} \text{ mA}/\mu\text{m}^2$ at 1 V bias. GaAs MOSFETs with InAlP native gate oxide have been fabricated with gate lengths from 7 to 2 μm . Devices with 2- μm -long gates exhibit a peak extrinsic transconductance of 24.2 mS/mm, an intrinsic transconductance of 63.8 mS/mm, a threshold voltage of 0.15 V, and an off-state gate-drain breakdown voltage of 21.2 V. Numerical Poisson's equation solutions provide close agreement with the measured sheet resistance and threshold voltage.

Index Terms—GaAs MOSFET, InAlP native oxide, wet thermal oxidation.

I. INTRODUCTION

GaAs-based field effect transistors (FETs) offer speed advantages over Si-based FETs, primarily due to GaAs's higher electron mobility and the availability of semi-insulating GaAs substrates for high-performance on-chip passive components. Conventional GaAs-based metal–semiconductor field effect transistors (MESFETs) and high electron mobility transistors (HEMTs), however, use Schottky contacts as the gate electrode. Prone to excessive gate leakage current, Schottky gates restrict the forward gate bias to only a few tenths of a volt, resulting in limited power handling capability in power amplifier applications. An attractive alternative is a metal–insulator–semiconductor (MIS) gate structure. The inclusion of an insulator layer between the gate electrode and the semiconductor channel allows much larger gate voltage swings while preserving a low gate leakage current.

To realize these potential advantages, practical GaAs-based MISFETs require a gate insulator with a large bandgap for low gate leakage current and a high quality insulator/semiconductor interface for efficient channel modulation. The difficulty in achieving a high quality insulator/semiconductor interface has historically been the main obstacle to achieving high-performance GaAs-based MISFETs. Recent advances

have yielded promising results for device applications; for example, MISFETs have been demonstrated with gate insulators of Ga_2O_3 grown by molecular beam epitaxy (MBE) [1], oxidized GaAs prepared by ultraviolet and ozone treatment [2], Al_2O_3 grown by atomic layer deposition [3], [4], and wet thermally oxidized AlAs [5], [6].

Previous research has shown that InAlP native oxides have a much lower leakage current density and higher dielectric strength than that of oxidized AlGaAs [7]–[9], and a low interface state density between the oxide and GaAs has been demonstrated [10], making them attractive for device applications. In this article, GaAs-based metal–oxide–semiconductor field effect transistors (MOSFETs) using wet thermally oxidized InAlP as the gate insulator are reported for the first time.

II. DEVICE STRUCTURE AND FABRICATION

InAlP native oxide–GaAs MOSFETs were fabricated on a heterostructure grown by metal–organic chemical vapor deposition. The structure was grown on a semi-insulating GaAs substrate. A 100-nm-thick undoped GaAs buffer layer was grown first, followed by a 100-nm Si-doped GaAs channel ($N_d \sim 1 \times 10^{17} \text{ cm}^{-3}$), a 4-nm undoped $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$ oxidation stop layer, 10 nm of undoped $\text{In}_{0.49}\text{Al}_{0.51}\text{P}$ lattice-matched to GaAs, and a 40-nm GaAs cap layer. The InAlP layer was wet thermally oxidized at 440°C for 25 min immediately after removing the GaAs cap layer by selective wet etching in a citric acid and hydrogen peroxide solution. Details of the oxidation process have been published previously [8]. After oxidation, the oxide thickness was measured to be 11 nm by variable angle spectroscopic ellipsometry. Devices were mesa isolated using wet-chemical etching, and source and drain regions were formed by wet etching to the channel followed by AuGe/Ni/Au contact deposition and rapid thermal annealing. Ti/Au metal gates were deposited using electron-beam evaporation and liftoff. The nominal source-to-gate and drain-to-gate spacings of all the fabricated devices are 1.5 μm , and the gate widths are 100 μm . MOSFETs with gate lengths from 2 to 7 μm were fabricated.

III. RESULTS AND DISCUSSION

DC characteristics of GaAs-based MOSFETs with InAlP native oxide gate insulators were measured; Fig. 1 shows the common-source current–voltage (I – V) characteristics for a 2- μm gate length device, and Fig. 2 shows the drain current and transconductance as a function of gate bias voltage. The dc characteristics show a clear pinch-off and channel modulation, with a peak extrinsic transconductance of 24.2 mS/mm and enhancement-mode operation (threshold voltage of +0.15 V).

Manuscript received July 28, 2004; revised September 23, 2004. This work was supported by the Air Force Office of Scientific Research under Grant AF-F49620-01-1-0331. The review of this letter was arranged by Editor T. Mizutani.

X. Li, Y. Cao, D. C. Hall, and P. Fay are with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA (e-mail: pfay@nd.edu).

B. Han, A. Wibowo, and N. Pan are with Microlink Devices, Inc., Niles, IL 60714 USA.

Digital Object Identifier 10.1109/LED.2004.838555

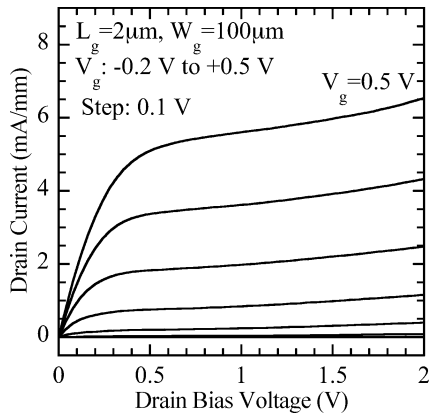


Fig. 1. Drain current versus drain bias as a function of gate bias for a $2 \times 100 \mu\text{m}^2$ MOSFET.

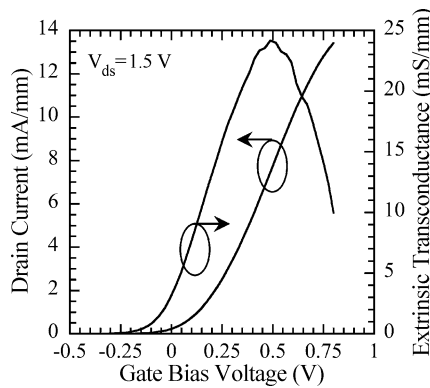


Fig. 2. Drain current and extrinsic transconductance versus gate bias for a $2 \times 100 \mu\text{m}^2$ MOSFET. The drain bias is 1.5 V.

The on-resistance of the MOSFETs, R_{on} , at 0.5 V gate bias was measured on devices as a function of gate length. From the gate length dependence of R_{on} (not shown), the extracted source series resistance, R_s , was found to be 260Ω , and the channel sheet resistance at 0.5 V gate bias was $5525 \Omega\text{sq}$. The intrinsic transconductance was calculated using $g_{m,\text{int}} = g_{m,\text{ex}} / (1 - g_{m,\text{ex}} R_s)$, where $g_{m,\text{ex}}$ and $g_{m,\text{int}}$ are the extrinsic and intrinsic transconductances, respectively. Fig. 3 shows the peak extrinsic and intrinsic transconductance versus gate length of MOSFETs with 2, 3, 5, and 7 μm gate lengths. The transconductances were measured at 1.5 V drain bias voltage. As shown in Fig. 3, the calculated peak intrinsic transconductance improved from 23.8 mS/mm for a 7 μm gate length to 63.8 mS/mm at a gate length of 2 μm , and the $g_{m,\text{int}}$ follows closely the expected $1/L_g$ trend. The large source series resistance arises from a combination of the unoptimized ohmic contact resistance on this sample and the large channel sheet resistance of these first-generation devices.

Numerical solution of the one-dimensional Poisson's equation [11] was also performed on this FET structure. In the simulation, the bandgap and relative permittivity of the InAlP oxide was set to 4 eV [9] and 6.57 [8], respectively, and the conduction band offset (ΔE_c) between InGaP and GaAs was 0.22 eV [12]. For calculation of the sheet resistance, an electron mobility of $3000 \text{ cm}^2/\text{Vs}$ was used for the GaAs channel, consistent

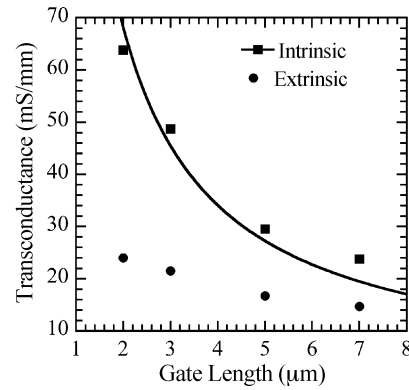


Fig. 3. Peak extrinsic and intrinsic transconductance for different gate lengths. The gate width is $100 \mu\text{m}$ for all the devices and the drain bias is 1.5 V in all measurements. Solid line shows $1/L_g$ trend.

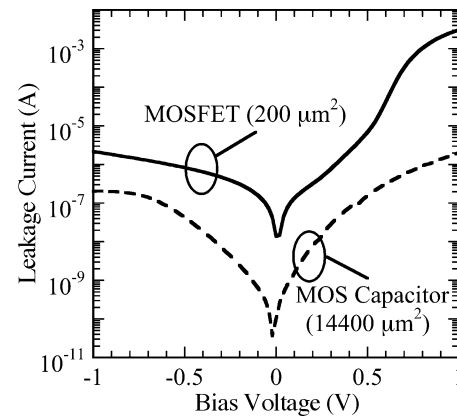


Fig. 4. Typical oxide leakage I - V characteristics of MOSFETs and MOS capacitors. The MOSFET gate area is $200 \mu\text{m}^2$, and the capacitor top plate area is $14400 \mu\text{m}^2$.

with Hall effect measurements. Using a 1.6-eV Schottky barrier height between the gate metal and oxide and a 0.7-eV ΔE_c between the InAlP oxide and GaAs, the simulation gives a structure sheet resistance of $5350 \Omega\text{sq}$ at 0.5-V gate bias and a 0.1-V threshold voltage, compared to the measured sheet resistance of $5525 \Omega\text{sq}$ and 0.15-V threshold voltage. The modest difference between the measured and simulated values may arise from the effect of any interface states and the uncertainty in the conduction band offsets used in the simulation.

Gate leakage current and off-state gate-drain breakdown voltage of the MOSFETs were also measured. A typical gate leakage I - V curve of a MOSFET with a 2- μm gate length ($200 \mu\text{m}^2$ gate area) is shown in Fig. 4. Similar I - V characteristics were obtained on MOSFETs of all gate lengths, and the leakage current was found to be essentially independent of gate electrode area. Also shown in Fig. 4 is the measured leakage current of a MOS capacitor fabricated on the same heterostructure as the MOSFETs with a $14400 \mu\text{m}^2$ electrode area. The MOS capacitor and MOSFET samples share the same oxidation and metallization processes. As can be seen from the figure, even with a much larger area, the leakage current of the MOS capacitor is three orders of magnitude lower than that of the MOSFET at 1-V gate bias. The comparison suggests that the 11-nm InAlP oxide has good insulating properties ($1.39 \times 10^{-7} \text{ mA}/\mu\text{m}^2$ at 1 V bias from MOS capacitor

I - V) and that the gate leakage current observed in the FETs comes from a parasitic gate-leakage path at the edge of the mesas that is not present in the MOS capacitor test structures. Improvement in device isolation processing is expected to improve the MOSFET gate leakage [13]. Even with the parasitic gate-leakage path, an off-state gate-drain breakdown of 21.2 V was obtained on a 2- μ m gate length device, indicating the high-quality of the InAlP native oxide.

IV. CONCLUSION

GaAs-based MOSFETs using InAlP native oxide as the gate insulator have been reported for the first time. Devices with 2- μ m gate lengths exhibit a peak intrinsic transconductance of 63.8 mS/mm and an off-state gate-drain breakdown voltage of 21.2 V. The devices show clear channel modulation and solid pinch-off, indicating that the wet thermal oxidation process generates a clean interface between the oxide and GaAs channel. Low gate leakage current can be expected with an optimized device isolation process. This suggests that the InAlP native oxide is a promising insulator for advanced MIS device applications.

ACKNOWLEDGMENT

The authors would like to thank Prof. G. L. Snider for useful discussions.

REFERENCES

[1] M. Passlack, J. K. Abrokwhah, R. Droopad, Z. Yu, C. Overgaard, S. I. Yi, M. Hale, J. Sexton, and A. C. Kummel, "Self-aligned GaAs p-channel enhancement mode MOS heterostructure field-effect transistor," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 508–510, Sep. 2002.

[2] K. Iiyama, Y. Kita, Y. Ohta, M. Nasuno, S. Takamiya, K. Higashimine, and N. Ohtsuka, "Fabrication of GaAs MISFET with nm-thin oxidized layer formed by UV and ozone process," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 1856–1862, Nov. 2002.

[3] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergeant, M. Hong, K. K. Ng, and J. Bude, "GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 209–211, Apr. 2003.

[4] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, M. Hong, K. K. Ng, and J. Bude, "Depletion-mode InGaAs metal-oxide-semiconductor field-effect-transistor with oxide gate dielectric grown by atomic-layer-deposition," *Appl. Phys. Lett.*, vol. 84, pp. 434–436, 2004.

[5] E. I. Chen, N. Holonyak, Jr., and S. A. Maranowski, "Al_xGa_{1-x}As-GaAs metal-oxide-semiconductor field-effect transistors formed by lateral water vapor oxidation of AlAs," *Appl. Phys. Lett.*, pp. 2688–2690, 1995.

[6] K. B. DeMelo, D. C. Hall, G. L. Snider, D. Xu, G. Kramer, and N. El-Zein, "High electron mobility InGaAs-GaAs field effect transistor with thermally oxidised AlAs gate insulator," *Electron. Lett.*, vol. 36, no. 1, pp. 84–86, 2000.

[7] A. L. Holmes, "Compound semiconductor native oxide-based technologies for optical and electrical devices grown on GaAs substrates using MOCVD," Ph.D. dissertation, Univ. Texas, Austin, 1999.

[8] P. J. Barrios, D. C. Hall, G. L. Snider, T. H. Kosel, U. Chowdhury, and R. D. Dupuis, "Electrical properties of InAlP native oxides for GaAs-based MOS applications," in *Proc. Int. SOTAPOCS XXXIV*, vol. 2001-1, F. Ren, D. N. Buckley, S. N. G. Chu, and S. J. Pearton, Eds., Pennington, NJ, pp. 258–264.

[9] Y. Cao, J. Zhang, X. Li, T. H. Kosel, P. Fay, D. C. Hall, R. E. Cook, X. Zhang, and R. D. Dupuis, "Electrical properties and microstructure of InAlP native oxides for MOS applications," in *Proc. Electron. Mater. Conf.*, 2004, p. 88.

[10] X. Li, Y. Cao, D. C. Hall, P. Fay, X. Zhang, and R. D. Dupuis, "Electrical characterization of native-oxide InAlP/GaAs metal-oxide-semiconductor heterostructures using impedance spectroscopy," *J. Appl. Phys.*, vol. 95, pp. 4209–4212, 2004.

[11] I.-H. Tan, G. L. Snider, and E. L. Hu, "A self-consistent solution of Schrödinger-Poisson equation using a nonuniform mesh," *J. Appl. Phys.*, vol. 68, pp. 4071–4076, 1990.

[12] K. F. Brennan and A. S. Brown, *Theory of Modern Electronic Semiconductor Devices*. New York: Wiley, 2002.

[13] S. R. Bahl, M. H. Leary, and J. A. del Alamo, "Mesa-sidewall gate leakage in InAlAs/InGaAs heterostructure field-effect transistors," *IEEE Trans. Electron Devices*, vol. 39, no. 9, pp. 2037–2043, Sep. 1992.