

# Epitaxially Grown Si Resonant Interband Tunnel Diodes Exhibiting High Current Densities

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**Abstract**—This study presents the room-temperature operation of  $\delta$ -doped Si resonant interband tunneling diodes which were fabricated by low-temperature molecular beam epitaxy. Post growth rapid thermal annealing of the samples was found to improve the current-voltage ( $I$ - $V$ ) characteristics. Optimal performance was observed for a 600 °C 1 min anneal, yielding a peak-to-valley current ratio (PVCR) as high as 1.38 with a peak current density ( $J_p$ ) as high as 1.42 kA/cm<sup>2</sup> for a device with a 4-nm intrinsic Si tunnel barrier. When the tunnel barrier was reduced to 2 nm, a PVCR of 1.41 with a  $J_p$  as high as 10.8 kA/cm<sup>2</sup> was observed. The devices withstood a series of burn-in measurements without noticeable degradation in either the  $J_p$  or PVCR. The structures presented are strain-free, and are compatible with a standard CMOS or HBT process.

**Index Terms**—CMOS compatibility, molecular beam epitaxy, negative differential resistance, rapid thermal annealing, resonant interband tunneling diodes, silicon.

## I. INTRODUCTION

TUNNEL diodes are undergoing a rebirth particularly in the III-V material systems where integrated tunnel diode/transistor circuits are showing promise for mixed signal [1], [2] and memory [3], [4] applications. However, the lack of a Si-based process compatible with CMOS or SiGe heterojunction bipolar transistor (HBT) technology has impeded similar efforts in Si. Many of the earliest Si-based tunnel diodes, including the Si Esaki diode with the highest reported peak-to-valley current ratio (PVCR) of 4.0 [5], were fabricated via an alloying process. While this technique was adept at fabricating discrete devices, it was not suited for integrated circuit processing [6]. Valient attempts were made in the early 1990's to fabricate Si/SiGe resonant tunneling diodes (RTD's), but the lack of a material capable of achieving a conduction band offset prevented the realization of RTD's with PVCR's much greater than 1.2 [7]. A recent letter by the authors presented the room-temperature operation of  $\delta$ -doped Si/Si<sub>0.5</sub>Ge<sub>0.5</sub>/Si resonant interband tunneling diodes (RITD's) which were fabricated epitaxially by low-temperature molecu-

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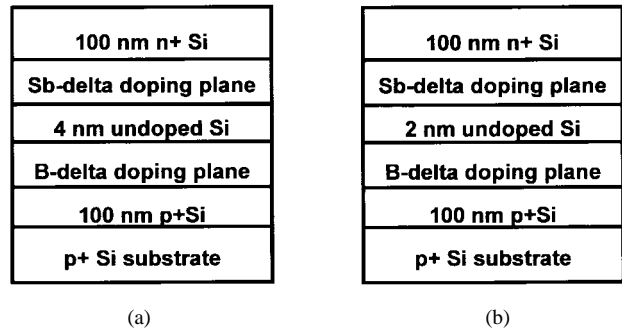


Fig. 1. Schematic diagrams of the Si RITD structures. (a) The tunnel barrier of SiTD1 is 4 nm of undoped Si. (b) The tunnel barrier of SiTD2 is 2 nm of undoped Si.

lar beam epitaxy (LT-MBE) [8]. As-grown samples showed no evidence of negative differential resistance (NDR). However, heat treatments in a rapid thermal annealing (RTA) furnace used for dopant activation and point defect reduction resulted in NDR behavior. PVCR's as high as 1.5 at a peak current density of 3.2 kA/cm<sup>2</sup> were reported for a 1-min anneal at 700 °C. Beyond this temperature, the current density was found to abruptly decrease by an order of magnitude. This letter builds upon the previous study, presenting epitaxially fabricated  $\delta$ -doped RITD structures consisting purely of Si which exhibit NDR at room temperature.

The key differences between the RITD's studied here and the previously reported Si/SiGe/Si RITD's are 1) a purely Si tunnel barrier eliminates critical thickness issues and strain associated with SiGe alloys, 2) strain relaxation during the RTA heat treatments is avoided, and 3) quantum confinement is not aided by the presence of a heterojunction discontinuity. The two structures presented, which will be referred to as SiTD1 and SiTD2, are shown in Fig. 1. The only variation between the two structures is the tunnel barrier thickness, which is 4 nm of undoped Si for SiTD1 and 2 nm of undoped Si for SiTD2. As with the previously reported Si/Si<sub>0.5</sub>Ge<sub>0.5</sub>/Si RITD's, B and Sb  $\delta$ -doped injectors are used to create confined states in the valence and conduction bands, respectively. Fig. 2 shows a calculated band diagram for SiTD1. The  $\delta$ -doped regions are assumed broadened over 1 nm with a dopant activation of 50%. The diagram was generated by solving the effective-mass Schrödinger equation and corresponding quantum charge for each band and iterating to convergence with Poisson's equation. As evidenced in this diagram, the built-in voltage drops across the intrinsic region. This region,

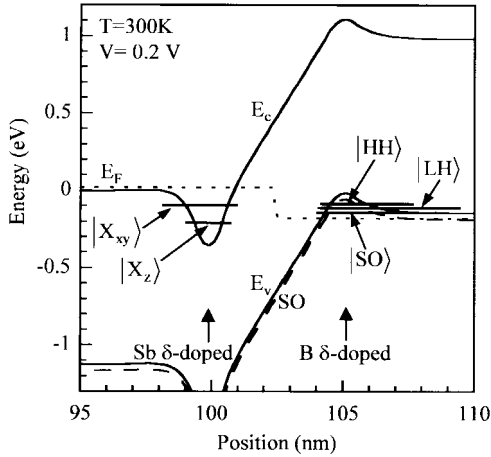


Fig. 2. Calculated energy band diagram and resonant states of SiTD1. The Sb and B activation of the  $\delta$ -doped regions is assumed to be 50%.  $X_z$  denotes the conduction band minimums along the  $k_z$  axis of the Brillouin zone, and  $X_{xy}$  denotes the conduction band minimums along the  $k_x$  and  $k_y$  axes where  $z$  is the growth direction. SO denotes the split-off valence band-edge.

therefore, is also treated as the tunnel barrier. As Si has an indirect bandgap, the peak current in this structure is attributed to phonon assisted tunneling between the  $X_{xy}$  electron and light hole states [9]. The NDR in this structure results from a decrease in the tunneling probability with applied bias as these bands uncross.

## II. EXPERIMENTAL SETUP

Epitaxial growth was achieved with a specially designed MBE growth system [10] using elemental Si and Ge in e-beam sources, elemental Sb in a standard Knudsen cell and elemental B in a high-temperature Knudsen cell. The structures were grown on 75-mm B-doped ( $\rho = 0.015\text{--}0.04 \Omega\cdot\text{cm}$ ) Si(100) wafers. Prior to growth, the substrates were prepared using a cleaning technique previously described [11]. The growths were initiated with a 2-nm undoped Si buffer layer grown at 700 °C. The substrate temperature was then lowered to 540 °C for the growth of a 70-nm B-doped  $p^+$ -Si ( $2 \times 10^{19}/\text{cm}^3$ ) layer. The substrate temperature was further reduced to 370 °C for the remainder of the sample growth. This included a B  $\delta$ -doped layer ( $7 \times 10^{13}/\text{cm}^2$ ), an undoped tunneling barrier (see Fig. 1), an Sb  $\delta$ -doped layer ( $3 \times 10^{14}/\text{cm}^2$ ), and a 100-nm Sb-doped  $n^+$ -Si ( $4 \times 10^{19}/\text{cm}^3$ ) contact layer. All regions of the sample were grown at a rate of 0.1 nm/s. Furthermore, with the exception of the lack of Ge in SiTD1 and SiTD2, their growth and doping was essentially identical to that of the previously reported Si/Si<sub>0.5</sub>Ge<sub>0.5</sub>/Si RITD's.

A series of samples were annealed under a 15% H<sub>2</sub> 85% N<sub>2</sub> ambient in an AG Associates Heatpulse 610 Rapid Thermal Annealing Furnace. The anneal time of all samples was fixed at one minute. Anneal temperatures of 500, 550, 600, 650, and 700 °C were employed in this study. Control samples without heat treatment were also fabricated for SiTD1 and SiTD2.

Al dots with diameters of 5, 10, 18, 50, and 75  $\mu\text{m}$  were patterned on the surface of the wafer via a standard contact lithography/liftoff process. The samples were dipped in a buffered oxide etch prior to metallization to remove the native

TABLE I  
SUMMARY OF THE ROOM TEMPERATURE  $I$ - $V$  CHARACTERISTICS OF THE Si RITD'S FOR SiTD1 AND SiTD2. RESULTS FROM 18  $\mu\text{m}$  DIAMETERS DIODES FROM SUBSTRATES ANNEALED AT 1 min ARE SHOWN. A PVCR ENTRY OF 1.00 INDICATES THAT THE DEVICE EXHIBITED A PLATEAU IN THE FORWARD DIRECTION RATHER THAN NDR BEHAVIOR

T (°C)		500	550	600	650	700
SiTD1	$J_p$ (kA/cm <sup>2</sup> )	1.60	0.61	1.36	0.87	0.17
	$J_v$ (kA/cm <sup>2</sup> )	—	0.52	0.98	0.65	0.15
PVCR		1.00	1.15	1.38	1.35	1.15
SiTD2	$J_p$ (kA/cm <sup>2</sup> )	32.00	15.8	9.40	1.40	0.46
	$J_v$ (kA/cm <sup>2</sup> )	27.0	14.8	6.28	1.28	0.41
PVCR		1.17	1.07	1.45	1.1	1.1

oxide. The Al dots served as a mask when the samples were etched in a CF<sub>4</sub>/O<sub>2</sub> plasma for mesa isolation. Finally, an Al backside contact was thermally evaporated to complete the device fabrication.

## III. RESULTS AND DISCUSSION

Room temperature current-voltage ( $I$ - $V$ ) characteristics were measured both with an HP 4142 Semiconductor Parameter Analyzer and a Textronix curve tracer. In contrast to the previous study, NDR behavior was observed in the control samples which were not heat treated. However, NDR was only evident in the 5- and 10- $\mu\text{m}$  diameter diodes of the control samples, and the observed PVCR from these samples was barely greater than one. Post-growth heat treatments substantially improved the device performance.

Table I summarizes the peak current density ( $J_p$ ), valley current density ( $J_v$ ), and PVCR of 18  $\mu\text{m}$  diameter diodes resulting from each anneal temperature employed on SiTD1 and SiTD2. The largest combination of  $J_p$  and PVCR occurred after a 600 °C, 1-min anneal for both SiTD1 and SiTD2; a PVCR of 1.38 with a  $J_p$  of 1.36 kA/cm<sup>2</sup>, and a PVCR of 1.45 with a  $J_p$  of 9.4 kA/cm<sup>2</sup> were observed for SiTD1 and SiTD2, respectively. Anneal temperatures above this optimal value led to lower values of  $J_p$ . It should also be noted that the degradation of Si RITD's occurred at an anneal temperature 100 °C below that of the Si/Si<sub>0.5</sub>Ge<sub>0.5</sub>/Si RITD study [8], possibly because the diffusion of B is more rapid in bulk Si than in Si<sub>1-x</sub>Ge<sub>x</sub> alloys [12].

Spacer thickness had a significant influence on  $J_p$  and  $v$ . Fig. 3 shows an overlay of the  $I$ - $V$  characteristics of 10  $\mu\text{m}$  diameter diodes from SiTD1 and SiTD2, both annealed at a temperature of 600 °C for 1 min. The current density of SiTD2 (10.8 kA/cm<sup>2</sup>) is almost an order of magnitude larger than that of SiTD1 (1.42 kA/cm<sup>2</sup>). Since the devices were grown under identical conditions with the exception of spacer thickness, the elevated current density of SiTD2 must be due to its thinner spacer. The fact that all entries from SiTD1 in Table I have smaller  $J_p$  and  $J_v$  values than corresponding entries from SiTD2 reinforces this conclusion. However, a reduction in spacer thickness did not yield as sharp of an increase in current density as the authors originally suspected. This may suggest that the depletion region for these structures extends beyond the  $\delta$ -doping planes. With proper adjustments to the doping levels and to growth parameters, this problem may be avoided.

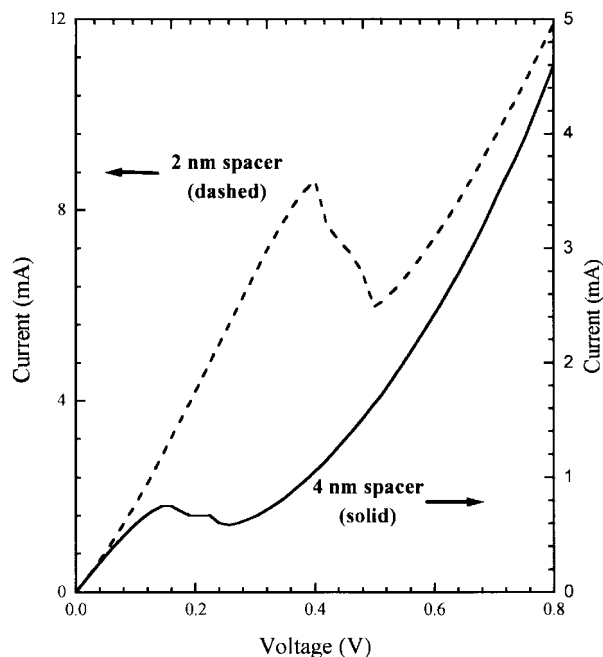


Fig. 3.  $I$ - $V$  characteristics of Si RITD's with 4-nm (SiTD1) and 2-nm (SiTD2) tunnel barriers. The current from the 2-nm structure and 4-nm structures are plotted on the left and right axes, respectively. The diodes shown have a  $10\text{-}\mu\text{m}$  diameter and were annealed at  $600\text{ }^\circ\text{C}$  for 1 min. The 4-nm device had a PVCR of 1.42 with a  $J_p$  of  $1.42\text{ kA/cm}^2$ . The 2-nm device had a PVCR of 1.41 with a  $J_p$  of  $10.8\text{ kA/cm}^2$ .

The variation in peak voltage evident in Fig. 3 is attributed to the series resistance of the Al contacts.

A burn-in study was performed on a portion of SiTD2 annealed at  $600\text{ }^\circ\text{C}$ . The devices on this sample were cycled between  $-1.5$  and  $1.5\text{ V}$  at a rate of 18 cycles/s for the first 20 500 cycles. The rate was then increased to 42 cycles/s for the duration of the measurements. A 0.47% reduction in  $J_p$  and  $J_v$  was observed over the first 20 500 cycles. The  $I$ - $V$  characteristics then remained essentially unchanged after 83 800 cycles.

#### IV. CONCLUSION

In conclusion, Si RITD's were fabricated epitaxially and found to exhibit NDR behavior at room temperature. PVCR's up to 1.42 with a  $J_p$  as high as  $1.42\text{ kA/cm}^2$  and up to 1.41 with a  $J_p$  as high as  $10.8\text{ kA/cm}^2$  were observed after a 1-min  $600\text{ }^\circ\text{C}$  anneal for 4- and 2-nm undoped Si spacers, respectively. The current density of the RITD's was found to depend on the thickness of the undoped Si spacer, allowing for engineering of the peak current density for specific device applications. Optimal anneal conditions may be affected by the interdiffusion of dopants, as device degradation occurred

$100\text{ }^\circ\text{C}$  below the  $700\text{ }^\circ\text{C}$ , 1-min optimal anneal previously reported for Si/SiGe/Si RITD's. The devices withstood a burn-in study which demonstrated their reliability for circuit operation. The device structure, as well its low temperature fabrication process makes it a strong candidate for integration in a CMOS or HBT fabrication line.

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