

A Monolithic 4-Bit 2-Gsps Resonant Tunneling Analog-to-Digital Converter

Tom P. E. Broekaert, Berinder Brar, *Member, IEEE*, J. Paul A. van der Wagt, *Member, IEEE*, Alan C. Seabaugh, *Senior Member, IEEE*, Frank J. Morris, *Member, IEEE*, Theodore S. Moise, *Member, IEEE*, Edward A. Beam, III, *Member, IEEE*, and Gary A. Frazier

Abstract—The combination of resonant-tunneling diodes and heterostructure field-effect transistors provides a versatile technology for implementing microwave digital and mixed-signal applications. Here we demonstrate and characterize the first monolithic flash analog-to-digital converter (ADC) in this technology. The first-pass ADC achieved 2.7 effective bits at 2 gigasamples per second (Gsps) for a 220-MHz input signal. The one-bit quantizer achieved a single-tone spurious free dynamic range greater than 40 dB at 2 Gsps for a 220-MHz single-tone input with dithering.

Index Terms—Analog–digital conversion, FET’s, indium compounds, quantization, resonant tunneling diodes, sample and hold circuits.

I. INTRODUCTION

ULTRAFast analog-to-digital converters (ADC’s) are finding increased application in sampling scopes, digital receivers, and phased array radars [1]–[4]. Modern ADC’s exceed 1-gigasample-per-second (Gsps) conversion rates, which enables digital receivers without analog channelization. With higher conversion rates the ADC can be moved closer to the front end, resulting in a more versatile digital receiver. For X-band operation, an ADC with a sampling rate of at least 20 Gsps will be required. To extend the ADC operation beyond 20 Gsps, a comparator function capable of analog-to-digital decisions in less than 25 ps is needed.

Conventional transistor-based comparators typically use regenerative feedback to obtain a valid digital output within a single clock cycle. The regeneration time constant associated with the feedback loop must be very small compared to the

clock period to achieve high sensitivity and is limited by the circuit interconnect loop delay and by transistor propagation delays. High speed and high sensitivity must then be obtained through compact circuit layout and the use of high-speed transistors.

As an alternative we propose and demonstrate novel high-speed circuit topologies enabled by a monolithic resonant-tunneling diode (RTD)/heterostructure field-effect transistor (HFET) technology. With the RTD available to the circuit designer, a more compact and faster comparator can be designed. The RTD is highly nonlinear and inherently self-latching with an appropriate load. When the RTD is operated as a current comparator, the self-latching is exploited to obtain a comparator where *no circuit feedback is required* and the “regeneration” time is limited only by the RTD and its intrinsic and parasitic capacitive load. With RTD’s capable of 1.5-ps large-signal switching transients [5], RTD-based comparators are expected to operate at clock rates exceeding 20 Gsps. RTD/HFET circuits typically feature reduced component count, lower power dissipation, and higher speed compared to transistor-only designs.

Previous efforts at RTD-based ADC’s have focused on a folding approach [6], [7]. Here we report on the first RTD-based flash ADC integrated circuit [8]. The flash architecture of the 4-bit 2-Gsps ADC provides a straightforward implementation and intrinsic high speed. A conservative HFET gate length (0.5 μm) and RTD peak current density (10 kA/cm^2) were used for this demonstration. Fig. 1 shows the completed $1.9 \times 2.1\text{-mm}^2$ ADC die.

II. DESIGN

A. RTD and HFET SPICE Models

RTD and HFET device models for SPICE simulation were obtained by fitting simulated to measured DC and S parameters. The RTD model [9] is similar to one recently published [10] and is described in Appendix A. For the HFET, the model of [11] was modified and implemented in a proprietary version of SPICE. An essential feature of the device models is the use of a continuous expression with continuous derivatives for the DC characteristics; for the RTD to describe the DC I–V characteristic, and for the HFET output characteristic to describe the subthreshold, linear, and saturated regimes of the

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T. P. E. Broekaert, B. Brar, A. C. Seabaugh, F. J. Morris, and G. A. Frazier are with Applied Research Laboratories, Raytheon Systems, Dallas, TX 75265 USA (e-mail: t-broekaert@rtis.ray.com).

J. P. A. van der Wagt was with Applied Research Laboratories, Raytheon Systems, Dallas, TX 75265 USA. He is now with Rockwell Science Center, Thousand Oaks, CA 91360 USA.

T. S. Moise was with Applied Research Laboratories, Raytheon Systems, Dallas, TX 75265 USA. He is now with Texas Instruments, Dallas, TX 75265 USA.

E. A. Beam, III, was with Applied Research Laboratories, Raytheon Systems, Dallas, TX 75265 USA. He is now with TriQuint Semiconductor Texas, Dallas, TX 75265 USA.

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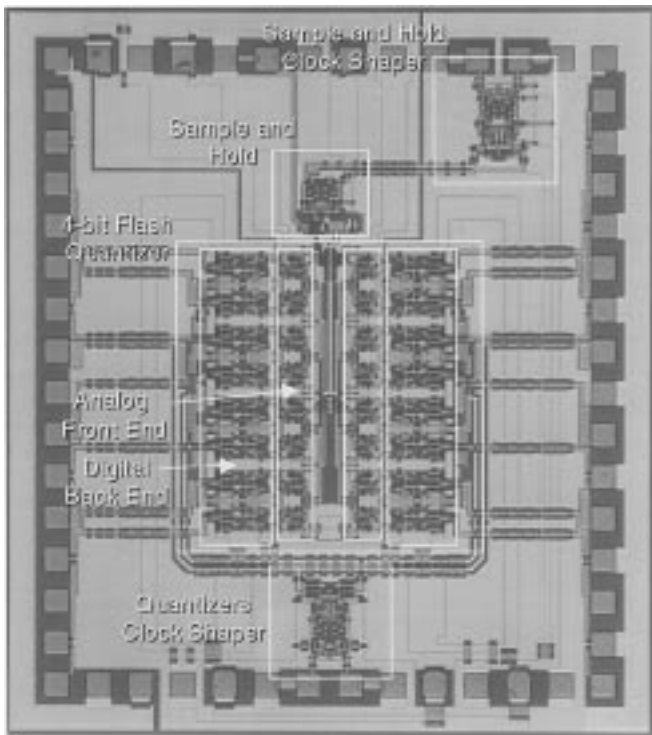


Fig. 1. Photomicrograph of the resonant-tunneling diode/heterojunction field-effect transistor analog-to-digital converter, measuring $1.9 \times 2.1 \text{ mm}^2$. The ADC die has 450 components, including 64 RTD's, 225 HFET's, Schottky diodes, resistors, and capacitors.

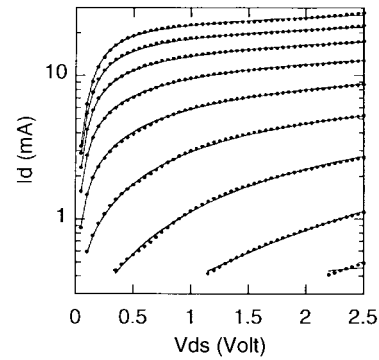
HFET. The continuous I-V expressions ensure convergence in transient simulations of HFET-RTD circuits in standard versions of SPICE; i.e., no new or modified convergence algorithms are required. Fig. 2 shows the excellent agreement between model and experiment for the RTD and in both the HFET large-signal and subthreshold regime.

B. ADC Architecture

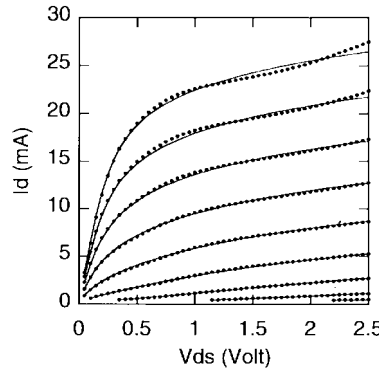
The flash-ADC reported here consists of an HFET sample-and-hold followed by 16 RTD/HFET clocked-comparators as shown in the block diagram in Fig. 3. Two on-chip clock shapers supply the clock signals for the sample-and-hold and for the 16 clocked-comparators. The ADC outputs a 16-level thermometer code. The sample-and-hold and clocked-comparators have a single-ended signal path with differential clock shaping and distribution. The single-ended signal path design limits the design to operation speeds up to a few GHz using the chosen transistors. The power supplies, including ground, of the analog quantizer front-end and sample-and-hold are separate from those of the digital ADC components. The circuit layout was optimized to minimize noise coupling between all power supplies as well as between components powered by the same supplies. On-chip capacitance was maximized within the given die area.

C. Sample-and-Hold

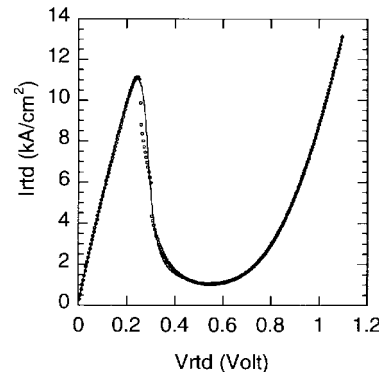
The sample-and-hold is an FET-only design with a pass-transistor, hold capacitor, buffer amplifier, and switching logic similar to the analog sampling switch described in [7]. The



(a)



(b)



(c)

Fig. 2. Simulated (solid lines) and measured (dots) DC data for (a) the HFET output characteristics on a linear scale, (b) on a logarithmic scale, and (c) the RTD I-V characteristics. Agreement between model and measured data is within a few percent rms error.

schematic is shown in Fig. 4. To provide a more constant on-resistance for a large input signal range of the pass gate in an n-channel only FET design, it is necessary to drive the pass gate FET with a gate bias that tracks the input signal. This tracking is achieved with a source follower at the output. This source follower output is then used as the supply rail of a differential-pair gain-stage that has the sample-and-hold clock as input. The output clock from the differential-pair gain-stage tracks the input signal during sampling and drives the sample-and-hold pass gate. In this design, the switching logic follows the output of the sample-and-hold rather than the input for lower hold-state input-signal feedthrough and improved linearity. The sample-and-hold design has a SPICE-simulated linearity of about 60 dB at 2 Gsps.

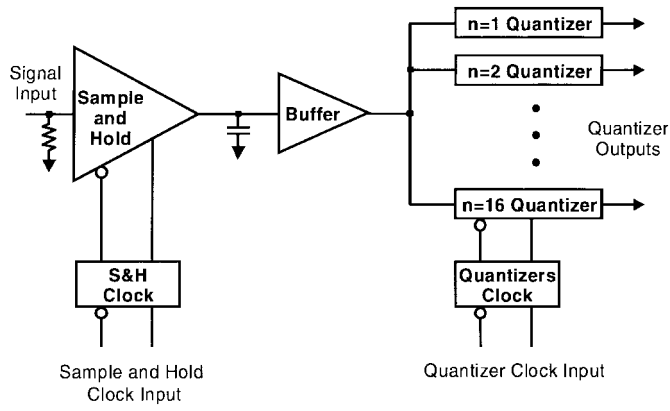


Fig. 3. Block diagram of the RTD-based flash ADC. The ADC consists of a sample-and-hold, buffer, 16 quantizers, and on-chip clock shapers. The threshold level of each of the quantizers is set through RTD-area sizing.

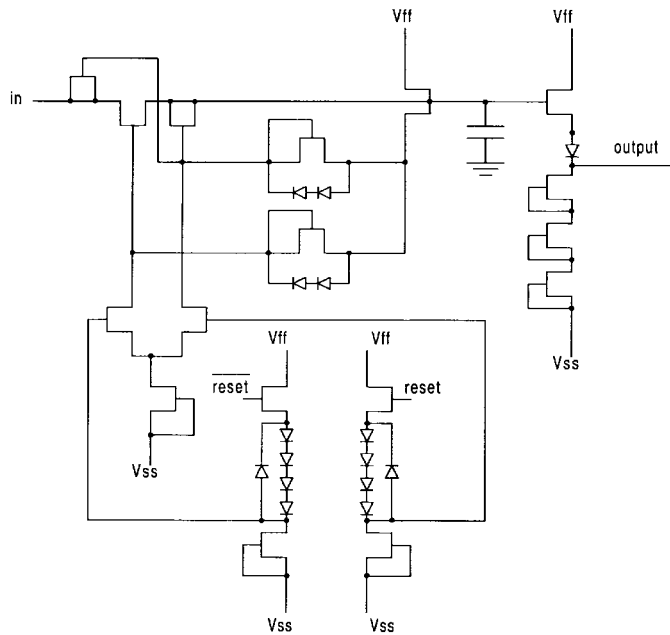


Fig. 4. Schematic diagram of the sample-and-hold. The sample-and-hold is a FET-only design with a pass-transistor FET, hold capacitor, buffer amplifier, and switching logic.

D. Clocked Comparator

The circuit diagram of the RTD/HFET clocked-comparator is shown in Fig. 5 [12]. The input HFET and the RTD at the source terminal (RTD-S) convert the input voltage to a current which is compared to the load RTD (RTD-L) current. The source-terminal RTD never switches and is used only as a resistor matched to the load RTD. By linearly sizing only the area of the load-RTD the trip point of the comparator is set for each of the 16 comparators. The nonlinear behavior of the RTD makes the comparator self-latching and obviates the need for circuit-level regenerative feedback. As a result, the RTD-based comparator is very compact and capable of high-speed operation.

The logic output levels of the comparator at this stage are the “prepeak” ($V_{out} > V_{AVdd} - V_{peak}$) and “post-peak” (i.e., valley, $V_{out} < V_{AVdd} - V_{valley}$) voltage states of the RTD.

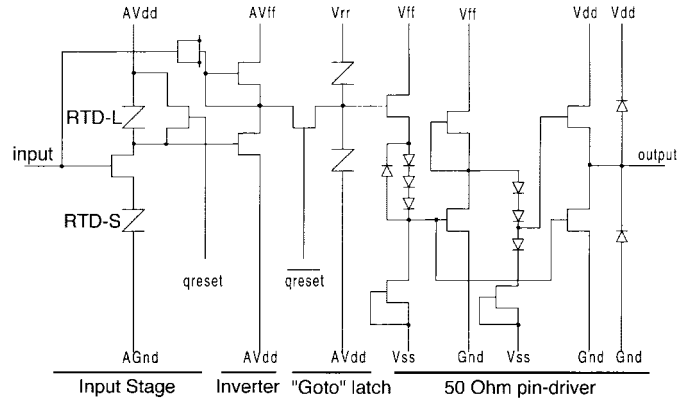


Fig. 5. Schematic diagram of one of the 16 flash comparators, consisting of 13 HFET’s, four RTD’s, and nine Schottky diodes. The four RTD’s belong to the section with an analog ground, AGND, separate from the digital ground, GND.

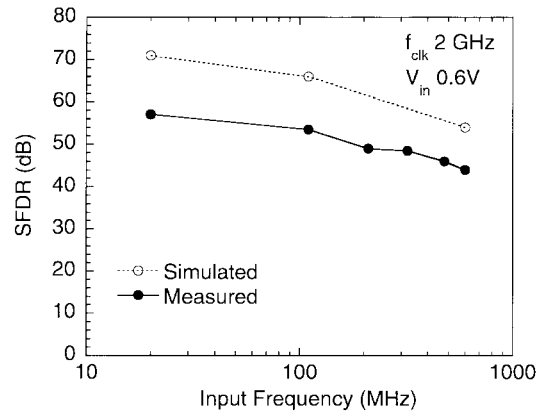


Fig. 6. Measured and simulated linearity of the sample-and-hold as a function of input frequency at 2 Gsps.

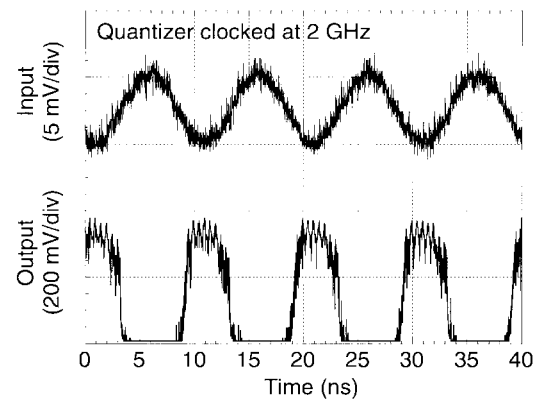


Fig. 7. Input and output waveforms of the RTD/HFET comparator at 100-MHz input and 2-GHz clock signal showing input sensitivity of 5 mV.

Shunting current around the load-RTD using an HFET-switch resets the comparator. This operation returns the load-RTD to its “prepeak” bias condition. To make the output signal amenable to data capture the reset signal is removed from the comparator output by writing the data with an inverter stage into an RTD “Goto-pair” latch [13]. The feedback source-drain shorted FET from the inverter stage to the comparator input reduces kickback onto the input node due to the switching of the load-RTD. A 50-Ω pin-driver completes the circuit.

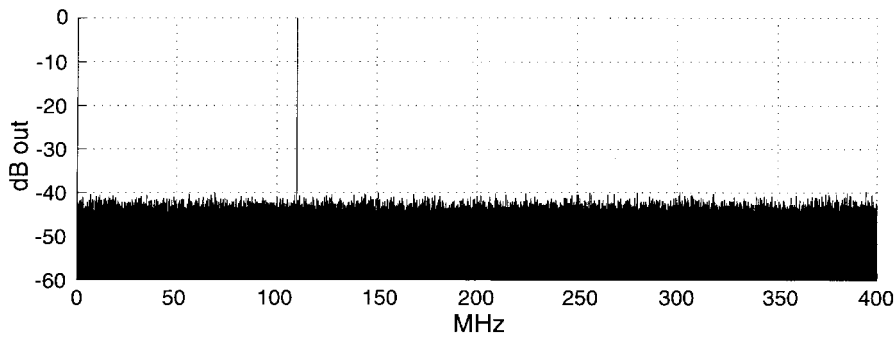


Fig. 8. Output fast Fourier transform spectrum of a single-bit comparator dither experiment for a 110-MHz single-tone input. The spurious free dynamic range is at least 40 dB.

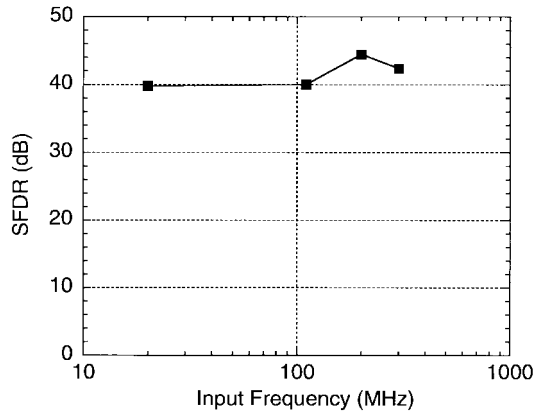


Fig. 9. Spurious free dynamic range of the single-bit comparator as a function of input frequency.

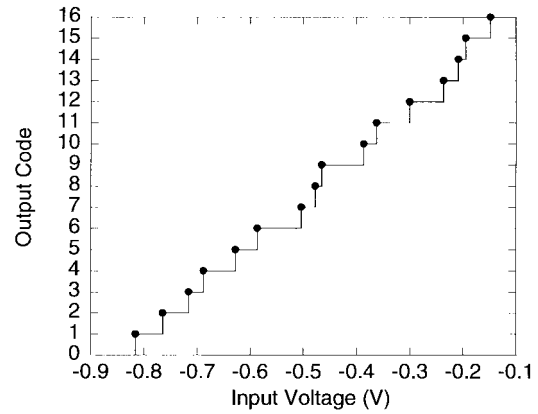
III. PROCESS

An 11-mask fabrication process produces the HFET's, RTD's, Schottky diodes, capacitors, resistors, and two interconnect levels from a single epitaxial growth. The details of the process are described in [14]. The HFET's are constructed from modulation-doped InGaAs/InAlAs heterojunctions grown by gas-source molecular beam epitaxy on 50 and 75 mm InP substrates, with a typical $f_{\tau}(f_{max})$ of 53 GHz (140 GHz) for a 0.5- μm gate length. The RTD heterostructure is located above the HFET and consists of pseudomorphic AlAs barriers and an InGaAs/InAs well designed for a peak current density of about 10 kA/cm² and a speed index of 0.1 V/ps. Passive elements are realized as 3000-Å silicon-nitride 0.2-fF/ μm^2 capacitors and 25- Ω /square NiCr resistors.

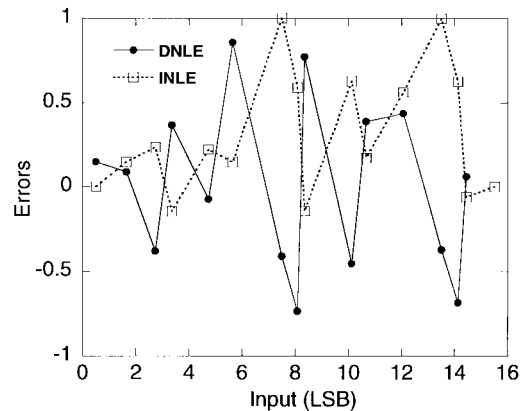
IV. RESULTS

The reticle to fabricate the ADC contains a comprehensive set of structures for testing the individual subcircuits and components. The sample-and-hold, the clock shapers, and the comparators have all been tested independently in this manner. All tests were performed on-wafer with Picoprobe multicontact wedge probes; all data reported here were acquired with a high speed Tektronix 11801A digital sampling oscilloscope.

Measured power dissipation for the subcircuits at 2 Gsps is 50 mW for the sample-and-hold, 190 mW for the clock shapers, 100 mW for the analog front end of the 16 comparators, and 470 mW for the 16 50- Ω pin-drivers, for a total power dissipation of 810 mW. Test results for the linearity



(a)



(b)

Fig. 10. Static input signal transfer function of the ADC measured at (a) 2-GHz clock input and (b) the differential (DNLE) and integral (INLE) nonlinearity errors associated with the transfer function.

as measured by the spur-free dynamic range (SFDR) of the sample-and-hold as a function of the input signal frequency are shown in Fig. 6. The measured linearity is about 10 dB less than the values predicted by SPICE simulation.

The comparators were characterized by measuring their input sensitivity and SFDR up to 3.3 Gsps. An example measurement for the input sensitivity of a single comparator is shown in Fig. 7. The input sensitivity is about 5 mV at 100-MHz input and 2-Gsps clock frequency.

Fig. 8 shows an output spectrum obtained from a single-bit quantizer for a 110 MHz single tone input combined with input noise for dithering. This measurement shows that the SFDR

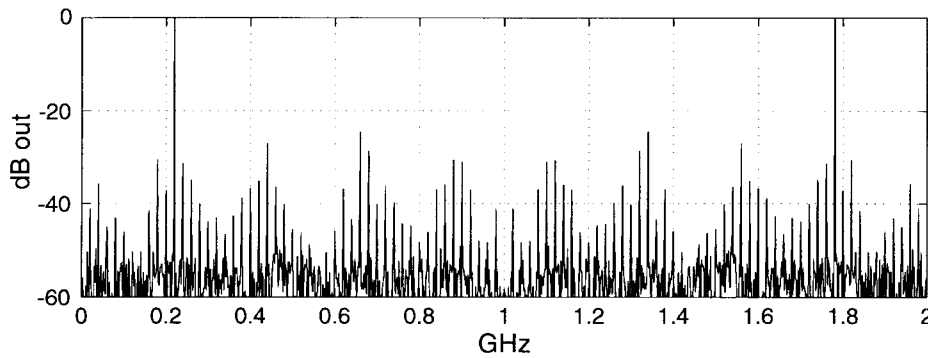


Fig. 11. Fourier transform output spectrum of the ADC for a 220-MHz single tone input at 2 Gsps.

TABLE I
MEASURED AND SIMULATED EFFECTIVE NUMBER
OF BITS AT 2 GSPS AND $0.7V_{DD}$ INPUT

Measured				
f_m (MHz)	SNR (dB)	ENOB	$2f_u$ (dB)	$3f_u$ (dB)
220	18.2	2.7	-29	-25
480	14.8	2.2	-22	-25
Simulated				
100	24.6	3.8	-38	-38
1000	24.4	3.7	-36	-36

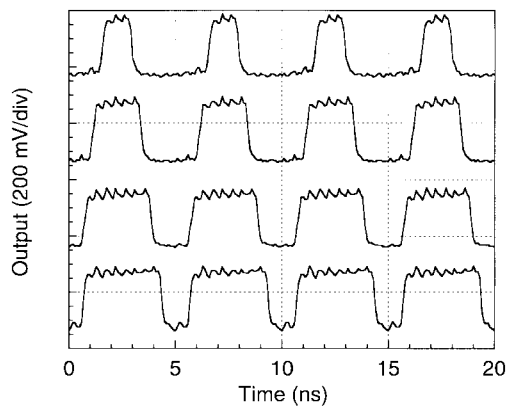


Fig. 12. Beat frequency test of the ADC. Outputs for four of the quantizers are shown for a 2.2-GHz clock and 2.0-GHz sinewave input, producing a 200-MHz beat frequency output.

of the single-bit quantizer is at least 40 dB. A summary of the SFDR as obtained from the single-bit comparator with dither is shown in Fig. 9.

The ADC static transfer function and associated differential and integral nonlinearity errors are shown in Fig. 10. The errors remain within one least significant bit but are relatively large due to the use of a single ended data path.

The dynamic ADC performance was analyzed by measuring the signal-to-noise ratio of the ADC output spectrum obtained by taking the Fourier transform of the digitized output data stream. Fig. 11 shows a typical output spectrum of the ADC for a 220-MHz single tone input at 2 Gsps. The signal-to-noise ratio obtained from the output spectrum is 18.2 dB, corresponding to 2.7 effective bits. Table I summarizes the effective number of bits (ENOB) as a function of the input signal frequency. That the effective number of bits is lower

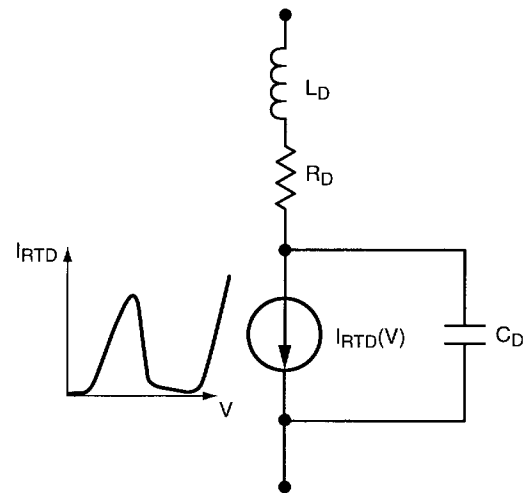


Fig. 13. Equivalent circuit representation of the RTD SPICE model.

than simulated is attributed to the sensitivity of the single-ended design to the FET threshold voltage variance and not the RTD process control which is greater than 7 bits [14]. The single-ended signal path results in comparator trip points that are *directly* dependent on the comparator input FET threshold voltage.

Finally, Fig. 12 shows the output of a beat frequency test of the ADC. A 2-GHz sinewave input is digitized at 2.2 Gsps resulting in a 200-MHz beat frequency output. This test demonstrates the ability of the sample-and-hold and quantizer circuits to operate beyond Nyquist at 2 Gsps.

V. CONCLUSION

The first monolithic flash RTD/HFET ADC has been demonstrated and characterized. The HFET/RTD ADC achieves 2.7 effective bits at 2 Gsps, and the single bit quantizer provides a very effective quantizer with a sensitivity of 5 mV and SFDR of 40 dB at 2 Gsps. The HFET-based sample-and-hold achieves better than 50-dB linearity at clock frequencies of up to 2 GHz. Performance of the IC is limited by its single-ended design. With improvements in the circuit design, e.g., a differential signal path, and process enhancements (scaling down of gate lengths from $0.5 \mu\text{m}$ to $0.1 \mu\text{m}$ and increasing the RTD current density from 10 kA/cm^2 to 50 kA/cm^2), we expect this technology to be capable of digitizing X-band signals.

APPENDIX
SPICE LARGE SIGNAL RTD MODEL DESCRIPTION

The SPICE model described here is similar to the large signal physics-based model in [10]. Departures include: an ideality or “lever” factor accounting for the voltage drop across the quantum well heterostructure relative to the applied voltage, a second resonance term which explicitly accounts for the tunneling through the second quantum well state, a capacitance model which includes a Debye, kT , screening voltage as well as a parallel capacitance related to the carrier transit time, and a series inductance [15].

The RTD is modeled as a SPICE subcircuit consisting of a nonlinear voltage dependent current source in parallel with a voltage dependent capacitor, the combination of which is in series with a resistance and an inductance as is shown in Fig. 13. The nonlinear current source represents the essential physics of the device and in combination with the series resistance represents the DC I–V characteristics of the RTD.

The nonlinear current source is a combination of three different current sources in parallel

$$I_{\text{RTD}}(V) = I_{\text{res1}}(V) + I_{\text{res2}}(V) + I_{\text{lk}}(V)$$

where V is the voltage over the nonlinear current source. The first of these terms I_{res1} represents the current through the first resonance of the RTD, the second I_{res2} represents the current through the second resonance, and the third I_{lk} represents the thermionic leakage current. The current through a resonance of the RTD is described by the expression (assuming a symmetric RTD)

$$I_{\text{res}}(V) = I_E(V) - I_E(-V)$$

with

$$I_E(V) = \frac{AJ_P}{2f} \left[1 + \frac{2}{\pi} \arctan \left(\frac{V_N - V}{\Gamma} \right) \right] \times \frac{nkT}{V_N - V_T} \ln \left[1 + \exp \left(\frac{V - V_T}{nkT} \right) \right]$$

and $f = 1 - \sqrt{2\Gamma/\pi(V_N - V_T)}$ where A is the device area, J_P the approximate peak current density, V_N the voltage at which the maximum negative differential resistance (NDR) occurs, V_T the resonance turn-on voltage, Γ the full-width at half maximum of the resonance, n a subthreshold ideality or “lever” factor, and kT the thermal voltage. The factor f is introduced so that the parameter J_P corresponds approximately to the true peak current density.

The leakage current component is given by

$$I_{\text{lk}}(V) = AJ_V \frac{\sinh\left(\frac{V}{n_V kT}\right)}{\sinh\left(\frac{V_V}{n_V kT}\right)}$$

where V_V is the valley voltage, J_V is the thermionic leakage current at V_V , and n_V is the leakage current ideality. It should be noted that most of the valley current at the first resonance is contributed by the resonance terms I_{res1} and I_{res2} .

TABLE II
RTD SPICE MODEL PARAMETERS

Parameter	Description
A	Device area
J_P	Peak current density (approximate)*
V_N	Voltage of maximum NDR*
V_T	Resonance turn-on voltage*
Γ	Full-width at half maximum of the resonance*
n	Resonance subthreshold ideality or “lever” factor*
J_V	Thermionic leakage current at V_V
n_V	Thermionic leakage current ideality
V_V	Valley voltage
C_0	Junction capacitance
ϕ	Capacitance voltage scaling factor
M	Capacitance grading coefficient
τ	Depletion layer carrier transit time
L_D	Device access inductance
R_D	Device series resistance
kT	Thermal voltage

*A separate parameter is used for each of the two resonance current terms, I_{res1} and I_{res2} .

The capacitance of the RTD is modeled as a voltage dependent capacitor in parallel with a transit time capacitance

$$C_D = AC_0 \left(1 + \frac{|V| + kT}{\phi} \right)^{-M} + \tau g$$

where C_0 is the junction capacitance per unit area, ϕ is a voltage scaling factor, M is a grading coefficient, τ is the depletion layer carrier transit time, and g is the differential conductance dI_{res}/dV of the nonlinear current source.

The RTD series resistance R_D and access inductance L_D are linear components and scale inversely with the RTD area.

A summary of the RTD model parameters is given in Table II.

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REFERENCES

- [1] K. Poulton, K. L. Knudsen, J. Kerley, J. Kang, J. Tani, E. Cornish, and M. VanGrouw, “An 8 GSa/s 8-bit ADC system,” in *Proc. Symp. VLSI Circ. Tech. Dig.*, 1997, pp. 23–24.
- [2] P. Xiao, K. Jenkins, M. Soyuer, H. Ainspan, J. Burghartz, H. Shin, M. Dolan, and D. Harame, “A 4 b 8 GSample/s A/D converter in SiGe bipolar technology,” in *IEEE Int. Solid-State Circ. Conf. Tech. Dig.*, 1997, pp. 124–125.
- [3] K. R. Nary, R. Nubling, S. Beccue, W. T. Colleran, J. Penney, and K.-C. Wang, “An 8-bit 2 Gigasample per second analog to digital converter,” in *GaAs IC Symp. Tech. Dig.*, 1995, pp. 303–306.
- [4] F. Oehler, J. Sauerer, R. Hagelauer, D. Seitzer, U. Nowotny, B. Raynor, and J. Schneider, “A 3.6 Gigasample/s 5 bit analog to digital converter using 0.3 μm AlGaAs-HEMT technology,” in *GaAs IC Symp. Tech. Dig.*, 1993, pp. 163–166.

- [5] N. Shimizu, T. Nagatsuma, T. Waho, M. Shinagawa, M. Yaita, and M. Yamamoto, "InGaAs/AlAs resonant tunneling diodes with switching time of 1.5 ps," *Electron. Lett.*, vol. 31, pp. 1695-1697, 1995.
- [6] R. C. Potter, A. Fathimulla, H. Hier, D. Shupe, J. Abrahams, C. Eichner, D. Jones, S.-J. Wei, and H. C. Lin, "A monolithic, resonant tunneling diode-based analog-to-digital converter built on InP," in *Proc. Fifth Int. Conf. Indium Phosphide and Rel. Mat.*, 1993, pp. 37-40.
- [7] S.-J. Wei, H. C. Lin, R. C. Potter, and D. Shupe, "A self-latching A/D converter using resonant tunneling diodes," *IEEE J. Solid-State Circuits*, vol. 28, pp. 697-700, 1993.
- [8] T. P. E. Broekaert, B. Brar, J. P. A. van der Wagt, A. C. Seabaugh, T. S. Moise, F. J. Morris, E. A. Beam III, and G. A. Frazier, "A monolithic 4 bit 2 Gbps resonant tunneling analog-to-digital converter," in *GaAs IC Symp. Tech. Dig.*, 1997, pp. 187-190.
- [9] T. P. E. Broekaert, "Ultrahigh speed resonant tunneling diode/transmission line clock generator and track-and-hold," in *Proc. IEEE/Cornell Conf. on Adv. Concepts in High Speed Semiconductor Devices and Circuits*, 1997, pp. 132-138.
- [10] J. N. Schulman, H. J. De-Los-Santos, and D. H. Chow, "Physics-based RTD current-voltage equation," *IEEE Electron Device Lett.*, vol. 17, pp. 220-222, 1996.
- [11] K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, *Semiconductor Device Modeling for VLSI*. Englewood Cliffs, NJ: Prentice Hall, 1993.
- [12] B. Brar, T. P. E. Broekaert, J. P. A. van der Wagt, A. C. Seabaugh, T. S. Moise, F. J. Morris, E. A. Beam III, and G. A. Frazier, "3 GHz resonant tunneling clocked comparator," in *Proc. IEEE/Cornell Conf. Adv. Concepts in High Speed Semiconductor Devices and Circuits*, 1997, pp. 28-34.
- [13] E. Goto, K. Murata, K. Nakazawa, K. Nakagawa, T. Moto-Oka, Y. Matsuoka, Y. Ishibashi, T. Soma, and E. Wada, "Esaki diode high-speed logical circuits," *IRE Trans. Electron. Comp.*, vol. 9, pp. 25-29, 1960.
- [14] A. Seabaugh, B. Brar, T. Broekaert, G. Frazier, F. Morris, P. van der Wagt, and E. Beam III, "Resonant tunneling circuit technology: Has it arrived?," in *GaAs IC Symp. Tech. Dig.*, 1997, pp. 119-122.
- [15] T. Wei, S. Stapleton, and E. Berolo, "Equivalent circuit and capacitance of double barrier resonant tunneling diode," *J. Appl. Phys.*, vol. 73, pp. 829-834, 1993.



J. Paul A. van der Wagt (M'95) received the M.S. degrees in applied physics in 1986 and in applied mathematics in 1988, both *cum laude*, from Twente University, Enschede, the Netherlands. He received the Ph.D. degree in applied physics from Stanford University, Stanford, CA, in 1994, where his doctoral research focused on the real-time detection of RHEED oscillations during MBE and fabrication and modeling of resonant-tunneling diodes.

He was at Texas Instruments, Dallas, from 1995 to 1998 as a Member of the Technical Staff engaged in the design and fabrication of quantum device circuits for ultrahigh speed analog-to-digital converters and low power memory. He joined the Rockwell Science Center, Thousand Oaks, CA, in 1998 where he is involved in high-speed mixed-signal design. He has authored or coauthored more than 20 papers and holds one U.S. patent.



Alan C. Seabaugh (S'78-M'79-SM'92) received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, in 1985.

He is a Distinguished Member of Technical Staff in the Nanoelectronics Branch of Raytheon Systems Company, Dallas, TX. He joined Texas Instrument's Central Research Laboratory in 1986. His current focus at Raytheon is on resonant tunneling analog-to-digital converters, high speed and low power circuits, and Si-based resonant tunneling. From 1979 to 1986, he was with the Electron Device Division of the National Bureau of Standards. He has authored or coauthored more than 100 papers and holds 14 U.S. patents.

Dr. Seabaugh is a member of the American Physical Society.



Tom P. E. Broekaert received the B.W.E.Ir. degree from the Vrije Universiteit Brussel, Belgium, in 1986 and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1989 and 1992 respectively.

From 1992 until 1994 he worked for Vitesse semiconductor. He joined Texas Instruments in 1994 as a Member of the Technical Staff and is presently employed by the Raytheon Systems Company, Dallas, TX, in the same position. He is presently

working on the cointegration of quantum effect devices and heterostructure field effect transistors, device modeling for SPICE, and circuit design using resonant tunneling diodes with applications toward high-speed analog-to-digital conversion and digital signal processing. He has authored or coauthored more than 30 papers.



Berinder Brar (M'96) was born in Kasauli, India. He received the Ph.D. degree in electrical engineering from the University of California, Santa Barbara, in 1995.

He is a Member of the Technical Staff in the Nanoelectronics branch of the Applied Research Laboratory, Raytheon Systems, Dallas, TX. He joined the Nanoelectronics branch in 1995 after completing his doctoral research on the hot-electron properties of InAs/AlSb heterostructure field-effect transistors.

Prior to his graduate work at University of California, Santa Barbara, he was in the Optoelectronics Department at the Rockwell Science Center where he was involved in the development of integrated optoelectronic laser drivers and receivers to implement a 16×16 fiber-optic crossbar switch. He has authored and co-authored over 50 papers.

Dr. Brar is a member of the IEEE Lasers and Electro-Optics Society, IEEE Electron Devices Society, American Physical Society, Eta Kappa Nu, and Tau Beta Pi.



Frank J. Morris (S'64-M'67) received the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, in 1968.

He is currently a Senior Member of the Technical Staff with the Nanoelectronics branch in the Raytheon TI Systems' Advanced Research Lab, Dallas, TX. He led the development for the DARPA GaAs HBT analog-to-digital converter (ADC) program that successfully fabricated the world's first GaAs 5-bit ADC. As a member of the TI's Semiconductor group he was responsible for the process

development for TI's Advanced Low Power Schottky (ALS) bipolar process. Prior to joining Texas Instruments, he was a Member of Technical Staff at Bell Laboratories in Murray Hill, NJ, where he was involved with charge-coupled-device (CCD) image sensors and silicon diode array vidicons. He has published in various professional journals and is a recipient of several patents in both the silicon and GaAs fields.

Theodore S. Moise (S'89-M'91) received the B.S. degree from Trinity College, Hartford, CT, in 1987 and the M.S. and Ph.D. degrees from Yale University, New Haven, CT, in 1988 and 1992, respectively.

He joined Texas Instruments (TI), Dallas, in 1992 as a Member of Technical Staff. He was Chairman of SPIE's Quantum Well and Superlattice Physics VI Conference. He became a Senior Member of TI's Technical Staff in 1997. Since then, he has managed the Memory Technology branch within TI's Silicon Technology Research group. He has authored or coauthored more than 40 papers.

Edward A. Beam, III (M'92) received the B.S., M.S., and Ph.D. degrees in materials science from Carnegie-Mellon University, Pittsburgh, PA, in 1984, 1986, and 1989, respectively.

He is with TriQuint Semiconductor-Texas, Dallas, where since January 1998 he has been responsible for III-V materials development activities in the Research and Development Center for Excellence. He previously occupied this position with Raytheon TI Systems. From 1989 to 1996, he was a Member of Technical Staff in the Materials Science Laboratory of Texas Instruments.

Gary A. Frazier received the B.S. degree in electrical engineering from the University of Maryland, College Park, in 1975 and the Ph.D. degree in physics from the University of Texas at Dallas in 1982.

He is Manager of the Nanotechnology Branch of the Applied Research Laboratory of Raytheon Systems Company, Dallas, TX. Recently at Texas Instruments and Raytheon, he has managed multiple programs to develop quantum effect devices, circuits, and modeling tools for advanced signal processing applications. He holds 27 U.S. patents on nanoelectronics, neural networks, computer architecture, lithography, and fiber optics.