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## TUNNEL DIODE/TRANSISTOR DIFFERENTIAL COMPARATOR

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A new tunnel diode/transistor circuit topology is reported, which both increases speed and reduces power in differential comparators. This circuit topology is of special interest for use in direct digital synthesis applications. The circuit topology can be extended to provide performance improvements in high speed logic and signal processing applications. The circuits are designed based on InP/GaAsSb double heterojunction bipolar transistors and AlAs/InGaAs/AlAs resonant tunneling diodes. A self-aligned and scalable fabrication approach using nitride sidewalls and chemical mechanical polishing is outlined.

*Keywords:* Differential comparator; flip-flop; tunnel diode; resonant tunneling diode; heterojunction bipolar transistor; nitride sidewall; chemical mechanical polishing.

### 1. Introduction

As minimum feature sizes are reached in transistor technologies, circuit performance can be expected to saturate. Therefore, it is important to find new ways to augment the performance of integrated circuit technology. Integrated tunnel diodes enable design options which can result in a decrease in power dissipation and an increase in speed and function per area.<sup>1</sup>

Since 1957, the tunnel diode has been widely investigated for high-speed circuit applications, due to its intrinsic high switching speed, and its “N-shaped” current-voltage ( $I-V$ ) characteristic featuring negative differential resistance (NDR).<sup>2,3</sup> Today, methods for integrating tunnel diodes with transistors in compound semiconductor technologies are well known.<sup>4,5,6</sup> In silicon technology both Si and SiGe  $p^+n^+$  tunnel diodes have been fabricated using CMOS-compatible processes.<sup>7,8</sup> Monolithic integration of a Si-based tunnel diode and a heterojunction bipolar transistor (HBT) have also been demonstrated.<sup>9</sup>

In this paper, we report on a circuit topology, utilizing high speed tunnel diodes integrated with transistors to lower the static power dissipation in a differential comparator and simultaneously increase the circuit speed. A novel scalable fabrication approach using nitride sidewalls and chemical mechanical polishing is also outlined for fabricating this tunnel diode/transistor (TDT) differential comparator.

2 *Q. Liu et al.*

## 2. Circuits Design

The schematic of the TDT differential comparator is shown in Fig. 1(a). Two tunnel diode pairs,  $D_1$ - $D_3$  and  $D_2$ - $D_4$ , are connected to the outputs of the differential pair  $Q_1$  and  $Q_2$ . Emitter followers  $Q_3$  and  $Q_4$  are used to buffer the output signal.

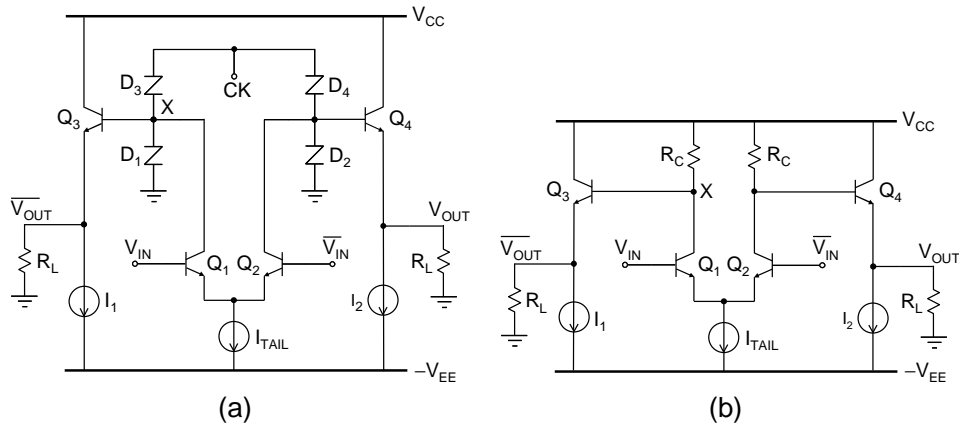


Fig. 1. Schematic diagrams of (a) tunnel diode/transistor (TDT) and (b) conventional bipolar transistor differential comparator.

When the clock is at a low level, the tunnel diode pair is in a monostable state. In this state, no matter what the applied input signal, the output voltage is low. When the clock switches to a high level, the tunnel diode pair switches to a bistable state. The output voltage latches to either a high or low voltage state, determined by the tunnel diode peak currents and the transistor collector current occurring at the rising edge of the clock. The peak currents,  $I_{P3}$  and  $I_{P4}$ , of diodes,  $D_3$  and  $D_4$ , are designed to be greater than the peak currents,  $I_{P1}$  and  $I_{P2}$ , of diodes,  $D_1$  and  $D_2$ , with the following relationships  $I_{P3} < I_{P1} + I_{TAIL}$  and  $I_{P4} < I_{P2} + I_{TAIL}$ . If the input to transistor  $Q_1$  is low, the tail current,  $I_{TAIL}$ , flows through transistor  $Q_2$ . When the clock switches from low to high, the output voltage at node  $X$  switches to the high level, because diode  $D_1$  has a smaller peak current and switches first. If, on the other hand, the input to transistor  $Q_1$  is high, the tail current,  $I_{TAIL}$ , flows through  $Q_1$ . When the clock switches from low to high, the output voltage at node  $X$  remains low, because  $I_{P3} < I_{P1} + I_{TAIL}$  and diode  $D_3$  switches instead of  $D_1$ . This circuit functions as an edge-triggered return-to-zero (RZ) D flip-flop with complementary input and output.

The TDT circuit, Fig. 1(a), has smaller output open-circuit time constant of the differential pair and faster switching speed than a conventional transistor-only current-mode-switching differential amplifier,<sup>10</sup> Fig. 1(b). In transistor-only comparator circuits, speed improvements are usually obtained by increasing the tail

current and decreasing the pull-up collector resistor. The tunnel diodes enable the differential pair current-switching at a lower tail current than the transistor-only differential pair. The tunnel diodes, therefore, lower the static power dissipation and simultaneously increase the circuit speed.<sup>10</sup>

### 3. Direct Digital Synthesis

This TDT differential comparator is of special interest for use as a switching element in direct digital synthesis applications. A recently developed algorithm, based on list decoding, for DDS provides an improved signal-to-noise ratio (SNR), compared with conventional  $\Sigma\Delta$  approaches.<sup>11,12</sup> In both list decoding and  $\Sigma\Delta$  approaches, a specially designed digital bitstream is output through a single-bit digital-to-analog converter (DAC) and a reconstruction filter to form the analog signal. The Fourier spectrum of the desired signal is embedded in the pattern of the bitstream. A high-speed and high-linearity single-bit DAC is required to achieve high SNR, because the severe distortion of the output signal is usually generated from the nonlinearity of the DAC. The circuits, proposed in this paper, are designed for use in such DDS applications.

To compare the power dissipation and linearity of both TDT and transistor-only circuits, we simulated both circuits (Fig. 1) in Agilent ADS. The transistor SPICE model we used in the simulation is for a high speed InP-based heterojunction bipolar transistor (HBT) with  $f_T/f_{MAX}$  of 140/340 GHz. Broekaert's RTD model<sup>13</sup> is used for an InP-based RTD with a speed index of 316 mV/ps. The input bitstream has a 100 Gbps bit rate, and an amplitude of 400 mV with rising and falling time of 1 ps. The synthesized passband signal frequency is approximately 37.3 GHz. The simulated spectrum of the synthesized signal in both TDT and transistor-only circuits is shown in Fig. 2. Approximately 60 dBc spur free dynamic range (SFDR) is obtained for both circuits, showing these two circuits have approximately the same linearity. The power dissipation of both circuits are also compared and shown in Table 1. The power dissipation is reduced by approximately  $4\times$  in the TDT differential pair and  $1.6\times$  in the full TDT circuit.

Table 1. Comparison of the power dissipation in the TDT and conventional HBT differential comparators of Fig. 1.

Power dissipation	TDT (mW)	HBT (mW)
Differential pair	3	12.5
Clock	0.5	0
Emitter followers	25.5	34
Total	29	46.5

4 *Q. Liu et al.*

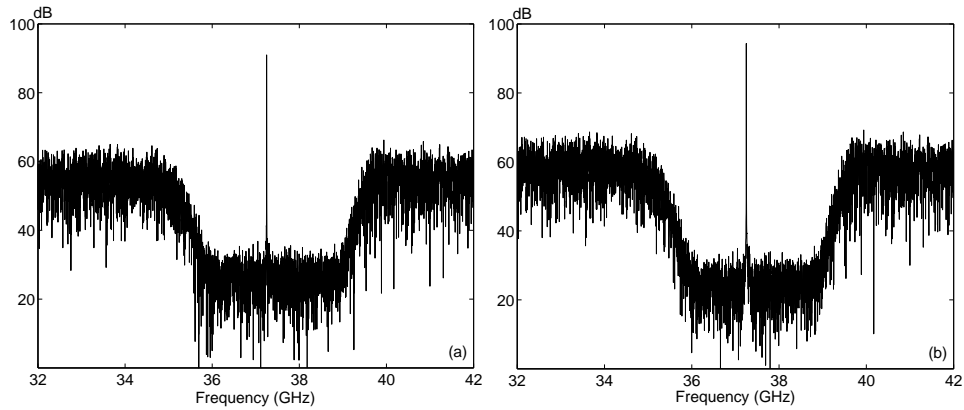


Fig. 2. Simulated output spectrum of the synthesized passband signal for (a) tunnel diode/transistor and (b) transistor-only differential comparator showing 60 dBc SFDR around 37.3 GHz. This simulation uses high speed InP-based HBT and RTD models.

#### 4. Fabrication Approach

A fabrication approach using AlAs/InGaAs/AlAs RTDs and InP/GaAsSb HBTs is described. The material layer structure is grown by molecular beam epitaxy (MBE). The energy band diagram of the structure is shown in Fig. 3.

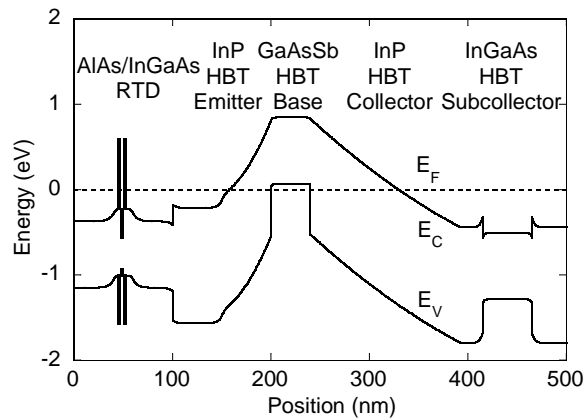


Fig. 3. Simulated energy band diagram of InP-based RTD/HBT structure, computed using the Schrödinger-Poisson solver, BandProf, of W. R. Frensley.

The process uses silicon nitride sidewalls and chemical mechanical polishing (CMP) to get scalable self-aligned contacts for the RTD and HBT. A schematic cross section of the RTD/HBT fabrication process is shown in Fig. 4. The RTD and

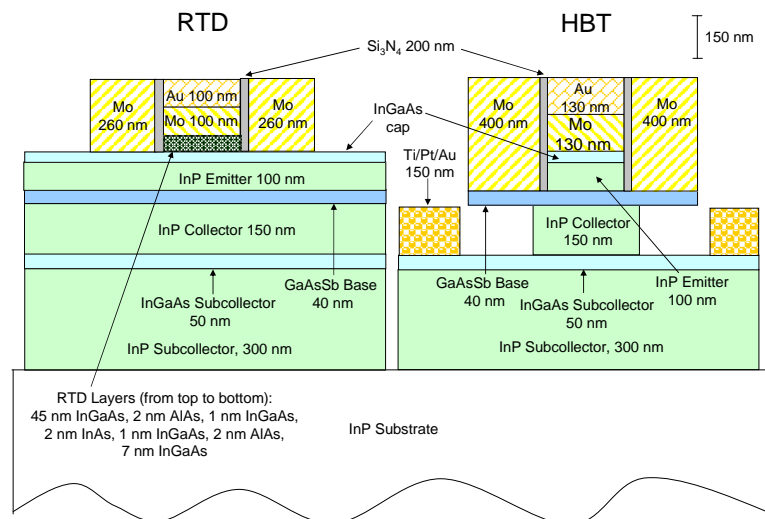


Fig. 4. Integrated resonant tunneling diode and heterojunction bipolar transistor fabrication approach, drawn to scale in the  $y$ -direction.

HBT emitter contacts are formed by lift-off. After defining the RTD and HBT mesas using reactive ion etching (RIE), silicon nitride sidewalls are formed by depositing a plasma-enhanced chemical vapor deposition (PECVD)  $\text{Si}_3\text{N}_4$  film, followed by an RIE process using  $\text{CHF}_3$ . A blanket deposition of Mo is used to form self-aligned RTD collector and HBT base contacts. Chemical mechanical polishing is employed to polish the molybdenum and electrically isolate the HBT emitter and base contacts, as well as the RTD emitter and collector contacts. The isolation is provided by the silicon nitride sidewall. An RIE process with  $\text{CF}_4/\text{O}_2$  is used to etch the molybdenum and define the RTD collector and HBT base contacts. The HBT collector contact is formed by lift-off. The silicon nitride sidewalls can be scaled to minimize the HBT base resistance and RTD series resistance and enhance the speed of the devices.

## 5. Conclusions

A new tunnel diode/transistor differential comparator is described for lowering power dissipation while simultaneously increasing speed. A fabrication approach for InP/GaAsSb HBTs and AlAs/InGaAs/AlAs RTDs using a novel scalable process, featuring nitride sidewalls and chemical mechanical polishing is also outlined. This circuit topology can be applied to all materials systems which can integrate a resonant or Esaki tunnel diode and therefore is applicable to Si and SiGe BiCMOS technologies, GaAs, InP, InAs, and GaN-based transistor technologies.

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