

# Partially Depleted SOI MOSFETs Under Uniaxial Tensile Strain

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**Abstract**—The effects of tensile uniaxial strain on the DC performance of partially-depleted silicon-on-insulator n and p-channel MOSFETs as a function of orientation and gate length are reported. The drain current of the n-MOSFETs increases for both longitudinal and transverse strain orientations with respect to the current flow direction. In the n-MOSFET, longitudinal strain provides greater enhancement than transverse strain. In contrast, for p-MOSFETs, longitudinal strain decreases the current while transverse strain increases the drain current. The magnitude of the fractional change in drain current decreases as gate length is reduced from 20 to 0.35  $\mu\text{m}$ . These phenomena are consistent with those of bulk silicon MOSFETs and are shown to be qualitatively correlated with the piezoresistance coefficients of the Si inversion layer. Analysis of the linear drain current versus gate voltage characteristics shows that the threshold voltage is independent of strain while the change in drain current tracks with the change in effective electron and hole mobility. Closer examination shows that as the gate length is reduced from 20 to 0.35  $\mu\text{m}$ , the relative increase in low-field electron and hole mobility is constant for transverse strain and generally decreases with gate length for longitudinal strain.

**Index Terms**—Mechanical stress, mobility enhancement, MOSFET mobility, partially depleted silicon-on-insulator (SOI) MOSFET, strained-Si.

## I. INTRODUCTION

IT IS WIDELY accepted that mechanical stress changes the drain current of n- and p-channel MOSFETs through a change in the electron and hole mobility. This stress is typically introduced by lattice mismatching of heteroepitaxial layers [1]–[4], or by polysilicon or nitride depositions in conjunction with implantation and rapid thermal processing [5]–[8], or, upon completion of the device process, by bending [9]–[15]. With the exception of [10] and [13], prior measurements of uniaxial bending have been on bulk MOSFETs. In this paper we report a detailed electrical characterization of partially depleted silicon-on-insulator (PD-SOI) n- and p-MOSFETs under tensile uniaxial strain. Our results extend the results of Hamada *et al.* [11] to PD-SOI MOSFETs and further show that the change in low field mobility with strain is independent of gate length for applied strain perpendicular to the current flow direction.

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## II. EXPERIMENTS

The devices measured in this work were fabricated using Honeywells 0.35  $\mu\text{m}$  technology with gate lengths ranging from 0.35 to 20  $\mu\text{m}$ . Each device had a gate oxide thickness of 8 nm, buried oxide thickness of approximately 400 nm, and a silicon-on-insulator (SOI) layer of approximately 200 nm. Transistors were oriented in the conventional way with the drain current flowing in the  $\langle 110 \rangle$  direction on (100) substrates. The test die ( $20 \times 16$  mm) was thinned to approximately 250  $\mu\text{m}$ . We designed a three-point bending apparatus to apply and remove the tensile mechanical stress, as shown in Fig. 1. The stainless steel apparatus consists of a cylindrical stainless steel base with a thickness of 6 mm, threaded along its outer diameter at 28 threads/inch. A piezoresistance Sensotec Model 13/2443-03 load cell with capacity of 1500 g and subgram resolution is recessed into the base. A second bending plate with a diameter of 40 mm and a rounded bending ridge, approximately 2 mm in cross section, is mounted over the load cell and aligned by four guide posts (two are shown) to the base. A cylindrical stressor plate is used to apply force to the two ends of the SOI wafer. The spacing between the two pressure points is 10 mm. A cylindrical threaded cap is used to set the applied stress. The apparatus is held by vacuum to the chuck of a Cascade Microtech 11 861 probe station. Devices were probed through the opening in the threaded cap and measured using an Agilent 4155B semiconductor parameter analyzer.

The surface strain  $\varepsilon$ , is calculated [16] from  $\varepsilon = 3aF/bt^2E$ , where  $a$  is the shortest distance between the bending ridge and the test device,  $F$  is the measured force from the load cell,  $b$  is the chip width,  $t$  is the wafer thickness, and  $E$  is the Youngs modulus of silicon ( $115 \times 10^9$  Pa).

## III. RESULTS AND ANALYSIS

Devices with gate lengths from 0.35 to 20  $\mu\text{m}$  were characterized. Representative n- and p-MOSFET characteristics both with and without transverse strain are shown in Fig. 2. Open symbols are for measurement of the unstrained device; closed solid symbols indicate the device in the strained condition. We see that transverse ( $\perp$ ) tensile strain, perpendicular to the current flow direction, increases the drain current for both low, and high drain-source electric fields, for both n- and p-channel devices, and for all gate lengths.

We observe no irreversible changes or hysteresis in the device characteristics for the range of strain we have applied, which is up to approximately 0.16%. Fig. 3 shows the relative changes in the low-field linear drain current and high-field saturation

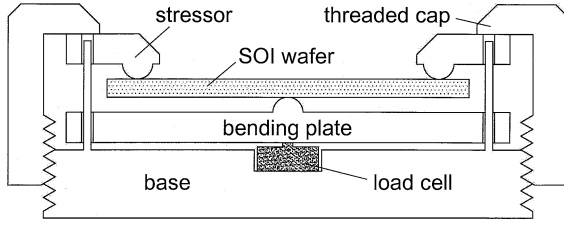
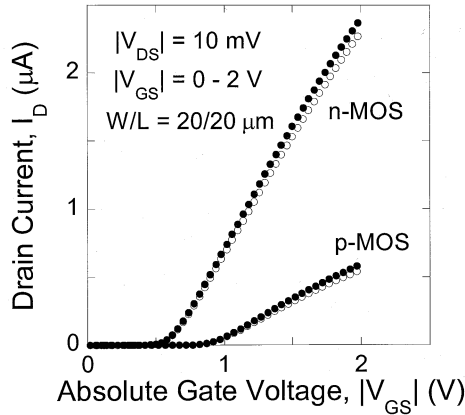
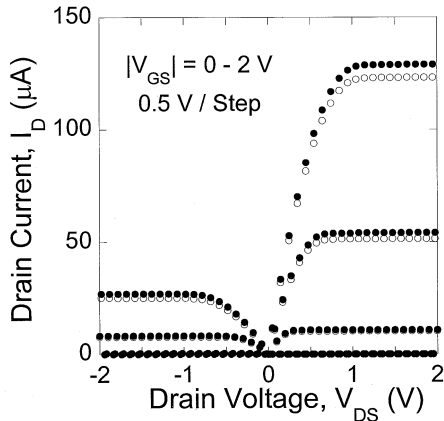


Fig. 1. Schematic diagram of the three-point bending apparatus designed for our measurements. The apparatus was machined from stainless steel; its cylindrical geometry makes it suitable for vacuum attachment to the wafer chuck of a Cascade Microtech 11 861 probe station, which enables probing through the open top.



(a)

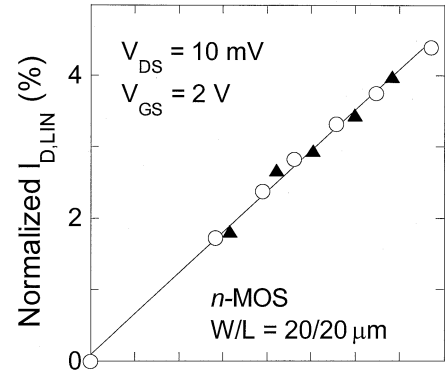


(b)

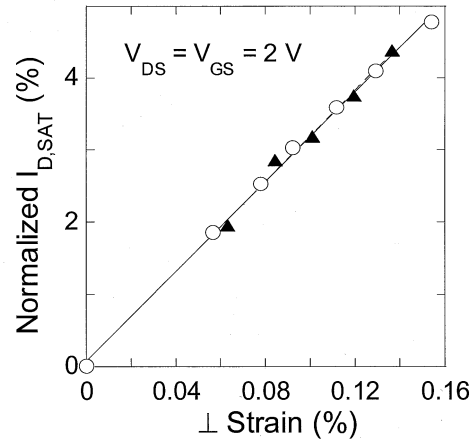
Fig. 2. Measured (a)  $I_D$  versus  $V_{GS}$  and (b)  $I_D$  versus  $V_{DS}$  for n- and p-MOSFETs before (open symbols) and after (solid symbols) uniaxial transverse tensile strain, 0.154% for the n-MOS, and 0.124% for the p-MOS transistors.

drain current versus transverse strain for a gate width to gate length ratio,  $W/L = 20/20 \mu\text{m}$ . The open circles denote the increasing strain characteristic and the triangles indicate the decreasing strain characteristic. These points nearly follow each other on a straight line indicating that the strain is elastic up to 0.16% in our SOI transistors.

A change in drain current with strain can result from changes in the effective mobility and effective channel charge density, arising from strain-induced changes in the energy band-structure, interface roughness, and/or interface charge densities. First



(a)



(b)

Fig. 3. (a) Normalized change in the linear drain current  $I_{D,LIN}$  and (b) saturated drain current  $I_{D,SAT}$  versus transverse strain ( $\perp$ ) for the n-MOSFET of Fig. 2. The open circles denote the increasing strain characteristic; the solid triangles indicate the decreasing strain characteristic.

we consider the effect of strain on the effective electron and hole mobility  $\mu_{\text{eff}}$  obtained from the following equation at low (10 mV) drain-source bias:

$$\mu_{\text{eff}} = \frac{I_D}{V_{DS} C_{OX} (V_{GS} - V_T) (W/L)}. \quad (1)$$

The threshold voltage,  $V_T$ , is linearly extrapolated from the point of maximum transconductance [17], and  $C_{OX}$  is the computed gate oxide capacitance per unit area. This  $\mu_{\text{eff}}$  extraction method is not as accurate as the split  $C-V$  method [18], especially in the low gate bias region because of the inaccuracy of the calculated inversion carrier density, however it is still useful for comparisons. The effective vertical field is calculated from using  $E_{\text{eff}} = (V_{GS} + V_T)/6T_{OX}$  for n-channel, and  $E_{\text{eff}} = (V_{GS} + 1.5V_T)/7.5T_{OX}$  for p-channel devices [19]. Here,  $T_{OX}$  is the gate oxide thickness.

Fig. 4 shows the extracted electron and hole effective mobility versus effective vertical field for  $W/L = 20/20 \mu\text{m}$  under transverse strain. From Fig. 4, we see that both electron and hole effective mobility increase monotonically with the transverse strain. The mobility in this field range is determined by phonon scattering [20], thus the enhanced mobility suggests a reduction in phonon scattering and effective mass because of the splitting of the energy band degeneracy.

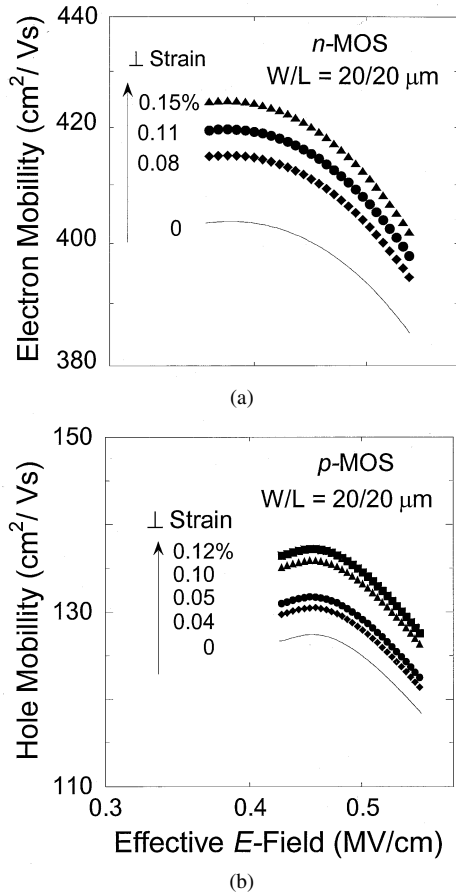


Fig. 4. (a) Extracted electron and (b) hole effective mobility ( $\mu_{\text{eff}}$ ) versus effective vertical field for the  $n$ -MOSFET under transverse ( $\perp$ ) strain.

Fig. 5 summarizes the relative changes in the low-field linear drain current,  $I_{D,\text{LIN}}$ , and high-field saturation drain current,  $I_{D,\text{SAT}}$ , with longitudinal tensile strain ( $//$ ), oriented parallel to the current flow direction, and transverse tensile strain, ( $\perp$ ), applied perpendicular to the current flow direction, for  $n$ - and  $p$ -MOSFETs. Both long-channel ( $L = 20 \mu\text{m}$ , open and solid circles) and short-channel ( $L = 0.35 \mu\text{m}$ , open and solid triangles) gate-length devices are included in Fig. 5. From Fig. 5(a), it is clear that longitudinal strain augments the drain current of the  $n$ -MOSFETs but decreases that of the  $p$ -channel devices. This strain-induced current surge is larger in the long-channel devices than in short ones. By contrast, transverse strain increases the drain currents of both types of devices, with the current increase in the  $p$ -MOSFETs being the greatest. The normalized drain current change as a function of longitudinal and transverse strain, for both  $n$ - and  $p$ -channel PD-SOI MOSFETs are consistent with those reported previously in bulk MOSFETs [9], [11]. We note that the magnitude of longitudinal strain we have applied is much less than that of the transverse strain owing to the location of the devices near the wafer edge where there is a lower applied strain.

The observed dependence of drain current on strain direction correlates well with the piezoresistance coefficients of  $n$  [16] and  $p$  [21] silicon inversion layers; see Table I. For  $n$ -MOSFETs, the piezoresistance coefficients are negative for both longitudinal and transverse strains resulting in a resistance decreases with stress. The absolute value of the longitudinal coefficient is larger so that it enhances the drain current more than the trans-

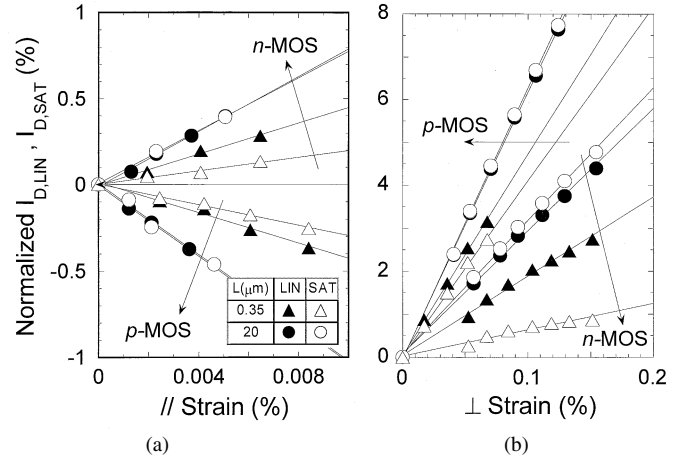


Fig. 5. Relative change in the linear current,  $I_{D,\text{LIN}}$  ( $|V_{\text{GS}}| = 2 \text{ V}$ ,  $|V_{\text{DS}}| = 10 \text{ mV}$ ) and saturation current  $I_{D,\text{SAT}}$  ( $|V_{\text{GS}}| = |V_{\text{DS}}| = 2 \text{ V}$ ) versus (a) longitudinal  $//$  and (b) transverse  $\perp$  tensile uniaxial strain for both long ( $W/L = 20/20 \mu\text{m}$ ) and short ( $W/L = 5/0.35 \mu\text{m}$ ) channel PD-SOI MOSFETs.

verse strain. For  $p$ -channel devices, the longitudinal coefficient is positive while the transverse one is negative. The sign and magnitude of the piezoresistance coefficients are attributed to the changes of carrier populations of different valleys and intervalley scattering with stress [21].

One can show that the piezoresistance coefficients can be approximated by the formula  $\Delta I_D/I_D \varepsilon E$ , where  $\varepsilon$  is the strain and  $E$  is the Youngs modulus defined previously. From our data in Fig. 5 for both long ( $20 \mu\text{m}$ ) and short ( $0.35 \mu\text{m}$ ) channel devices, we have extracted the piezoresistance coefficients and include them in Table I. Our coefficients are in fairly good agreement with those reported by Dorda [16] and Coleman, Bate, and Mize [21]. We note that the short ( $0.35 \mu\text{m}$ ) channel device has smaller piezoresistance coefficients than the long ( $20 \mu\text{m}$ ) one.

From Fig. 5, we also see that the normalized changes of  $I_{D,\text{LIN}}$  (solid symbols) and  $I_{D,\text{SAT}}$  (open symbols) are almost equal for the long-channel devices; the change in  $I_{D,\text{LIN}}$  is larger than that of  $I_{D,\text{SAT}}$  for short-channel devices. This result is reasonable because  $\Delta I_{D,\text{LIN}}$  (the relative change in  $I_{D,\text{LIN}}$ ) is related to the change in effective mobility,  $\Delta \mu_{\text{eff}}$ , while  $\Delta I_{D,\text{SAT}}$  is determined by the change in near-source carrier injection velocity,  $\Delta \nu_e$ , for short-channel devices. The change in carrier injection velocity with strain is smaller than the change in effective mobility for short-channel devices [15]. The ratio,  $\Delta \nu_e/\Delta \mu_{\text{eff}}$ , is much larger for  $p$ -MOSFETs than for  $n$ -channel devices, which implies that holes are less affected by nonequilibrium transport than electrons.

In order to quantify the change in a device property with strain, we define several normalized “gauge” factors, similar to Lochtefeld and Antoniadis [15]. First, we define two drain current gauge factors,  $\Gamma_{\text{LIN}}$  and  $\Gamma_{\text{SAT}}$ , to characterize the relative changes in low-field linear drain current and high-field saturation drain current with strain, respectively. Fig. 6 shows the linear and saturation current gauge factors’ dependence on the gate length for transverse and longitudinal strain for  $n$ -channel devices. It is evident that the magnitudes of  $\Gamma_{\text{LIN}}$  and  $\Gamma_{\text{SAT}}$  decrease generally with gate length, which is again similar to that of bulk MOSFETs [11]. Hamada *et al.* [11]

TABLE I  
PIEZORESISTANCE COEFFICIENTS ( $\times 10^{-11} \text{ Pa}^{-1}$ ) FOR SILICON INVERSION LAYER ELECTRONS [16] AND HOLES [21] UNDER // AND  $\perp$  STRAIN IN THE (110) DIRECTION ON THE (100) PLANE. THE CALCULATED PIEZORESISTANCE COEFFICIENTS FROM THIS WORK ARE ALSO SHOWN FOR BOTH LONG-(20  $\mu\text{m}$ ) AND SHORT-(0.35  $\mu\text{m}$ ) CHANNEL DEVICES

L ( $\mu\text{m}$ )	carrier	//	$\perp$	reference
20	electron	-70	-25	this work
	hole	89	-54	
0.35	electron	-39	-16	
	hole	38	-41	
40	electron	-47	-22	Dorda
2290	hole	75	-53	Coleman

attributed this dependence to the surface stress distribution for different gate-length devices. They found that shorter devices exhibited a lower channel surface stress compared with longer ones. The ratio of  $\Gamma_{\text{LIN}}(\text{//})/\Gamma_{\text{LIN}}(\perp)$  is a measure of the relative strength of the strain effect versus orientation. We find that this ratio is relatively insensitive to gate length for n-MOSFETs and that the value, 2.45, correlates approximately with the ratio of the piezoresistance coefficients for electron inversion layer,  $47/22 = 2.14$ . The corresponding ratio of high-field current gauge factor,  $\Gamma_{\text{SAT}}(\text{//})/\Gamma_{\text{SAT}}(\perp)$ , increases with the shrinking of gate length and reaches approximately 3.3 for an  $L = 0.35 \mu\text{m}$  n-MOSFET; this shows that the longitudinal strain is more effective than transverse strain for augmenting the drive current of short n-MOSFETs.

Fig. 6(c) shows that the ratio,  $\Gamma_{\text{SAT}}/\Gamma_{\text{LIN}}$ , decreases with gate length and is only 0.32 (0.44) for 0.35  $\mu\text{m}$  n-channel transistors under transverse (longitudinal) strain. This means a 100% increase of linear current will result in only a 32% (44%) increase of saturation current for transverse (longitudinal) strain. This ratio is somewhat lower than expected when compared to the ratio  $R_{\nu\mu} = \Delta\nu_e/\Delta\mu_{\text{eff}}$ , the change in near source electron velocity divided by the change in low-field effective mobility [15]. This low ratio is possibly an indication of self-heating effect in our PD-SOI devices. Shorter channel devices suffer more from this effect because of their larger current.

A similar gate length dependence of  $\Gamma_{\text{LIN}}$  and  $\Gamma_{\text{SAT}}$  is also observed in p-MOSFETs with // and  $\perp$  strain, as is shown in Fig. 7(a) and (b), respectively. The gauge factors are negative for // strain, which is consistent with the piezoresistance coefficient in Table I. Compared with n-MOSFETs, Fig. 7 shows that the ratio  $\Gamma_{\text{SAT}}/\Gamma_{\text{LIN}}$  is much larger and has a weaker dependence on gate length for p-channel devices.

We have closely examined the low-field characteristics of the transistors, following the equations of Cristoloveanu *et al.* [22] to obtain the low-field mobility,  $\mu_0$ , (the mobility when  $V_{\text{GS}} = V_T$ ), threshold voltage,  $V_T$ , and mobility attenuation coefficient,  $\theta$ , from the  $I_D$ - $V_{\text{GS}}$  characteristic at low drain-source bias,  $|V_{\text{DS}}| = 10 \text{ mV}$

$$I_d = \frac{W}{L_{\text{eff}}} \mu_0 C_{\text{OX}} \frac{(V_{\text{GS}} - V_T)V_{\text{DS}} - \frac{1}{2}V_{\text{DS}}^2}{1 + \theta(V_{\text{GS}} - V_T)} \quad (2)$$

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \theta(V_{\text{GS}} - V_T)} \quad (3)$$

$$\theta = \theta_0 + R_{\text{SD}} C_{\text{OX}} \mu_0 W / L_{\text{eff}}. \quad (4)$$

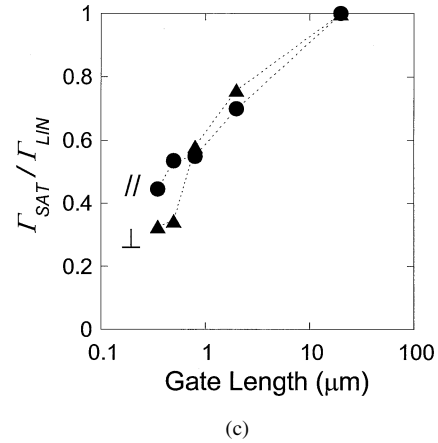
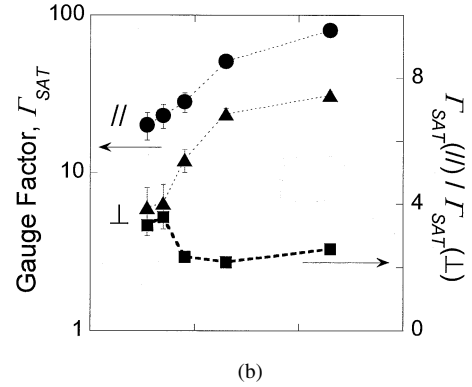
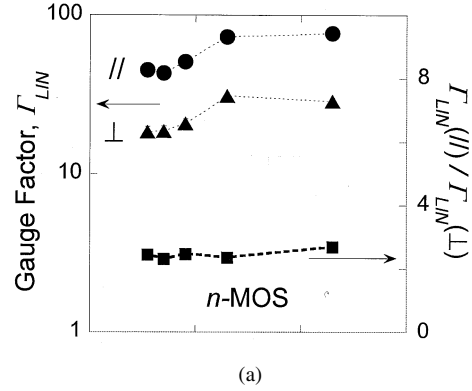


Fig. 6. Gauge factors  $\Gamma_{\text{LIN}}$  and  $\Gamma_{\text{SAT}}$ , defined as the change in the normalized, low-field, linear drain current  $I_{D,\text{LIN}}$ , and high-field, saturated drain current  $I_{D,\text{SAT}}$ , respectively, with uniaxial strain versus gate length for n-MOSFETs under longitudinal (//) and transverse uniaxial strain ( $\perp$ ). The gauge ratios are used to compare (a) // and  $\perp$  transport at low field, (b) // and  $\perp$  transport at high field, and (c) high and low field transport for both // and  $\perp$  transport.

Here,  $L_{\text{eff}}$  is the effective channel length and  $R_{\text{SD}}$  is the source-drain series resistance. Fig. 8 gives an example fit of the linear drain current vs gate-source voltage for  $L = 0.35 \mu\text{m}$  in an n-channel MOSFET. The dots are the measurements and the line denotes the fit using (2), from which we get  $\mu_0$ ,  $V_T$ , and  $\theta$ .

Using the extracted parameters from (2), we show in Fig. 9 the changes in  $\mu_0$ ,  $V_T$ , and  $\theta$  with strain. These results are also typical across gate length. We can see  $\mu_0$  increases linearly with the strain and  $V_T$  remains almost constant (less than 0.2% variation). The mobility degradation factor,  $\theta$ , increases almost linearly with strain. From (4), the overall effect of strain on  $\theta$  is determined by both the changes in  $R_{\text{SD}}$  and  $\mu_0$ . For n-type de-

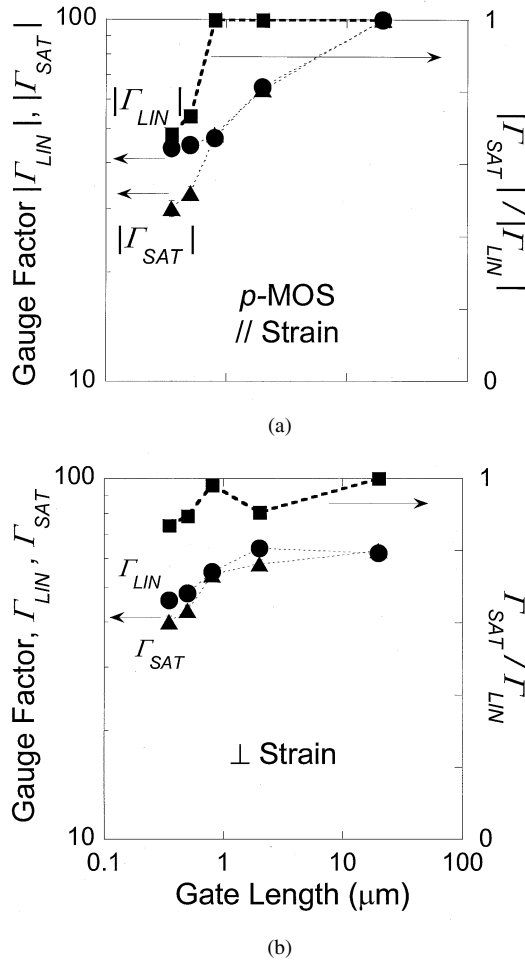


Fig. 7. (a) Low- and high-field gauge factors  $\Gamma_{LIN}$  and  $\Gamma_{SAT}$ , for p-MOSFETs with // and (b)  $\perp$  strain orientations. The gauge factors with // strain are negative for p-channel devices. The gauge ratios compare (a) high and low field transport for // strain and (b) high and low field transport for  $\perp$  strain.

vices under transverse strain,  $R_{SD}$  decreases due to the piezoresistance of the  $n^+$  source/drain regions and  $\mu_0$  increases linearly, but the change in  $R_{SD}$  is very small because the high doping concentrations in the source/drain regions results in a lower piezoresistance coefficient and the change in source/drain resistivity only partially contributes to the total  $R_{SD}$  [15]. As a result, we observe that the mobility attenuation coefficient,  $\theta$ , increases with strain in Fig. 9(c).

Similarly, we can analyze  $\theta$  changes for other circumstances. For both n- and p-channel transistors, the extracted threshold voltage  $V_T$  is constant within our experimental uncertainty under longitudinal and transverse strain, although it is theoretically expected [23] to decrease with strain for n-MOSFETs due to the lowering of the two conduction band ellipsoids with their principle revolution axis perpendicular to the  $\text{SiO}_2/\text{Si}$  interface. The reduced band bending required at inversion makes  $V_T$  lower with the application of strain, similar to the strained Si/SiGe MOSFET. The strain magnitude is so small here that we do not detect any variation of  $V_T$  with strain. Since the threshold voltage is constant, changes in the linear current  $I_{D,LIN}$  and linear current gauge factor  $\Gamma_{LIN}$  are almost completely due to the variation of effective mobility  $\mu_{eff}$ . Fig. 9(d) supports this assertion by comparing the changes in

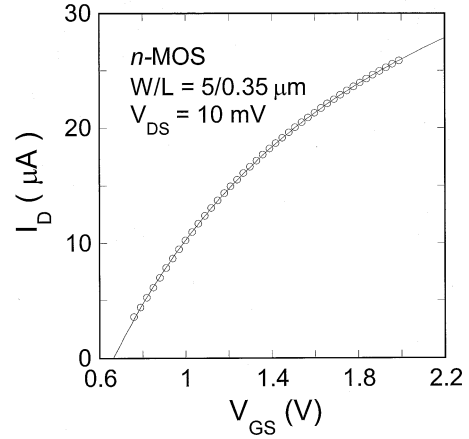


Fig. 8. Measured  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 10$  mV for the PDSOI n-MOSFET. The circles are the experimental data, and the line is obtained from curve fitting of (3).

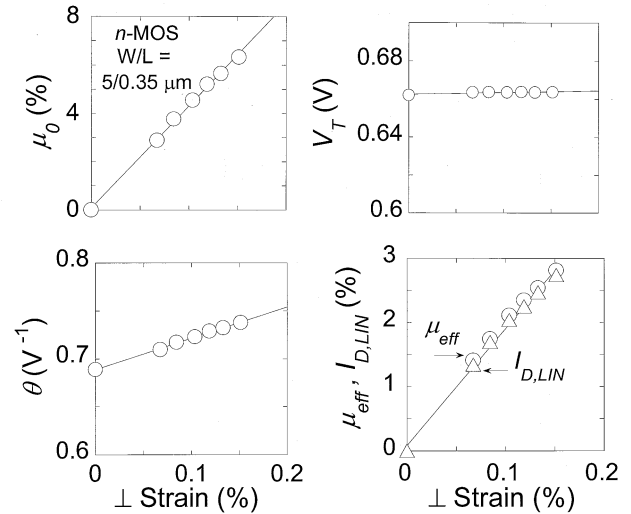


Fig. 9. (a) Comparison of the normalized low-field mobility  $\mu_0$  at  $V_{GS} = V_T$ , (b) threshold voltage  $V_T$ , and (c) mobility attenuation coefficient  $\theta$  for the n-MOSFET ( $W/L = 5/0.35 \mu\text{m}$ ) versus  $\perp$  strain. (d) Effective mobility  $\mu_{eff} = \mu_0 / (1 + \theta(V_{GS} - V_T))$  given by the circles, accounts for all of the strain-induced change in the low-field, linear, drain current  $I_{D,LIN}$  (triangles).

effective mobility  $\Delta\mu_{eff}$  and the linear current  $\Delta I_{D,LIN}$  versus strain. We see these trends almost overlay with less than 5% of difference.

Despite the gate length dependence of  $\Gamma_{LIN}$ , we find, for the first time, that the  $\mu_0$  gauge factor  $\Gamma_{\mu_0}$ , i.e., the relative change of  $\mu_0$  with strain, is almost independent of the gate length for the transverse strain and it is about  $43 \pm 3$  ( $60 \pm 4$ ) for n- (p-) MOSFETs, as shown in Fig. 10. This means a 1% transverse strain will increase  $\mu_0$  by 43% (60%) for n- (p-) MOSFETs (we note that the drain current will not change linearly with the application of strain larger than roughly 1%). The magnitude of  $\Gamma_{\mu_0}$  does decrease with the shrinking of gate length for the longitudinal strain, see Fig. 10, which is the same as that of  $\Gamma_{LIN}$ . We also note that the  $\Gamma_{\mu_0}$  of our p-MOSFETs is negative under longitudinal strain. Hamada [11] attributed the gate length dependence of the transconductance change (which is actually equivalent to the change of effective mobility  $\mu_{eff}$ ) to the difference

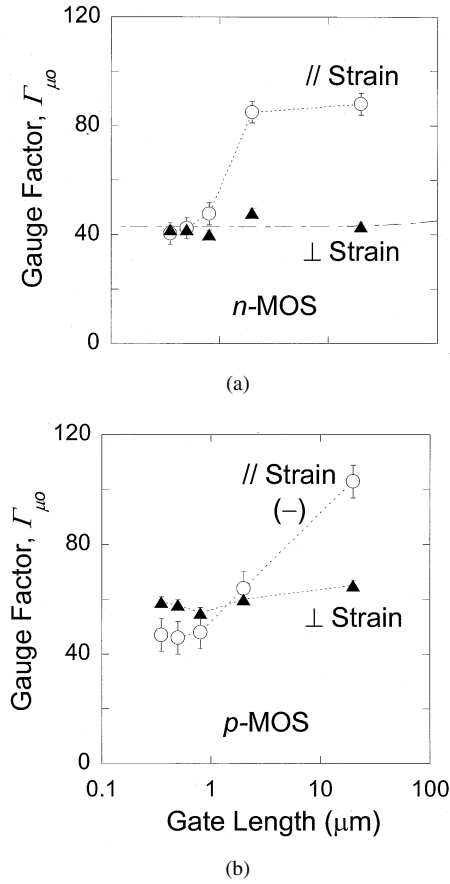


Fig. 10. (a) Low-field mobility  $\mu_0$  gauge factor ( $\Gamma_{\mu_0}$ , the normalized  $\mu_0$  change with strain) versus gate length for n- and p-MOSFETs. (b) The low-field mobility gauge factor is almost constant for both n- ( $43 \pm 3$ ) and p-MOSFETs ( $60 \pm 4$ ) under transverse ( $\perp$ ) strain. The mobility gauge factor is negative for p-MOSFETs under longitudinal (//) strain as indicated by the (-) sign in (b).

of channel stress distribution for different gate-length devices. However, the effective mobility  $\mu_{\text{eff}}$  is an extrinsic parameter depending on both vertical effective field,  $R_{\text{SD}}$ , and mobility, see (3). By contrast,  $\mu_0$  has the physical meaning of the mobility right at the start of inversion and is an intrinsic parameter. The mobility  $\mu_0$  is therefore more suitable than  $\mu_{\text{eff}}$  for characterizing the strains effects on the intrinsic property of MOSFETs. From the extracted  $\mu_0$  gauge factors, Hamadas explanation seems plausible for the longitudinal strain but not applicable for the transverse strain in our case. This may be an indication that there is no difference in the channel stress distribution versus gate-length for devices under transverse strain.

#### IV. CONCLUSION

We have investigated the effects of uniaxial strain on the DC characteristics of PD-SOI MOSFETs. The drain current increases under both longitudinal and transverse strains for the n-MOSFETs, although the former is more effective. The current of the p-channel devices decreases (increases) under longitudinal (transverse) strain. This phenomenon is consistent with that of bulk MOSFETs. These changes correlate with the piezoresistance coefficients of Si inversion layers. The ratio of the saturation to linear current gauge factor ( $\Gamma_{\text{SAT}}/\Gamma_{\text{LIN}}$ ) decreases with the shortening of gate length for both n- and

p-type devices. The low ratio, 0.32 (0.44) for  $L = 0.35 \mu\text{m}$  n-MOSFET under transverse (longitudinal) strain, is due to both nonequilibrium carrier transport and possible self-heating effects. The threshold voltage  $V_T$  remains nearly constant under both strains for n- and p-channel devices. The change in drain current is due to a modification of the effective mobility  $\mu_{\text{eff}}$ . The magnitudes of linear ( $\Gamma_{\text{LIN}}$ ) and saturation ( $\Gamma_{\text{SAT}}$ ) current gauge factors are smaller for shorter gate-length n- and p-MOSFETs. The relative change of low-field mobility with transverse strain is independent of gate length for both carrier type devices ( $\Gamma_{\mu_0} = 43 \pm 3(60 \pm 4)$ ). For longitudinal strain, the low-field mobility follows the gate-length dependence of the linear current change with strain.

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