Controlled chemical mechanical polishing of polysilicon and silicon dioxide for single-electron device

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In this article, the authors report experimental results of the chemical mechanical polishing (CMP) of silicon dioxide (SiO_2) and polysilicon to produce nanoscale features with very smooth surfaces. The sizes of the features polished ranged from 30 to 500 nm. For polysilicon polishing, the nanostructures were defined in positive tone e-beam resist and the pattern was transferred to the oxide substrate using reactive ion etching. These etched nanostructures (70 nm deep trenches) were conformally filled with low pressure chemical vapor deposited polysilicon and polished using a CMP system. Polishing planarized the sample and removed the polysilicon overburden to expose the filled trenches in the SiO_2. The polished structures were studied using scanning electron microscopy (cross sections) and atomic force microscopy (surface). The authors report controllable CMP to realize ~20 nm thick layers after polishing, with rms roughness of ~0.3 nm. Better control of the CMP process (few nm/min removal rate) was demonstrated by using diluted slurry or pure de-ionized water as the CMP slurry. © *2007 American Vacuum Society.* [DOI: 10.1116/1.2433986]

I. INTRODUCTION

For more than a decade chemical mechanical polishing (CMP) has been the key enabling technology in the manufacture of integrated circuits (ICs).[1] CMP is used to planarize and polish the starting wafers used for IC fabrication, as well as to planarize the topography (dielectric CMP) or pattern interconnects (metal CMP) at several stages of the fabrication process.[2] With features shrinking to the nanoscale, well-controlled CMP becomes critical.

The results presented in this article are derived from the fabrication techniques being developed for a Si based single-electron device (SED).[3,4] Room temperature Si single-electron transistors (SETs) have been reported in the literature;[5] however, these devices suffer from a number of problems that will preclude their use in the production of integrated circuits. These problems are a result of the uncontrolled dot size and tunnel barrier thickness. We are developing a fabrication technique based on lithography, dry etching, and CMP that will produce a SET with a well-controlled geometry, dot size, and most importantly a high-quality well-controlled tunnel oxide. The device consists of a Si rib, which forms the source and drain leads for the device, and a heavily doped polysilicon island isolated from the source and drain leads by ultrathin thermal silicon dioxide. A simplified description of the fabrication is as follows. The device layer (~50 nm thick) of a silicon-on-insulator wafer is patterned by electron-beam lithography (EBL) and high selectivity (Si over SiO_2) inductively coupled plasma (ICP) etch to form thin Si ribs (~20–40 nm wide) and an adjacent gate on the buried oxide (BOX). Silicon dioxide is deposited on the sample with a thickness greater than that of the Si rib. The sample is planarized using the CMP system to expose the top of the Si ribs. The SET island is defined by writing lines (~20–40 nm wide) by EBL to perpendicularly intersect the Si rib. After development of the EBL resist, the exposed part of the Si rib is etched up to the BOX using the same high selectivity ICP etch. An ultra thin thermal oxide (~1–2 nm) is grown on the sidewalls of the etched pit in the Si rib. Polysilicon is deposited by low pressure chemical vapor deposition (LPCVD) on the sample, filling the pit. A final CMP step will remove the overburden of polysilicon, leaving only that in the pit. A three-dimensional representation of the completed device is shown in Fig. 1. The fabrication method introduces CMP as a key processing technique in the production of nanometer scale features for SETs. In CMP, the polishing pad removes high spots on the wafer, planarizing the surface and removing the topology that develops as layers are deposited in the interconnect stack of the circuit. We plan to extend the use of CMP to nanoscale dimensions. It is essential to develop a controlled CMP process to achieve this device structure. In this work, the focus is on developing a CMP recipe to meet the stringent requirements of our device fabrication and investigate the possibilities and limitations of polishing nanostructures.

II. EXPERIMENTS

The first step of the experiment was to develop a CMP recipe for polysilicon with very controlled polishing rates. A 240 nm thick thermal oxide was grown on 4 in. ⟨100⟩ silicon wafers. 270 nm thick polysilicon was deposited in a LPCVD furnace at 625 °C on oxidized silicon wafers. The polysilicon deposited wafers were diced to 1×1 cm^2 size samples to fit into a CMP template used to hold the samples during CMP. Prior to further processing, the samples were cleaned in acetone, isopropyl alcohol (IPA), and de-ionized (DI) water to remove any debris from the dicing process. The thicknesses of the polysilicon and oxide films were accurately measured using variable angle spectroscopic ellipsometer

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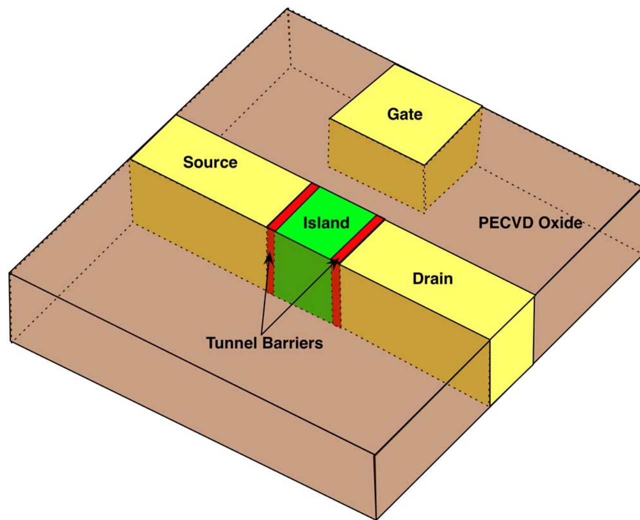


FIG. 1. 3D pictorial representation of the proposed Si based SED.

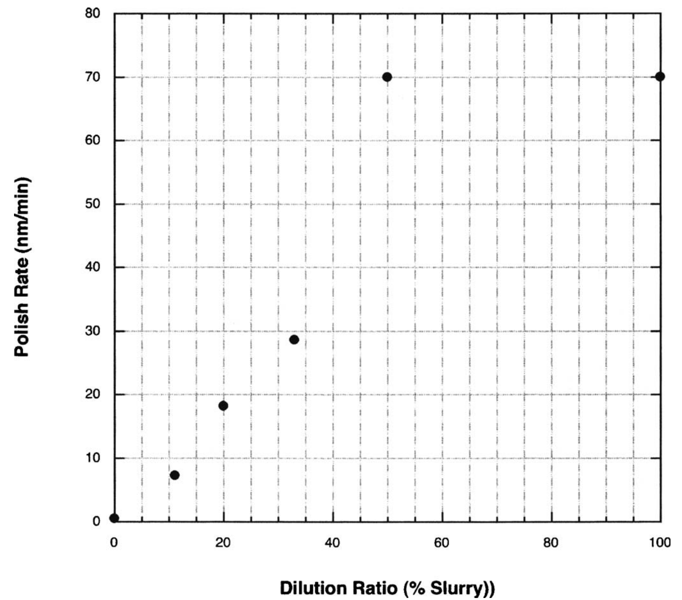
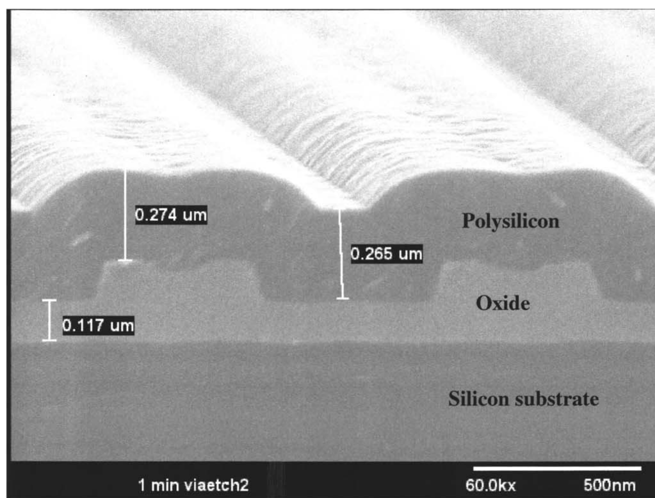


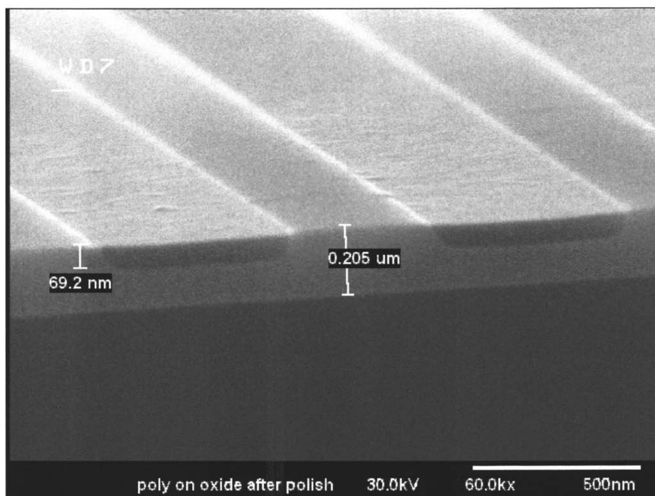
FIG. 2. Plot of polishing rate of polysilicon vs the dilution ratio of the slurry.

(VASE) and by cross-section measurements in scanning electron microscope (SEM). Both these techniques require a thermal oxide layer underneath the polysilicon for accurate measurements of the polysilicon film. After this, the samples were polished in a Logitech chemical delayering and planarization system with *in situ* pad conditioning on an Epic® D100 CMP pad from Cabot Microelectronics. The pad and sample carrier rotation were fixed at 25 and 30 rpm, respectively. Very low pressure of 0.25 psi (converted to actual pressure between the sample and the pad) was applied to maintain good contact between the sample and the pad. Higher pressure results in higher material removal rates, whereas no back pressure causes the sample to hydroplane on the slurry, yielding nonideal CMP performance. We had to use a very low pressure to ensure that we get controlled polishing rate with the ability to stop precisely at the required film thickness. A flow rate of 50 ml/min of Semi-Sperse® P1000 ready-to-use polysilicon slurry from Cabot Microelectronics was used for the polishing. The polishing was done for all the samples with the same conditions but with varying dilution of the slurry. The slurry was diluted with DI water in the ratios of 1:1, 1:2, 1:4, and 1:8 by volume. An important characteristic of the diluted slurry is that it retained its colloidal consistency even after standing for 2 weeks. Post-CMP cleaning consisted of dipping the polished sample for a few seconds in dilute ammonium hydroxide (NH_4OH:DI water=1:4) and a DI water rinse.[6] The main objective of the ammonium hydroxide dip was to remove the slurry particles adhering to the sample surface, or to reduce the van der Waals force of attraction, hence making it easier to remove the slurry particles during subsequent DI water rinse. So the cleaning in ammonium hydroxide involved a few seconds dip with slight agitation. We used 1:4 diluted ammonium hydroxide solution and did not notice any adverse effects on the polished surface. After the polishing process, the thickness of the remaining polysilicon film was measured using VASE. Different models for polysilicon were tested to ensure that the fits obtained conformed to the real thickness. Also, the cross section was measured in SEM to corroborate our VASE results. The VASE measurements and the SEM measurements were taken from approximately the same spot for all the samples to ensure validity of the results. Because of the small size of the samples, it was seen that the polishing rate was not very uniform over the entire sample. The polished surfaces were scanned with an atomic force microscope (AFM) to measure the surface roughness. It was seen that by diluting the slurry, it was possible to reduce the material removal rate.

The next part of the experiment was to apply the developed CMP recipe to polish the nanostructures. Oxidized Si wafers, with an oxide thickness of 240 nm, were diced to 1×1 cm^2 size pieces. These samples were cleaned in acetone, IPA, and DI water to remove any Si dust adhering to the surface. Following hexamethyldisilazane treatment, ZEP-520A, positive tone e-beam resist from Zeon Corp., was spun on the samples at 3000 rpm, giving a resist thickness of ~420 nm. An Elionix ELS-7700 e-beam lithography system was used to write lines in the resist (75 kV, 50 pA) with different pitches of 200 nm, 500 nm, and 1 μm. The linewidth was varied from 30 to 500 nm. After development in *o*-Xylene (1,2-dimethylbenzene or C_8H_{10}) for 2 min, the pattern was transferred into the silicon dioxide by dry etching in reactive ion etching (CHF_3/O_2). ZEP series resists provide much better dry etch resistivity as compared to the other commonly used positive tone e-beam resists such as polymethylmethacrylate. The depth of the etched trenches varied from 50 to 90 nm, depending on the linewidths. The trenches were conformally filled with 270 nm thick LPCVD polysilicon. Cross-sectional analysis in SEM was done to ensure that the polysilicon conformally filled the etched narrow trenches. The samples were polished to the oxide to expose the polysilicon-filled trenches. Surface roughness of the polished surfaces and the phenomenon of dishing and its



(a)



(b)

FIG. 3. (a) SEM cross-sectional view of an unpolished sample showing the patterned oxide with LPCVD polysilicon on top. (b) SEM cross-sectional view of a sample polished down to the oxide removing the polysilicon overburden.

dependence on pattern density were studied in these nanostructures using AFM. The samples were cleaved through the pattern to study the cross section of the polished nanostructures.

III. RESULTS AND DISCUSSION

Figure 2 shows the polishing rate of polysilicon versus the percentage dilution of the slurry. For the given polishing conditions we can reduce the polishing rate by increasing the dilution of the slurry without affecting the quality of the polished surface. Dilutions lower than 1:8 were not tried as this dilution ratio already provided us with a very good control over the amount of material removed. The polishing rate drops to a few angstroms per min when pure DI water is used as the slurry. The surface roughness of the sample polished with undiluted P1000 slurry was measured to be around 0.34 nm (rms), while the surface roughness for the sample polished with DI water was around 0.35 nm (rms). It was seen that the surface roughness of the polished polysilicon was lower than the originally deposited LPCVD polysilicon (~2.3 nm rms). It should be noted that in Fig. 2 the polishing rate for undiluted slurry does not follow the trend and is anomalous. As the focus of our experiments was to develop a CMP recipe with low polishing rate, further investigation of this anomaly was not pursued.

TABLE I. Tabulation of the dishing depth (nm) dependence on feature width and pattern density.

Pitch (nm)	Linewidth (nm)	Dishing effect depth (nm)
200	50	1.9–3.1
	80	2.1–3.1
500	30	2.0–2.5
	100	4.4–5.7
1000	50	1.9–2.6
	130	5.4–7.4
1000	200	10–15

Figures 3(a) and 3(b) show the SEM cross-section images of the unpolished and polished samples, respectively. P1000 polysilicon slurry has a very high selectivity for polishing polysilicon over silicon dioxide (~300:1). Hence, once the silicon dioxide surface is exposed the polishing rate falls drastically. Further polishing results in the phenomenon of dishing wherein the polysilicon in the trenches is removed more than the surrounding oxide, resulting in a concave surface on the polysilicon channel. The dishing effect is due to the combined effect of pad flexibility and chemical selectivity of the CMP slurry.[7] The extent of dishing depends on the width of the wire. The polished surfaces were scanned with AFM to measure the surface roughness and the extent of dishing. Table I gives the measured depth of polysilicon in the trenches as compared to the surrounding oxide. The dishing effect is more prominent in the wider wires as compared to that in the narrow ones. In our specific experiment the dishing effect did not show any dependence on the pattern density. Further polishing revealed that after a dishing depth of around 15 nm in the 200 nm wide rectangles, there is no further increase. Beyond this, the polishing proceeds with the polishing rate of silicon dioxide. This is probably determined by the flexibility of the pad material. Minimizing the depth of these pits in polysilicon layer is essential to the fabrication of nanostructures required for our device. It is our observation that higher relative velocity between the pad and the sample and increased pressure result in a more planar surface at the expense of a higher material removal rate. So after removal of most of the polysilicon overburden, CMP was continued with pad and sample carrier rotations of 50 and 55 rpm, respectively, and a pressure of 0.5 psi. Figures 4 shows the controlled thinning of the polysilicon-filled trench

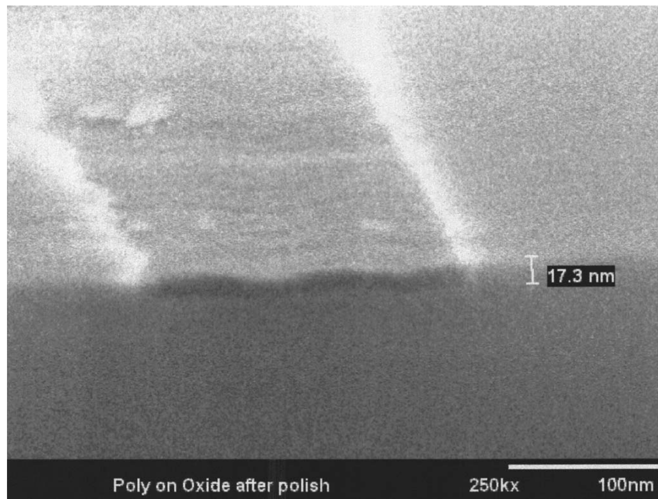


FIG. 4. <20 nm thin polysilicon channel fabricated by CMP. The undulation seen on the surface is an artifact of the acoustic noise affecting the scanning electron beam.

to form a <20 nm thick polysilicon channel. Improved planarity enables the fabrication of 20 nm thick polysilicon structures.

IV. CONCLUSIONS

This work shows that it is possible to achieve very controlled CMP material removal rate by dilution of the commercially available ready-to-use slurry. The diluted slurry produces a near-atomic-level smooth surface quality similar to the original undiluted slurry. The experiments demonstrate successful CMP on nanoscale features. The dishing effect was more prominent in wider features. By increasing the relative velocity between the pad and the sample, it was possible to improve the planarity of the polished nanostructures. Also the pattern density did not influence the dishing depth. With the recipes developed, we show successful fabrication of very thin channels formed in polysilicon by CMP and we anticipate that these results can be adapted for polishing other materials.

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