**EXPERIMENTAL STUDIES OF CLOCKED QUANTUM-DOT CELLULAR AUTOMATA DEVICES.**

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Devices based on Quantum-dot Cellular Automata (QCA) computational approach [1] use interacting quantum dots to encode and process binary information. In this transistorless approach to computation, logic levels are represented by the configurations of single electrons in coupled quantum-dot systems. In the last few years, significant progress has been made towards the realization of basic QCA elements. A fully functional QCA cell, small chain of cells forming a binary wire, and a digital logic gate have been demonstrated [2]. However, in these devices power gain needed for the operation of large QCA arrays was not possible since the only source of energy was the signal input.

Recent theoretical work [3] proposed clocked control of the QCA circuitry. Clocked controlled QCA systems have many advantages such as power gain, reduced power dissipation, and pipelined architectures. Power gain is possible because energy can be supplied to each cell directly by the clock lines rather than passed from the inputs alone. Pipelining is possible because clocked cells can be placed in a lock state which acts as a short-term memory, allowing an array to be broken into sub-arrays, with each working on different parts of a computational problem. The original theoretical work applied only to semiconductor implementation of clocked QCA arrays, but recently a scheme for clocked control of metallic QCA cells was proposed [4]. Here an extra dot placed between the two dots of the QCA half-cell acts as a tunable barrier controlled by the clock signal.

We present the experimental demonstration of a clocked QCA cell. The device consists of two capacitively coupled half-cells, where each half-cell consists of three micron-size Al islands separated by tunnel junctions ( D1-D3, and D4-D6 ), and four electrometers ( E1-E4 ) to measure the charge state of the half-cells (Fig.1). The half-cells are leadless, with no DC connection to the environment. Figure 2 demonstrates the clock controlled switching of single electrons in such a cell. The signal input $V_{IN}$ defines the direction of switching only, whereas the actual electron switching is accomplished by the clock signal $V_{CL}$.

Another important feature of the clocked QCA architecture is the ability of cells to provide a short-term memory to adjacent cells. In this case an appropriate clock signal "locks" an electron in a metastable state, so that the half-cell remains polarized even in the absence of the input signal. Figure 3 shows experimental observation of the locked mode in a half-cell, where the hysteresis loop represents two different states of memory in this mode. To measure this device in our present experimental set-up, some modifications of the cell were made. To increase the lifetime of the metastable locked mode, multiple tunnel junctions have been added between the central and outside dots.

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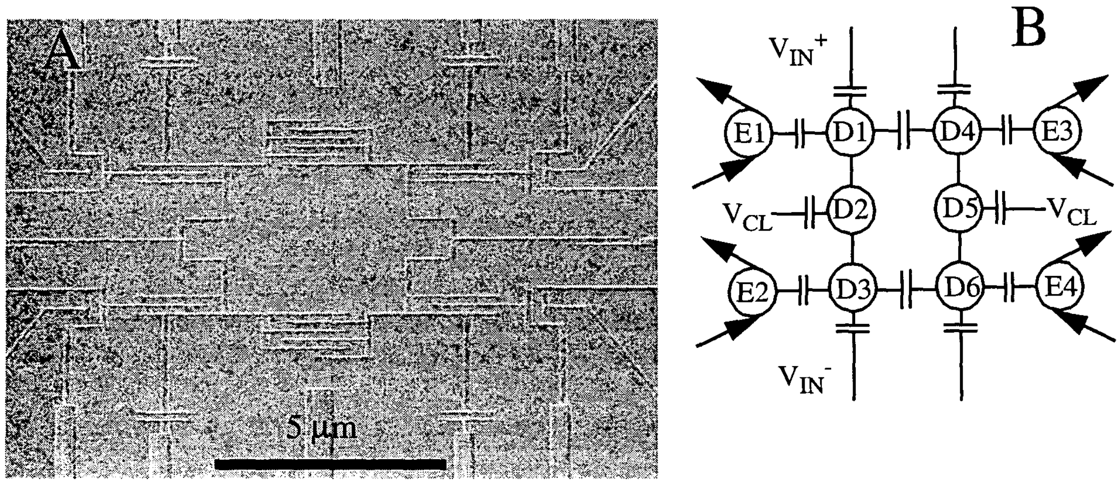


Figure 1. (A) SEM micrograph of the clocked QCA cell (B) Schematic diagram of the device

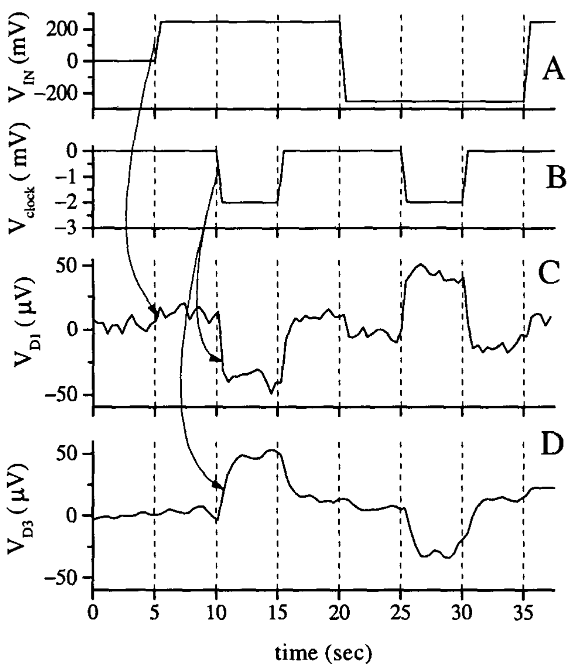


Figure 2. Clocked QCA cell experiment. From top to bottom: (A) signal input; (B) clock input; (C) signal measured on dot D1; (D) signal measured on dot D4.

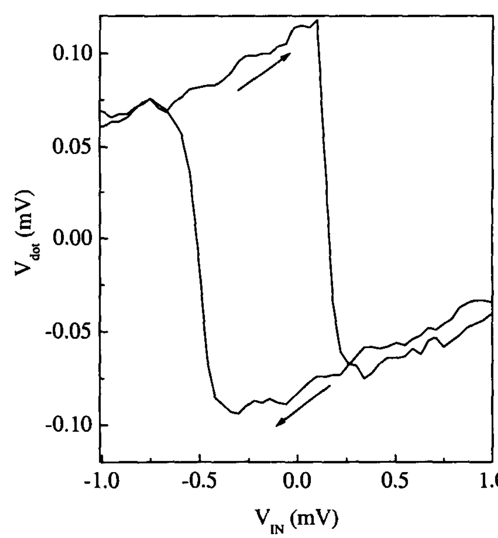


Figure 3. Demonstration of the "memory" in the clocked QCA cell