Electronic Quantum-dot Cellular Automata

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Abstract

This paper presents an overview of the electronic implementation of quantum-dot cellular automata (QCA). QCA is a computing paradigm that encodes and processes information by the position of individual electrons. This opens the possibility of dense, ultra-low power devices. Resent results are presented from QCA cells implemented using metal-dots, as well as investigations toward molecular and silicon QCA devices.

1. Introduction

Are alternative electronic devices needed? If so, what form should they take? Are revolutionary devices needed, or will evolutionary development of existing devices be sufficient? There are no definitive answers to these questions, and yet finding the answers takes on extreme importance as the end of MOSFET scaling approaches. Questions regarding the fundamental limits of the energy required for computation also become important as the end of scaling approaches.

The MOSFET has been the driving engine of the microelectronics industry for over 30 years, and the industry has proven remarkably able to scale MOSFETs to ever-smaller dimensions. The end of scaling has been predicted many times, but the dire predictions have never come to pass. However, the end of scaling is in sight and most observers believe that the industry will hit the "Red Brick Wall" between 2015 and 2020. Scaling of MOS will come to an end for several fundamental reasons, but perhaps the most important is the power density. For common MOS circuits this is already 75-100 W/cm^{-2}, more than twice the power density of a standard electric range-top element. The goal of the industry is to go from device densities of ~10^8 cm^{-2} today to 10^{11} – 10^{12} cm^{-2}, but to achieve such high densities will be difficult given the power constraints of attainable packages. Already, chip designs reflect the limitations imposed by power dissipation. Clock speeds are no longer increasing, and Moore's Law is maintained by increasing the amount of cache memory, or placing multiple cores on a chip. This represents a fundamental shift in the definition of progress.

In the past progress was defined as performance increases achieved by making transistors smaller and clocking the circuits faster. Now transistors are not clocked as fast as they could be (due to heat), and the performance issue is passed to the computer architects who achieve higher performance with reduced memory latency (bigger caches) and parallel processing (multi-cores).

This paper will present one possible approach to achieving the ambitious goals of the industry is to employ a paradigm based on nanoelectronic devices. This family of devices, called quantum-dot cellular automata (QCA) was developed at the Univ. of Notre Dame [1, 2]. The fundamental idea for QCA operation is to encode information using the charge configuration of electrons within a set of coupled quantum dots [3]. This is an important break with the transistor paradigm. QCA has been demonstrated in both electronic [4, 5] and magnet implementations [6]. This paper will concentrate on electronic implementations.

A schematic diagram of a four-dot QCA cell is shown in Fig. 1. This is the simplest non-clocked QCA cell. The cell consists of four quantum dots positioned at the corners of a square. The cell contains two extra mobile electrons, which are allowed to tunnel between neighboring sites of the cell, but not out of the cell. If the tunnel barriers between cells are sufficiently high, the electrons will be well localized on individual dots. The Coulomb repulsion between the electrons makes them occupy antipodal sites in the square as shown. For an isolated cell there are two energetically equivalent arrangements, polarizations, of the extra electrons that we can denote as binary 1 and binary 0. The two polarization states of the cell will not be energetically equivalent if other cells are nearby, since the Coulomb interaction with other cells breaks the degeneracy.

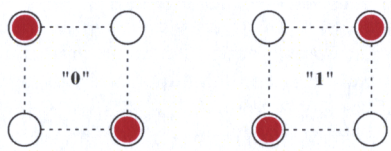

Figure 1. Four dot QCA Cells

A QCA wire is shown in Fig. 2(a). The left-most cell is fixed with a polarization representing the input. The difference between input and outputs cells in QCA arrays is simply that inputs are fixed and outputs are free to change. The ground state configuration of the remaining free cells is then one with each cell polarized in the same way as the input cell. We can consider this transmission of the input signal from one end to the other. Cells that are positioned diagonally from each other tend

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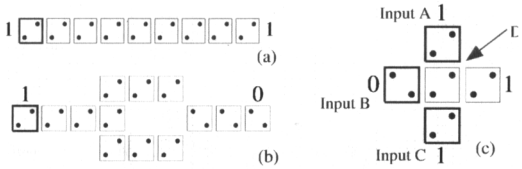

Figure 2. Fundamental QCA devices. (a) Binary wire. (b) QCA inverter. (c) Majority logic gate.

to anti-align. This behavior is employed to construct an inverter as shown in Fig. 2(b). Figure 2(c) shows the fundamental QCA logical device, a three-input majority gate, from which more complex circuits can be built. The central cell, labeled the device cell, has three fixed inputs, labeled A, B, and C. The device cell has its lowest energy state if it assumes the polarization of the majority of the three input cells. It is possible to "reduce" a majority logic gate by fixing one of its three inputs in the 1 or 0 state. In this way, a reduced majority logic gate can also serve as a programmable AND/OR gate. Combined with the inverter shown above, this AND/OR functionality ensures that QCA devices provide logical completeness.

Clocking is an important concept in QCA as it provides the means to produce power gain, needed to restore logic levels in a large system. Clocking in QCA is based on a concept developed by Keyes and Landauer in 1970 [7]. In this scheme an electron is in one of two wells, separated by an energy barrier. To quasi-adiabatically switch the electron to the other well, the barrier between the wells is lowered so that the electron can access both wells, an input applied which nudges the electron to the other well, and finally the barrier is raised forcing the electron into the selected well. The potential that modulates the barrier can do work on the system, and thus be the source of power gain. In a QCA cell the barrier is modulated by a clock signal, and the input can be that of an adjacent cell. If the coupling between cells is weak, power gain can be achieved since the input merely nudges the electron toward the proper dot, while the clock does the work of forcing the electron to that dot.

Clocking of QCA cells is also important because it enables control of the flow of energy in the system, making it possible to attain ultra-low power dissipation. It has been asserted that a state variable other than charge will be required for future computation because there are fundamental limits to the size, and dissipation that doom the scaling of charge-based devices [8]. However, the arguments presented in [8] are flawed in a number of ways. There is no fundamental lower limit to the dissipation of computational elements. It has been shown theoretically that QCA systems can be used to perform reversible computing with no lower limit to the dissipation, and that Bennett clocking can be used to simplify the implementation of reversible computing [9].

QCA cells have been demonstrated in a number of different physical implementations including metal dots, magnetic dots [6], GaAs/AlGaAs dots [10], and phosphorous islands in silicon [11]. The remainder of this paper will concentrate on the research at Notre Dame on electronic QCA cells.

2. Metal-dot QCA

The operation of QCA cells has been experimentally verified using aluminum dots coupled by aluminum oxide tunnel junctions. These devices are fabricated using electron-beam lithography and the Dolan bridge technique [12] to produce small (~50 x 50 nm) tunnel junction capacitors. Although all of these devices operate only at cryogenic temperatures, ~300 mK - 1K, they have been very useful in demonstrating the operating principals of QCA. The research group at Notre Dame demonstrated the first QCA cell [5, 13], which showed that the position of a single electron can control the position of a second single electron.

In metal-dot QCA cells the barrier between the dots is aluminum oxide, and hence cannot be modulated to implement clocking. The variable barrier in this case is formed by adding two additional dots to each cell. The potential of these additional dots is set by the clock line to control the tunneling of the electron between the top and bottom dots on the left and right halves of the cell. Using these modified cells we have also demonstrated clocked QCA cells, a QCA shift register, and power gain in QCA cells [14, 15].

At an early stage of QCA development particular attention was drawn to the issue of energy distribution in the fanout gate, which comprises of a single input port transmitted to two output ports, Fig. 3(a). For the signal to propagate in a fanout gate, one input feeding two outputs, it is essential for the input cell to flip the polarization of the two output cells. It was shown that an unclocked fanout gate architecture has a high probability to enter a metastable state. Clocked control [16] by cyclical manipulation of inter-dot tunnel barriers solves the problem of unwanted metastable states. In fact, the operation of a fanout gate is a direct demonstration of power gain in QCA circuits since one input drives two outputs.

A fanout gate consists of three QCA latches capacitively coupled by inter-latch coupling capacitors C_C, Fig. 3(a) [17]. Each QCA latch consists of three aluminum metal islands connected in series by multiple (N=3) tunnel junctions (MTJs). The typical tunnel junction resistance is ~500 kΩ and capacitance is ~ 300 aF. MTJs are used to increase the hold time of the latch to match our low-speed measurement. Single electron transistors coupled to the end dots of each latch are used

to detect electron switching in the latch [18]. To achieve symmetry in inter-latch coupling the electrometers E_2 and E_3 are connected to the opposite end dots in the output latches L_2 and L_3. Therefore if latches L_2 and L_3 are switched to the same polarization, the signals in the corresponding electrometers (E_2 and E_3) will be out of phase. For signal detection in the input latch either electrometer (E_1 or E_1^*) can be used. Electrometer E_1 is used in the experiment described below. Lock-in amplifiers are used to measure currents through the electrometers biased with an excitation bias of ≤ 100 μV at 3 kHz.

Figure 3(b) shows the operation, at approximately 100 mK, of the clocked fanout gate as pulsed input and clock signals are applied to the latches. The operation of the device is accomplished in two clocking cycles and can be divided into two phases for both polarities of the applied input signal, representing binary 0 and 1. In phase #1, a negative (positive, second phase) input signal is first applied to the input latch L_1 at t_1 (t_7), and then on the application of the clock signal CLK1 at t_2 (t_8) an electron switching occurs in L_1. Note that both CLK HIGH signals are negative voltages. Removal of the input bias applied to L_1 at t_3 (t_9) leaves the latch L_1 in the locked state where the switched electron in the end dot is retained as long as the CLK1 is set HIGH. Once L_1 is locked, it acts as an input to the output latches (L_2 and L_3). In phase #2, the clock signal CLK2 is simultaneously applied to L_2 and L_3 at t_4 (t_{10}) and the Coulomb repulsion caused by the latched electron in L_1 leads to latching of electrons in L_2 and L_3. The polarization of the output state in L_2 and L_3 depends upon the polarization of the input latch L_1. Note that no separate input pulses are applied to input leads of L_2 and L_3 in this process. Resetting the clock signal of L_1 at t_5 (t_{11}) does not affect the electrons switched in L_2 and L_3 as they are now in the locked state. L_2 and L_3 remain in the locked state until CLK2 is removed at t_6 (t_{12}). Multiple measured experimental traces (shown in Fig. 3(b)) demonstrate fanout gate operation as described above.

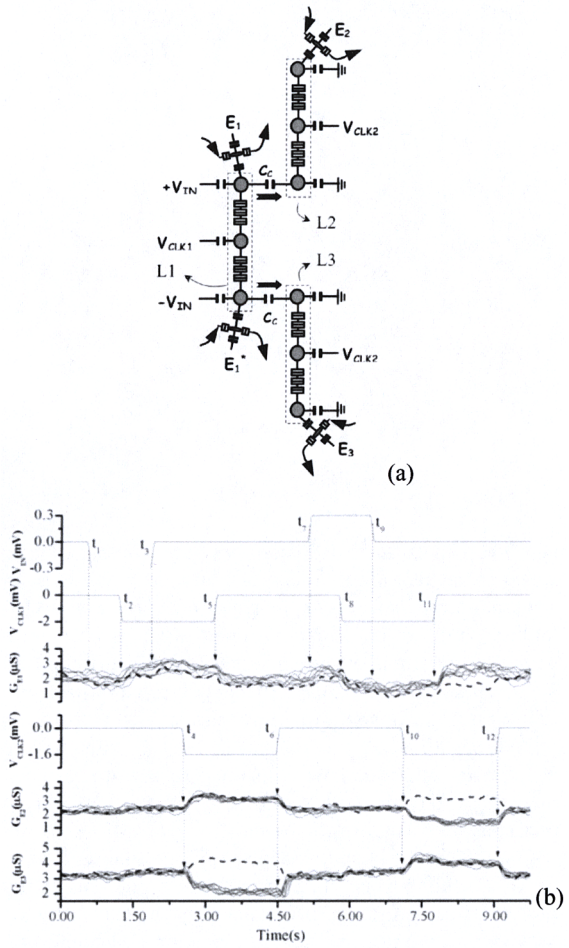

Figure 3. (a) Schematic of metal dot implementation of fan-out gate. (b) Experimental data.

3. Molecular QCA

The greatest drawback to existing demonstrations of QCA devices is the cryogenic temperatures required for operation. To operate at higher temperatures a smaller device is required. If the dots are scaled to molecular sizes the cell will work at room temperature. To investigate molecular QCA, we have studied the control of charge motion within molecules. Electric field-driven bi-stability has been demonstrated using a large number of silicon surface bound, vertically oriented molecules over a large area using a dinuclear complex and a capacitive measurement [19, 20]. These molecules can be bound to the surface of a chlorinated, highly p-type silicon substrate and oxidized to become stable, biased $Fe^{III} - Ru^{II}$ mixed-valence complexes. Application of an electric field can drive the molecules from the $Fe^{III} - Ru^{II}$ configuration to the $Fe^{II} - Ru^{III}$ configuration.

The next step in the pursuit of molecular QCA cells is to demonstrate charge switching in individual molecules. To do this we interface molecules to SET electrometers similar to those used in the metal-dot devices. Measurements of these devices are currently underway.

4. Silicon QCA Devices

The first step in making a silicon QCA cell is to fabricate a Si based SET. Previously reported results on Si-SETs [21] show that these devices have excellent long term charge stability, the obligatory feature for any practical use of SET devices. Si-SETs operating at room temperature have been reported in the literature, but these devices suffer from a number of problems due to

uncontrolled dot size and tunnel barrier thickness. We have developed a fabrication method using lithography, dry-etching, and chemical mechanical polishing (CMP). Our method produces an SET with a well-defined geometry of the dot and, most importantly, a high quality well-controlled tunnel oxide. A simplified description of the fabrication is as follows. The device layer (~50 nm thick) of a SOI wafer is patterned by electron-beam lithography (EBL) and high selectivity inductively coupled plasma (ICP) etch to form thin Si ribs (~20-40 nm wide) and an adjacent gate on the buried oxide (BOX). Silicon dioxide is deposited on the sample with a thickness greater than that of the Si rib and planarized using CMP to expose the top of the ribs. The SET island is defined by writing lines (~20-40 nm wide) by EBL to perpendicularly intersect the Si rib. The exposed part of the Si rib is etched up to the BOX using the same high selectivity ICP etch. An ultra-thin thermal oxide (<1.5 nm) is grown on the sidewalls of the etched pit in the Si rib. LPCVD polysilicon is deposited on the sample, filling the pit and a final CMP step removes the overburden of polysilicon, leaving only that in the pit. A 3-dimensional representation of completed device is shown in Fig. 4(a).

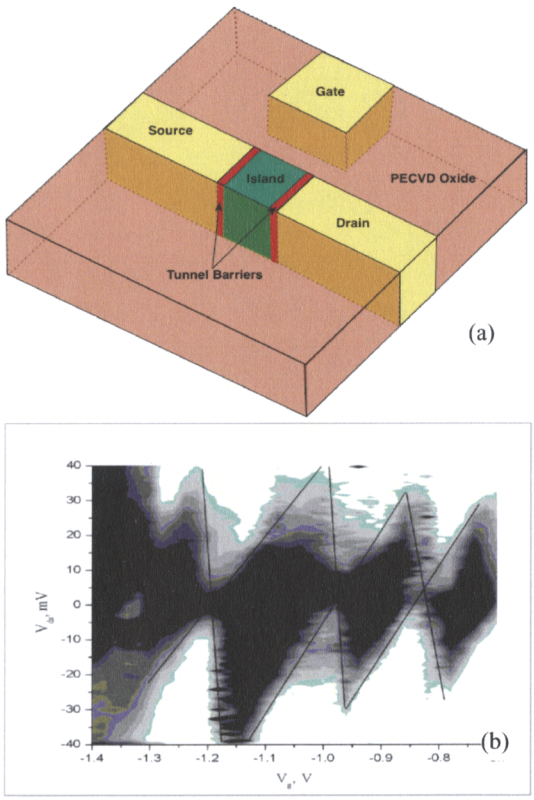

Figure 4 (a) Silicon SET Structure. (b) Charging diagram.

The charging diagram of this device is shown in Fig. 4(b). This plots the conductance (gray-scale) against the gate voltage (V_g) and the drain-source voltage (V_{ds}). It shows the characteristic "Coulomb Diamonds", and has a charging energy of over 20 meV. Coulomb blockade oscillations can be see at 180 K. This early result points to possibility of QCA cells operating at close to room temperature.

Acknowledgments

The authors would like to acknowledge the support of the National Science Foundation.

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