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Temperature dependence of the locked mode in a single-electron latch

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Abstract

Interaction between single electrons in coupled quantum dots is used to perform binary logic operations in Quantum-dot Cellular Automata (QCA). Clocked control over tunneling is necessary to achieve power gain and minimize power dissipation in QCA. The high temperature limit for clocked operation is set by the ability of the cells to store binary information when the input signal is removed (so-called 'locked mode'). We present an experimental investigation of the temperature dependence of the locked mode in metal-dot based clocked QCA device. The experimental results are in very good agreement with the orthodox Coulomb blockade theory for thermally activated electron escape mechanism.

Keywords: Single-electron logic; Quantum-dot cellular automata; Bistability

1. Introduction

Quantum-dot cellular automata (QCA) is an architecture targeting nanometer-sized devices, which uses interaction between single electrons in coupled quantum dots to perform binary logic operations [1]. One of the biggest challenges for the nanostructure-based devices is to achieve power gain, which is a key mechanism for obtaining logic level restoration. Cyclical manipulation of quantum wells to perform binary operations (with logic level restoration and ultimately low power dissipation), was first discussed by Keyes and Landauer [2]. Clocked control for semiconductor-quantum-dot based QCA was proposed by Lent et al. in [3] and further developed in [4]. The first implementation of the Keyes–Landauer scheme for classical Coulomb blockade system with tunnel barriers was suggested by Likharev and Korotkov in [5] and later refined in [6]. A similar design was used by Toth and Lent [7] for clocked control of the switching in metal-dot QCA cells. While molecular QCA devices operating at room temperature are currently being investigated, no technology is available yet to implement it. Metal–tunnel junction prototypes of QCA, fabricated using high-resolution electron beam lithography, operating at sub-1 K temperatures have been studied experimentally in the past several years. This research has demonstrated key features of clocked QCA architectures and helped understand the challenges in QCA implementation [8,9]. A basic building block of metal-dot based clocked architectures [6,7] is a Single-Electron Latch (SEL) [10] (Fig. 1). One of the major challenges on the way to implementation of 'real world' QCA is very stringent requirement on Coulomb energy barriers which control the operation of quantum-dot logic. Most importantly, for clocked QCA to operate, it must possess a memory feature ('locked mode'), so that once a cell is locked by raising the Coulomb barrier, it can act on the other cell as a fixed input. From the energy point of view, a cell in the locked mode must retain its charge state even if it has to move into a metastable state at a local energy minimum. As the temperature increases, the probability of a transition from this local minimum to the true ground state increases and above some critical temperature, T_{MAX} the bistability can no longer be observed.

In SEL, the localization of a single electron within three dots (D1, D2, D3) connected in series by tunnel junctions, is controlled by a combination of input and clock biases [6,7]. SEL is initially electrically neutral, and single-bit is represented by electro-statically bound electron–hole

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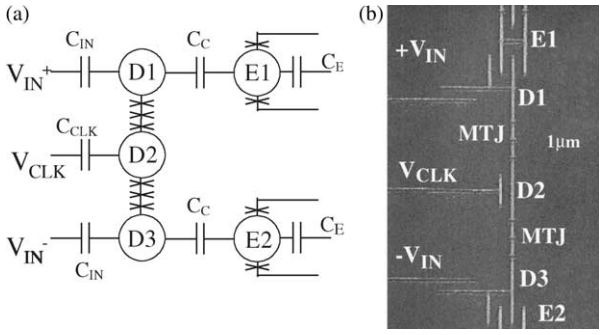

Fig. 1. (a) Circuit diagram of a single-electron latch [6,7]. (b) Electron micrograph of the device.

pair [6]. If clock bias with the magnitude large enough to lift Coulomb blockade condition for D2, $V_{CLK} > e/C_{CLK}$, (where C_{CLK} is the capacitance between clock line and D2), is applied, an electron must leave D2 to minimize the energy of the system. This electron jumps randomly on either of D1 or D3 if no input signal is applied to the end dots. However, if a small (compared to V_{CLK}) differential input signal V_{IN} is applied to end dots the symmetry breaks and an electron tunnels to the dot with lower energy. Depending on which dot the electron is located, the latch represents a digital '0' or digital '1' state. One very important feature of an SEL is its ability to hold an electron even if the input is removed, for as long as the clock signal is applied, thus converting an SEL into a memory element. An electron in this case is trapped in a local energy minimum ('locked mode'). The 'locking' barrier, W, which separates the ground and this metastable state depends on combination of input and clock biases. It can be shown that if the charging energy, E_C, is the same for all dots in the SEL, $W \sim E_C/2$ in the region of SEL operation in locked mode [11]. As a result, the capability of SEL to retain a bit is strongly influenced by the temperature as the thermal energy approaches the energy of the Coulomb barrier separating D1 and D3.

Here we present an experimental study of the temperature dependence of the locked mode in the metal-dot QCA. This analysis could be further applied to the research of the future molecular implementations of QCA.

2. Fabrication and experimental technique

To fabricate the SEL we use well-established metal–tunnel junction technology where device is first defined in the e-beam resist using direct electron beam writing and then fabricated using metal deposition through the shadow mask with in situ oxidation (Dolan bridge technique [12]). The SEL consists of three dots, connected in series by multiple tunnel junctions (MTJ). For the detailed description of SEL operation, see Ref. [10]. MTJs are used to suppress co-tunneling [13] which can lead to escape of an electron from locked state. Single-electron transistors (SET) E1 and E2 are used as readout electrometers. They are biased using control gates to provide linear response to electron switch on the dots coupled to it. Lock-in amplifier technique is used to measure current through electrometers; the magnitude of excitation voltage was $\sim 50\ \mu V$. The frequency of the test signal (~ 3 kHz) and averaging time constant (~ 10 ms) are chosen to exclude distortions of the measured signals. To cancel the parasitic capacitive coupling between the gates of the latch and electrometers a small cancellation voltage is applied to the gates of the electrometers [14]. To suppress superconductivity of Al the magnetic field of 0.5 T is applied to the sample.

3. Experiment and discussion

To study the bistable properties of latch as a function of temperature it is instructive to measure charging 'phase diagrams' of the device for the opposite directions of the input bias sweep. The phase diagram is a gray-scale map of the electrostatic potential on a dot versus the differential input V_{IN}, and the clock voltage V_{CLK}. Each plot is a raster scan, obtained by sweeping one variable and incrementing ('stepping') the other after each sweep. The measurement of the electrostatic potential is obtained by measuring a signal from the electrometer capacitively coupled to a dot. White shade on the map corresponds to positive potential, and black corresponds to a negative potential. The abrupt transitions from white to black correspond to the irreversible single-electron transfers in the bistable region, whereas smooth transitions correspond to the reversible processes. The charge cancellation technique [14] used in the detector circuits also eliminates the monotonic background potential caused by voltage division in the clock circuitry. By measuring the electrostatic potential on one of the end dots (D1 or D3) we can detect all possible single-electron transitions in SEL. For the system which always follows the ground state, the sequence of 'sweeps' and 'steps' is unimportant. However, if system exhibits a bistability, the shape of the phase diagram depends on the direction of the sweeps and on the sequence of operations (step or sweeps). Due to the symmetry of the system with respect to the middle dot, D2 [6,7], the bistability exhibits itself only for the sweeps of the input bias. Therefore, to study the bistability one needs to sweep the input and step the clock signal. The rate of the sweep must be chosen to exclude dynamic errors which occur when the time of the input bias sweep, Δt, over one period of single-electron transitions in the phase diagram, $\Delta V = e/C_{IN}$, is comparable to the tunneling time $\tau \sim R_J C_J$, where R_J and C_J are the capacitance and resistance of the tunnel junctions, and C_{IN} is input gate capacitance. For our set of parameters the maximum sweep rate therefore is limited by $\Delta V/\Delta t < e/(\tau C_{IN}) \sim 10^8$ V/s. In the experiments we use sweep rate of 10^{-1} V/s. Fig. 2 shows phase diagrams sensed by the electrometer E1 for opposite scan directions and measured at three different temperatures: 92, 190, and 320 mK. On the resulting phase

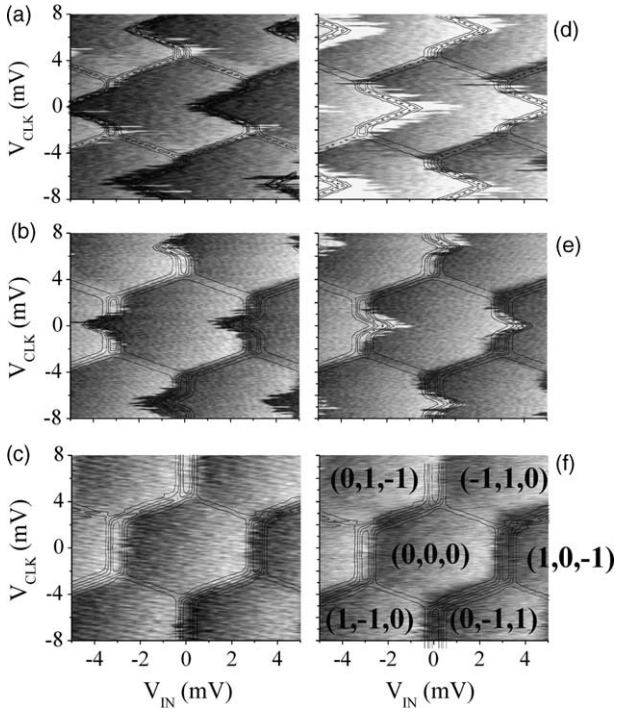

Fig. 2. Phase diagrams of the single-electron latch measured at different temperatures for two directions of the input bias sweeps measured by E1 (a and d) 92; (b and e) 190; (c and f) 320 mK. Sweeps (a–c) are from positive to negative V_{IN}, sweeps (d–f) are from negative to positive V_{IN}. Theoretical calculations are superimposed with measurements. Numbers in the brackets correspond to uncompensated electron charges on D1, D2, and D3 accordingly.

diagram the bistability exhibits itself as a distinctive triangular-shaped area; when the input voltage swept in the opposite directions the triangle extends in the directions of the sweeps. A sum of the two triangles forms a rhombus-shaped region [6] (note that a cross-section along horizontal axis of the rhombus shows a hysteresis loop—this is the 'memory area' (Fig. 3a)). In Fig. 2(a–c) the differential input signal V_{IN} is varied from -5 to $+5$ mV during each scan and then the clock signal V_{CLK} is increased by 0.2 mV after each V_{IN} scan, taking it from -8 to 8 mV. Fig. 2(d–f) shows the phase plot for scanning V_{IN} from negative to positive voltages and stepping V_{CLK} also from negative to positive voltages. It is clear from the graph that as the temperature increases, the bistable region gradually shrinks in size and eventually vanishes, so that above certain temperature T_{MAX} phase diagram does not depend anymore on the direction of the sweep. The phase diagram for $T > T_{MAX}$ always corresponds to the ground state of the system.

For better understanding of the temperature dependence of the bistability in SEL we performed numerical simulations using parameters obtained from experiments. We assume the capacitance of the junctions to be the same as for the electrometers and neglected the capacitances of the islands in MTJs. Capacitances of the SEL gates (C_{IN}, C_{CLK}, C_E) are calculated from the periods of Coulomb blockade oscillations. Coupling capacitanes, C_C are measured using

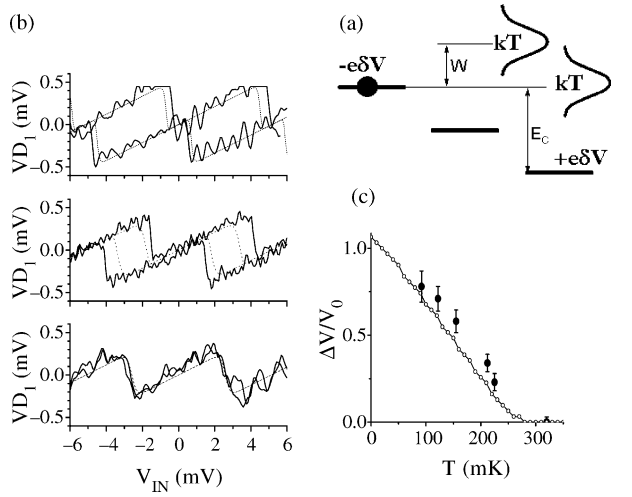

Fig. 3. (a) Energy diagram illustrating temperature smearing of the locking barrier, V_{IN} shown corresponds to the 'equilibrium border' [7]. If not for the Coulomb barrier, electron would be transferred from the D1 to D3. (b) Measured and calculated electrostatic potentials on D1 for input bias swing at $T = 122$ mK (top), 212 mK (middle) 320 mK (bottom). (c) Temperature dependence of the relative size of bistable area. V_0 is the period of the phase plot for input bias, $V_0 = e/C_{IN}$; ΔV is a width of the hysteresis loop. The fact that $\Delta V/V_0 > 1$ at $T = 0$ K means that system becomes multistable [6] at very low temperatures.

test single-electron transistors with gates having the same geometry as C_C. To simulate a latch we use a model based on orthodox theory of Coulomb blockade [15], where the circuit is described by charge configurations, which are determined by the number of uncompensated electrons on each of the metal islands. The free energy of charge configuration is the electrostatic energy of the capacitors and junctions minus the work done by the voltage sources (V_{IN}, V_{CLK})

$$F = \frac{1}{2}\begin{bmatrix} q \\ q' \end{bmatrix}^{T} C^{-1} \begin{bmatrix} q \\ q' \end{bmatrix} - v^{T} q' \tag{1}$$

where C is the capacitor matrix including all the junctions and capacitors, v is the column vector of applied voltages, and q and q' are the column vectors of dot charges and charges on the input leads. At zero temperature, the number of electrons on each island is an integer. The equilibrium charge configuration is the one that has the minimum free energy. A tunneling event happens only when the free energy decreases. At finite temperatures, however, even if the free energy increases, there is still a certain probability that a tunneling event might happen. The transition rate of tunneling between two charge configurations is given by

$$\Gamma_{ij} = \frac{1}{e^2 R_T} \frac{\Delta F_{ij}}{1 - e^{-\Delta F_{ij}/(kT)}} \tag{2}$$

where R_T is the tunneling resistance, ΔF_{ij} is the energy difference between the initial state i and final state j.

The usual approach for simulating single electron system is statistical Monte–Carlo method, which calculates all

the possible tunneling events, chooses one of them randomly and then weights it according to its probability. Because SEL operates close to the ground state, fewer states needed to be considered. We can therefore employ a master equation approach where P is the vector of state probabilities (the probability of each of the

$$\frac{dP}{dt} = \Gamma P \tag{3}$$

possible configurations) and Γ is the transition matrix. P is the ensemble average of the charges in the islands. Note that cotunneling is not included in our model. For each V_{CLK}, we sweep the V_{IN} from negative to positive values and solve the time dependent master equation, then reverse the direction of the sweep and solve it again; the sweep rate is the same as in the experiment. The results of the calculations are shown in Fig. 2 as lines superimposed with the experimental data. Each line on the diagram corresponds to a transition between charge configurations. As it was pointed out in [6], the crossing of any phase boundary outside of the bistable regions involves one tunneling event, whereas crossing the borders of the bistable region involves the transfer of two electrons. Charge states are marked by the numbers where ($n1$–$n3$) are excess charges on D1–D3. Positive number represents the number of electrons and negative number represents the number of holes, while the system as a whole remains charge neutral. In equilibrium state (i.e. for $T=320$ mK), each hexagonal area in Fig. 2(c and f) represents a charge configuration for which the system has the lowest energy. To simplify the calculations for every border on the phase plot we consider only adjacent charge configurations, which is a good approximation for temperatures $kT<E_C$. (In our experiment $E_C\sim0.8$ meV$=k_B\times9.3$ K). When $V_{CLK}=0$, $V_{IN}=0$, the system is in (0, 0, 0) configuration, which is the ground state of the system for this combination of biases. If for $V_{CLK}=0$ we change differential input bias toward positive 5 mV value, at approximately 2 mV the equilibrium charge border is crossed, and the charge configuration (0, 0, 0) becomes metastable. At low temperatures, however, the system cannot switch into ground state (1, 0, −1) configuration because of the Coulomb barrier created by D2 (Fig. 3a). Only when this barrier is surmounted by extra input bias, the charge configuration can be changed. If the direction of the scan is then reversed, charge configuration stays at (1, 0, −1) until high enough negative input bias is applied. With the increase of temperature, the tunneling rate increases, so an electron can overcome the energy barrier for reaching ground state charge configuration for smaller input bias deviations from the equilibrium border. At certain temperature the bistability disappears as it is no longer possible to keep the system in a local energy minimum. Fig. 3b shows measured and calculated electrostatic potentials on D1 for $V_{CLK}=0$ as a function of the input bias at different temperatures. A wide hysteresis loop could be clearly seen at low temperatures. In Fig. 3c we plotted the measured and calculated size of the bistable region along V_{IN} as a function of temperature. As it can be seen from Fig. 3a and c the size of the bistable region shrinks in size with temperature increase until it disappears at $T_{MAX}\sim0.3$ K. Note that the charging energy barrier which controls the tunneling between dots $W\approx E_{C2}$. Thus for the operation of the clocked QCA-type logic the height of this barrier has to fulfill the condition $W\geq15$ kT.

To summarize, we present an experimental investigation of the temperature dependence of the locked mode in metal-dot based clocked QCA device. The experimental results are in very good agreement with the orthodox Coulomb blockade theory for thermally activated electron escape mechanism [15]. An important conclusion which comes from this work is that for successful operation of clocked QCA at room temperature, the energy barrier separating the charge states must of the order of 1 eV.

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References

[1] C.S. Lent, et al., Quantum cellular automata, Nanotechnology 4 (1) (1993) 49–57.
[2] R.W. Keyes, R. Landauer, Minimal energy dissipation in logic, IBM J. Res. Dev. 14 (1970) 152–157.
[3] C.S. Lent, P.D. Tougaw, W. Porod, PhysComp '94: Proceeding of the Workshop on Physics and Computing, PhysComp '94: Workshop on Physics and Computing, IEEE Computer Society Press, 1994.
[4] C.S. Lent, P.D. Tougaw, A device architecture for computing with quantum dots, Proc. IEEE 85 (1997) 541–557.
[5] K.K. Likharev, A.N. Korotkov, Single-electron parametron: reversible computation in a discrete-state system, Science 273 (1996) 763–765.
[6] A. Korotkov, K. Likharev, Single-electron-parametron-based logic devices, J. Appl. Phys. 84 (11) (1998) 6114–6126.
[7] G. Toth, C.S. Lent, Quasiadiabatic switching for metal-island quantum-dot cellular automata, J. Appl. Phys. 85 (5) (1999) 2977–2982.
[8] A.O. Orlov, et al., Clocked quantum-dot cellular automata shift register, Surf. Sci. 532–535 (2003) 1193–1198.
[9] R.K. Kummamuru, et al., Power gain in quantum-dot cellular automata, Appl. Phys. Lett. 81 (2002) 1331–1334.
[10] A.O. Orlov, et al., Experimental demonstration of a latch in clocked quantum-dot cellular automata, Appl. Phys. Lett. 78 (2001) 1625–2627.
[11] M. Liu, C.S. Lent, unpublished.
[12] T.A. Fulton, G.H. Dolan, Observation of single-electron charging effects in small tunnel junctions, Phys. Rev. Lett. 59 (1987) 109–112.
[13] D.V. Averin, A.A. Odintsov, Macroscopic quantum tunneling of the electric charge in small tunnel junctions, Phys. Lett. A 140 (5) (1989) 251–257.
[14] G.L. Snider, et al., Jpn. J. Appl. Phys. 38 (1999) 7227.
[15] K.K. Likharev, Correlated discrete transfer of single electrons in ultrasmall tunnel junctions, IBM J. Res. Dev. 32 (1988) 144–158.