# Power Gain in a Quantum-dot Cellular Automata (QCA) Shift Register

Ravi K. Kummamuru, Alexei O. Orlov, Geza Toth[1], John Timler, Ramasubramaniam Rajagopal,
Craig S. Lent, Gary H. Bernstein, and Gregory L. Snider.

*Dept. of Electrical Engineering, University of Notre Dame,*
*Notre Dame, IN 46556, Phone: (219) 631-9011*

## Abstract

In this paper we discuss an experiment that demonstrates power gain in a Quantum-dot Cellular Automata (QCA) shift register. Power gain is essential in any electronic system for the restoration of logic levels. The clock signal plays an important role in providing power gain in QCA devices as it can be used as a source of energy for the system. We discuss how this can be achieved in a QCA shift register and experimentally demonstrate a power gain greater than unity.

## 1. Introduction

Quantum-dot Cellular Automata (QCA) is a device architecture that uses position of electrons in quantum-dot arrays to implement digital logic [1]. Each QCA cell is a bistable system with two degenerate ground states. Switching between the two states occurs when discrete electrons tunnel between the dots from one ground state to the other. The voltage levels associated with binary logic are set by the charging energy $(e^2/C_\Sigma)$ of the dots rather than external power lines as in conventional transistor based digital circuits.

Dissipation of energy is inevitable in any practical electronic system. Weak signals could result from a loss of energy in the system or due to problems in fabrication. Therefore, a mechanism for power gain is necessary in any electronic circuit, in order to restore logic levels. In current digital integrated circuits, power supply lines and transistors are used to boost weak signals to acceptable levels. In QCA devices where power supply lines are not used, the clock signal acts as the source of energy to achieve power gain in the system. Clocked control in QCA devices was proposed as a way to achieve quasi-adiabatic switching or ground state computing [2]. A scheme for implementation of clocking in metal-based QCA devices was proposed by Toth et. al. [3]. A clocked QCA device [4], and a QCA latch [5] were recently fabricated and tested.

In this paper, we demonstrate power gain in a two-bit QCA shift register. We will also discuss the effect of errors on the operation of the device and its relation to power gain.

## 2. Device Fabrication

There are a number of technologies that can be used for fabrication of QCA devices. The basic requirements for implementation of QCA are charge quantization in quantum dots or islands, and single-electron tunneling between the dots. Nanostructures, molecular electronics, aluminum/aluminum oxide and semiconductor-based technologies are some of the possible technologies for fabrication of QCA devices. The device that will be discussed in this paper was fabricated using the aluminum tunnel junction technology [6]. Here, the 'quantum dots' are formed by islands of aluminum. A thin layer of aluminum oxide sandwiched between two layers of aluminum, forms the tunnel junctions between islands. The area of tunnel junctions determines the junction capacitance which dominates total dot capacitance and hence the

---

1 Current address: Theoretical physics, Oxford University, 1 Keble Rd, Oxford, OX1 3NP, UK.
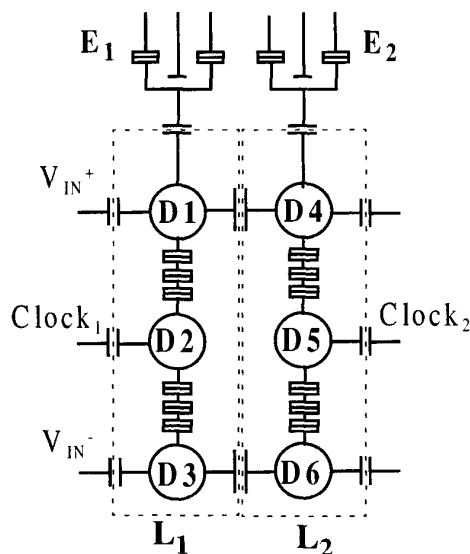
Figure 1: Schematic diagram of a QCA shift register.

charging energy of the device ($E_C = e^2/C_\Sigma$). Single electron charging effects are observed when the charging energy of the device is much greater than the characteristic energy of thermal fluctuations i.e., $E_C \gg k_BT$. For our devices, the area of tunnel junctions is about 50nm by 50nm, which limits the temperature of operation of the device to below 200mK. The experiment is performed in a dilution refrigerator with a base temperature of about 15mK, in a magnetic field of 1T to suppress superconductivity in aluminum.

The schematic diagram of the device, a QCA shift register is shown in Fig. 1. It consists of two QCA latches capacitively coupled to each other. Each latch is made up of three dots or islands. The top and the bottom dots store the binary information while the middle dot is used as an adjustable barrier. A clock signal is applied to the middle dot to modulate its potential and control electron tunneling between the top and the bottom dots. Each latch is a short-term memory element capable of storing a bit for one or more clock cycles. The operation of a QCA latch is discussed in

detail in references [3] and [5]. Three tunnel junctions are used between dots instead of a single junction to enhance retention time of the latches. Dots $D_1$, $D_2$ and $D_3$ form latch $L_1$ while dots $D_4$, $D_5$ and $D_6$ form latch $L_2$. $E_1$ and $E_2$ are the electrometers used to measure the potentials on dots $D_1$ and $D_4$ respectively.

## 3. Operation of a Shift Register

A QCA shift register is a line of latches where binary information can be transferred in a sequential manner from one latch to the next. Clock signals control switching in each latch. Phase-shifted clock signals are used to switch the latches sequentially and move bits along the shift register one latch at a time[3]. We use a three-phase clock to operate the shift register.

The signals applied for the operation of a two-bit shift register are shown schematically in Fig. 2. Differential input signals $V_{IN}^+$ and $V_{IN}^-$ are applied to the first latch (latch 1) through capacitors $C_1$ and $C_3$. When clock signal (clock 1) is applied to the latch, it switches in the direction defined by the input. Once latch 1 switches, the input can be removed without losing the bit stored in latch 1. Latch 1 then acts as an input to latch 2. When clock 2 is turned on, latch 2 switches in the direction defined by latch 1, and the binary information gets copied into latch 2. Now, latch 1 can be turned off and the bit is stored in latch 2. As new bits appear at the input, older bits move forward along the shift register one step at a time.

Figure 3 depicts the sequence of events in the operation of a shift register. At time $t_0$ all the inputs and latches are off. At $t_1$, the input is applied. At $t_2$, latch 1 is turned on by applying clock 1. At $t_3$, the input is removed while latch 1 remains on. At $t_4$, latch 2 is turned on by applying clock 2. At $t_5$, latch 1 is turned off by removing its clock signal. At $t_6$, a new input is
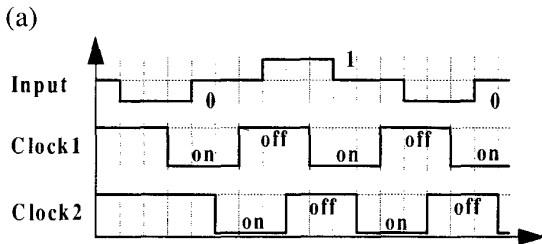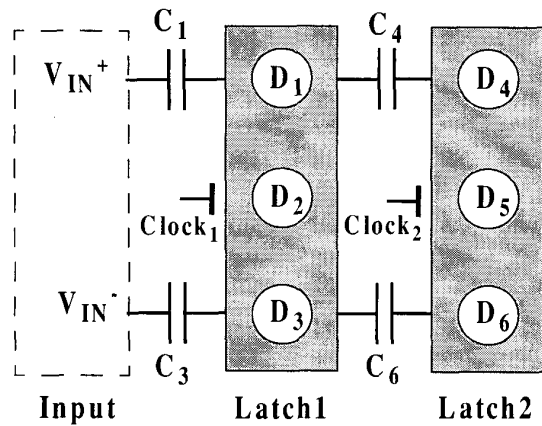
(a)



(b)

Figure 2: (a) Schematic diagram of a shift register. (b) Input and clock signals applied to the shift register to transfer bits from the along the line of latches.

applied to latch 1. And finally, latch 2 is turned off and the system returns to the state it was in at $t_1$. The path followed from $t_1$ to $t_6$ represents the periodic operation of the two-bit shift register controlled by a three-phase clock.

## 4. Power flow in a QCA shift register

In order to verify power gain in the shift register, we measure the power flow in the system. Each latch is considered a black-box with an input, an output, a clock signal and a dissipative coupling to the environment. The input and the output signals form the information-bearing signals while the clock is a control signal which also acts as a major source and sink of energy. When a weak input signal is applied to a latch, the clock provides the addi-
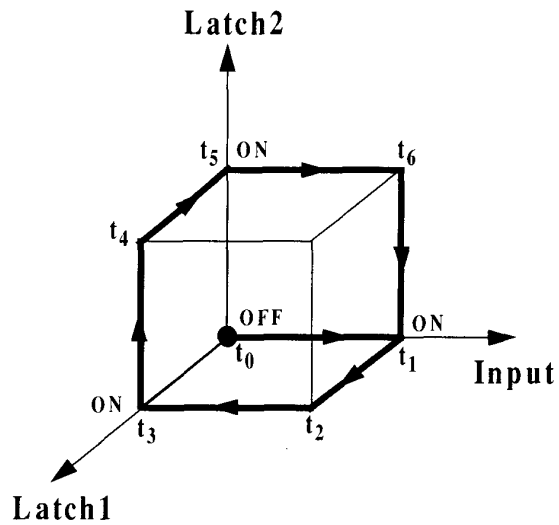


Figure 3: Diagram depicting the switching scheme of the shift register. The arrows show the sequence of switching events.

tional amount of energy required to switch the latch and pull up the logic level [7]. In order to measure change in the signal power as it passes through a latch, we focus on latch 1 and measure its input and output power. The ratio of the output to the input signal power gives the power gain that occurs in latch 1.

$$\text{Power Gain} = \frac{P_{out}}{P_{in}} = \frac{W_{out}}{W_{in}}$$

The work done on a device by an input (V), applied through a capacitor (C) is given by

$$W = \int_0^t V_{(t)} \frac{d}{dt} Q_c(t) dt$$

where $Q_c(t)$ is the charge on capacitor C. For the input $V_{IN+}$ this equation becomes

$$W = \int_0^t V_{IN+}(t) d[C_1(V_{IN+}(t) - V_{D1}(t))]$$

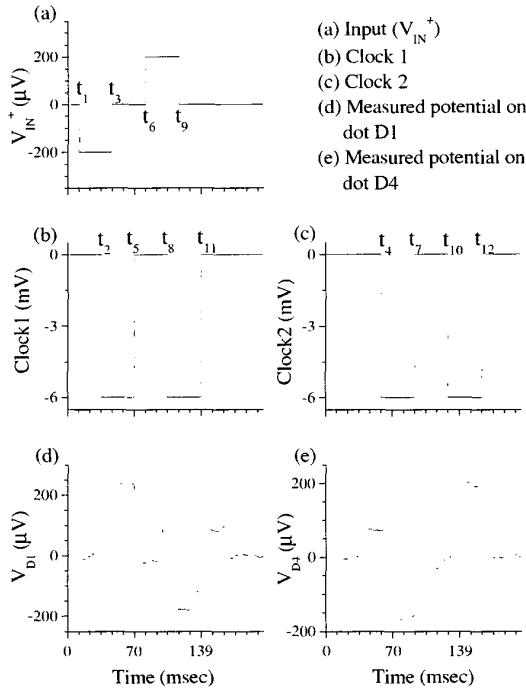where $V_{D1}$ is the potential on dot $D_1$.

Figure 4: Timing diagram showing the input and clock signals applied to the shift register and the measured dot potentials on the two latches.

When the input (V) to a latch is plotted against the charge stored in the capacitor (Q), the area under the plot gives the work done by the input on the latch. If after one clock cycle system returns to the initial state, the Q-V plot forms a loop and the area enclosed by the loop gives the work done on the latch.

## 5. Experiment

In an ideal shift register power gain is unity for all latches since all the voltage levels and coupling capacitors are identical. We examine what happens when a weak signal is applied to a latch. We use weak input coupling capacitors $(C_1 = C_3 = C_4 / 4 = C_6 / 4)$ to simulate an imperfection in the device.

The input and clock signals applied to the shift register and the corresponding experimentally measured dot potentials are shown in Fig. 4.
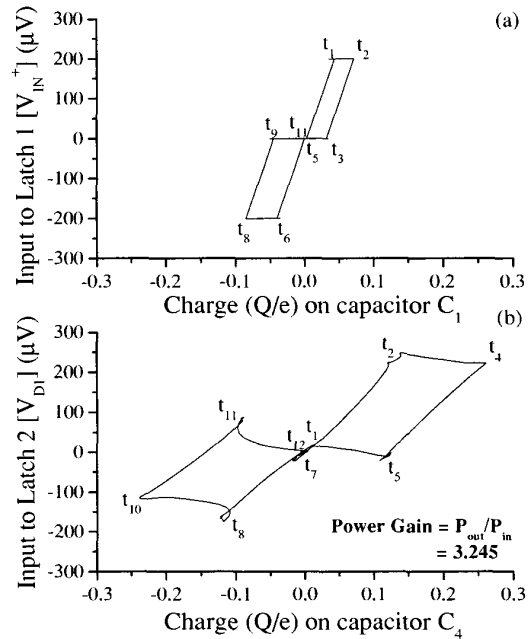


Figure 5: Q-V plot of the data shown in Fig. 4 . (a) Q-V plot for latch 1 for the input $V_{IN}^+$ applied through the capacitor $C_1$. Area enclosed by the plot gives the work done by the input on latch 1. (b) Q-V plot for latch 2 with latch 1 as its input. Area enclosed by the plot gives the work done by latch 1 on latch 2.

The shift register is operated for two clock cycles and two bits, a '0' and a '1' are transferred from the input to latch 2 before returning the system to its initial state. The measured potentials on dots $D_1$ and $D_4$ are shown in Fig. 4(d)and (e). The inputs $V_{IN}^+$ and $V_{IN}^-$ are applied to latch 1 whereas latch 1 acts as the input to latch 2. When the clocks are applied, each latch switches according to its input. It should be noted that each QCA latch is also an inverter and so each bit gets flipped at latch 1 and flipped back at latch 2.

Figure 5 shows the Q-V plots corresponding to the data measured in Fig. 4. The data was averaged over 10 scans to eliminate noise. The data Figure 5 (a) shows the work done by the input

signal on latch 1 while Fig. 5(b) shows the work done by latch 1 on latch 2. Various points on the Q-V plot represent various stages in the experiment. At $t_1$, the input is applied to latch 1, and the charge across the capacitor $C_1$ ($Q_{C1}$) changes by a small amount. At $t_2$, the clock is applied to latch 1 and it switches. The charge on the capacitor changes due to a change in the potential on dot $D_1$. Latch 1 now acts as an input to latch 2 and $Q_{C2}$ changes by a small amount. At $t_3$, the input is removed but latch 1 doesnot switch off. At $t_4$, the clock is applied to latch 2 and it switches, changing $Q_{C2}$. At $t_5$, latch 1 is switched off by removing its clock. Latch 1 returns to its initial state while latch 2 doesnot switch off. At $t_6$, a new input is applied to latch 1. At $t_7$, latch 2 is switched off, and the cycle is repeated for the new input.

The area enclosed by the loops in the Q-V plots gives the work done in each case. For both Fig. 5(a) and Fig. 5(b), the Q-V plots form paths looping in the clockwise direction, indicating that the work done by $V_{IN}^{+}$ on latch 1 and the work done by latch 1 on latch 2 are positive. The work done by $V_{IN}^{-}$ would be similar since the latch is symmetric. A weak coupling from the $V_{IN}^{+}$ to latch 1 results in a smaller work done on the system by the input. However, the latch still switches since the clock does most of the work required for switching. As a result, the output work done by latch 1 i.e. the work done by latch 1 on latch 2 is greater than the work done by the input on latch1. The ratio of output work to input work, per clock cycle gives power gain. For the input ($V_{IN}^{+}$) shown in Fig. 4 power gain in latch 1 is 3.245. The same experiment is performed with different input magnitudes. An input of 0.5mV yields a power gain of 1.93 while an input of 0.1mV yields a power gain of 6.12. For much larger inputs, power gain could becomesmaller than unity. Therefore, the clock
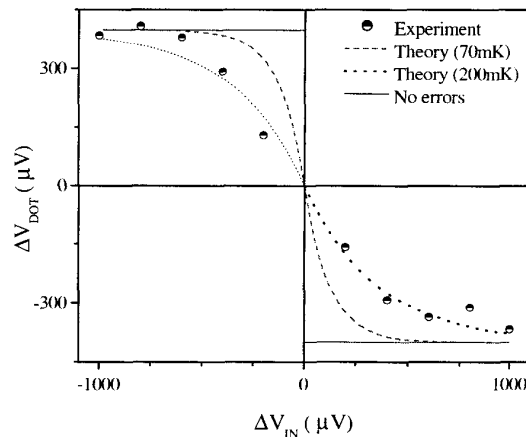


Figure 6: The output vs input chatacteristics of a latch averaged over a 1000 scans. $V_{IN}$ is the input applied to the latch while $V_{OUT}$ is the dot potential generated on the latch due to switching. Small inputs are easily affected by error sources and cause the average of the output to diminish. The characteristics predicted by considering thermal error sources at two temperatures are also shown.

provides only the amount of energy that is required for switching and pulls up the logic levels when a weak input or a weak coupling occurs in the system.

Thermal and electrical noise can cause errors in switching in a latch [8]. Such errors have sources and mechanisms that are unrelated to the current discussion on power gain , but play a role in deciding the practical limits on the size of the input and the power gain. The size of the input signal required for switching a latch can be very small due to bistable saturation in QCA devices [9]. However, small inputs are more likely to be affected by noise sources and hence result in switching errors. Therefore, error sources set a lower limit on the size of the input signal and hence an upper limit on the power gain.

Figure 6 shows a statistical average of the input and output for latch 1 over a 1000 scans. Errors in switching in the latch due to thermal and electrical noise sources result in a '0' instead of a '1' or vice versa and when aver-

aged over a number of scans would result in a reduction in the size of the average output. In an ideal case where no errors occur, the latch shows an ideal sigmoidal characteristics, and a very small input would cause the latch to switch correctly. However, in a practical device, a region around the centre of the x axis (Fig. 6) cannot be used. Switching error probabilities fall exponentially with the magnitude of input. As QCA devices are made smaller, charging energies and consequently voltage swings become larger, and the effect of error sources on the operation of the devices would be minimized.

## 6. Conclusions

Power gain is an essential feature of any electronic system. In QCA devices it is achievable by using the clock signal as a source of energy to the system. The clock signal does extra work on the system whenever a need appears in the form of a weak input signal. The clock signal provides only the amount of energy required to restore logic levels in the system. We have demonstrated in a QCA shift register that when a weak input occurs due to dissipation or fabrication imperfections, power gain greater than unity occurs by the clock supplying energy to the system, restoring logic levels.

## References

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum cellular automata," Nanotechnology, vol. 4, pp. 49-57, 1993.

[2] C. S. Lent and P. D. Tougaw, "A Device Architecture for Computing with Quantum Dots," Proceedings of the IEEE, vol. 85, pp. 541-557, 1997.

[3] G. Toth and C. S. Lent, "Quasiadiabatic switching for metal-island quantum-dot cellular automata," Journal of Applied Physics, vol. 85, pp. 2977-2982, 1999.

[4] A. O. Orlov, I. Amlani, R. K. Kummamuru, R. Ramasubramaniam, G. Toth, C. S. Lent, G. H. Bernstein, and G. L. Snider, "Experimental demonstration of clocked single-electron switching in quantum-dot cellular automata," Applied Physics Letters, vol. 77, pp. 295-297, 2000.

[5] A. O. Orlov, R. K. Kummamuru, R. Ramasubramaniam, G. Toth, C. S. Lent, G. H. Bernstein, and G. L. Snider, "Experimental demonstration of a latch in clocked quantum-dot cellular automata," Applied Physics Letters, vol. 78, pp. 1625-1627, 2001.

[6] T. A. Fulton and G. H. Dolan, "Observation of Single-Electron Charging Effects in Small Tunnel Junctions," Physical Review Letters, vol. 59, pp. 109-112, 1987.

[7] J. Timler and C. S. Lent, "Power Gain and Dissipation in Quantum-dot Cellular Automata," Submitted to Journal of Applied Physics.

[8] A. O. Orlov, R. K. Kummamuru, R. Rajagopal, C. S. Lent, G. H. Bernstein, and G. L. Snider, "Clocked Quantum-dot Cellular Automata Devices : Experimental Studies," to be presented at IEEE-NANO 2001.

[9] C. S. Lent, P. D. Tougaw, and W. Porod, "Bistable saturation in coupled quantum dots for quantum cellular automata," Applied Physics Letters, vol. 62, pp. 714-16, 1993.