Operation of a Quantum-Dot Cellular Automata (QCA) Shift Register and Analysis of Errors

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***Abstract*—Quantum-dot cellular automata (QCA) is a digital logic architecture that uses single electrons in arrays of quantum dots to perform binary operations. A QCA latch is an elementary building block which can be used to build shift registers and logic devices for clocked QCA architectures. We discuss the operation of a QCA latch and a shift register and present an analysis of the types and properties of errors encountered in their operation.**

***Index Terms*—Error rate, latch, logic, quantum-dot cellular automata (QCA), shift register, single electron.**

I. Introduction

THE last four decades has been an impressive period of development for microelectronics, and has resulted in integrated circuits with device densities of tens of millions of transistors per chip. Such high levels of integration and continual push toward smaller transistors has caused an increase in nonideal device behavior, such as leakage currents through the gate, resulting in chip power density levels comparable to a hot plate and set to approach that of nuclear reactors. Quantum-dot cellular automata (QCA) is a binary logic architecture which can miniaturize digital circuits to the molecular levels and operate at very low power levels [1]. QCA devices encode and process binary information as charge configurations in arrays of coupled quantum dots, rather than current and voltage levels. In the last few years, several basic QCA elements: a QCA cell, small binary wire, and digital logic gate, have been demonstrated [2]. However, in these devices the power gain needed for the operation of large QCA arrays was not achievable since the only source of energy was the signal input. To overcome this obstacle, clocked control of the QCA circuitry was proposed in [3]. Clock controlled QCA systems have many advantages over edge-driven cellular architectures. The most important of these are the ability to achieve power gain and to use pipelined architectures. In clocked devices, switching is caused due to the clock signal while the input decides the direction of switching. The clock signal acts as a major source of energy to the device. Power gain is possible since a weak input signal can be augmented by the clock. Controlling tunnel barriers using a clock signal also allows cells to be locked into a particular state, giving rise to memory. A simple binary logic structure that is capable of clocking was discussed by Keyes and Landauer in [4] as early as 1970. The proposed element consists of a particle (e.g., an electron) in a potential well that can be varied between a monostable and a bistable states by external means. The essential steps in its operation are as follows. Initially the device is in the monostable state as shown in Fig. 1(a). To write a bit into the device, the input is applied and the barrier is slowly raised [Fig. 1(b)]. The magnitude of the input signal can be small since it only has to provide a preferential direction for switching. The particle settles into the state suggested by the input. The barrier is then raised high enough to trap the particle in this state [Fig. 1(c)]. Now the bit is stored in the device and the input can be removed without affecting the device. To erase the bit, the barrier is lowered and the potential well is brought back to the monostable state [Fig. 1(d)].

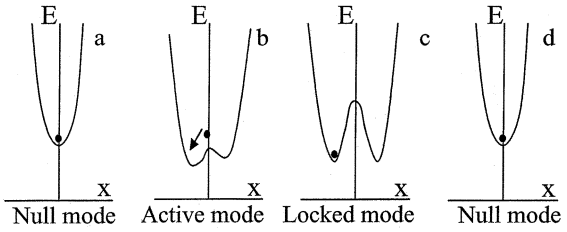

Fig. 1. Simplified diagram of the Keyes–Landauer clocking scheme. Depicts the three main stages involved in varying the potential well from a monostable to a bistable state by modulating a barrier.

A similar scheme of operation was proposed for QCA devices by Lent *et al.* [3], called adiabatic switching. In semiconductor QCA devices the barriers are formed by depletion in the substrate, and can be modulated easily using voltages applied through gates. In implementations with fixed barriers (like the device described here), the barrier is formed by an oxide layer and hence cannot be modulated. A way to incorporate clocking in systems with fixed barriers was proposed in [5], [6]. In this implementation, an extra dot is added between the top and bottom dots, whose potential acts as a barrier that can be modulated using a clock signal.

II. Device Fabrication

The devices were fabricated using Al/AlO_x tunnel junctions. The technique uses a combination of electron beam lithography and dual angle evaporation [7] to deposit thin lines of aluminum that form overlaps of a very small area. These lines of aluminum form the quantum "dots" and a thin layer of aluminum oxide sandwiched within the overlaps, forms the tunnel junctions. The total capacitance depends on the area of tunnel junc-

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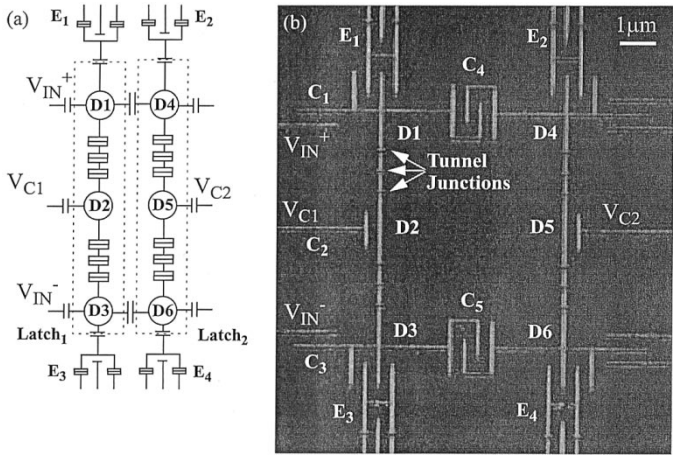


Fig. 2. (a) Schematic diagram of a QCA shift register. (b) Scanning electron micrograph of the shift register.

tions as well as the size of the island but is dominated by the former. The charging energy of an island is given by the equation $E_C = e^2/C_\Sigma$ where C_Σ is the total capacitance of the island. Single electron effects are observed when the charging energy of the device is much greater than the characteristic energy of thermal fluctuations i.e., $E_C \gg k_bT$. For our devices, the tunnel junction area is about 50×50 nm^2. This results in a junction capacitance of about 300 aF and limits the operating temperature of the device to below 200 mK.

Fig. 2(a) shows the schematic diagram of a QCA shift register. Fig. 2(b) shows a scanning electron micrograph of the device. The shift register consists of two QCA latches [8] capacitively coupled to each other. D_1–D_3 are the three aluminum islands that form latch L_1 while D_4–D_6 form latch L_2. To measure electrostatic potentials on the dots single-electron transistors (SET) [9] are used as electrometers E_1–E_4.

Capacitances in the circuit are measured in two ways. Capacitances of all gates to the electrometers were extracted from the periods of coulomb blockade oscillations. Other capacitances like the coupling capacitors C_1, C_3, C_4 were estimated by fabricating additional test devices consisting of single-electron transistors, coupled to gates of the same geometry as the corresponding capacitor in the latch, and its capacitance calculated from the period of coulomb blockade oscillations.

The experiment is performed in a dilution refrigerator with a base temperature of about 15 mK. The device is placed in an ambient magnetic field of 1 T to suppress superconductivity in aluminum. The measurements have been conducted on multiple devices of the same design.

III. QCA Latch

The QCA latch is made up of three aluminum islands connected by tunnel junctions as shown in Fig. 2(a). A clock signal is applied to the middle dot to vary the potential on it so that it acts as a barrier for tunneling between the dots. Inputs are applied to the top and the bottom dots of the latch either by a neighboring latch or by external input voltages. To describe the operation of a QCA latch it is helpful to have a nomenclature that describes the various states involved in switching a latch depending on the clock signal [5]. When no clock signal is applied and all the dots are neutral, we say that the latch is in the "null" state and holds no information. As the clock signal is applied, the barrier height increases, and the polarization of the latch takes on a definite value determined by the input. We call this the "active" state. When the barrier height is large enough to suppress switching over the relevant time scale, we say the latch is in the "locked" state.

In the locked state, the latch polarization is independent of the input and it acts as a single-bit memory element. The primary mechanism responsible for the loss of information in the latch is cotunneling [10], where n electrons tunnel simultaneously across n tunnel junctions with the net effect of a transfer of one electron from one end to the other. To increase the hold time of the latch, by suppressing co-tunneling, multiple tunnel junctions are used to connect the dots. However, as a result, additional small islands are formed between the tunnel junctions. In turnstile devices [11], extra gates are used to compensate for random background charges on these intermediate islands. However, extra gates are not necessary in our device. First, these islands are made much smaller to reduce the influence on them from the gates. Second, we choose appropriate gate bias voltages where the influence of the background charge is minimal. This is possible since the device operating characteristics are periodic in both V_{IN} and V_{CLK} coordinates but not periodic with respect to background charge.

To characterize the device and determine a bias point for its operation, we measure the "phase plot" for the device. A phase plot is a gray-scale map of the electrostatic potential on a dot versus the differential input V_{IN} ($V_{IN}^+ = V_{IN}$ applied to the top dot, $V_{IN}^- = -V_{IN}$ applied to the bottom dot), and the clock voltage V_C applied to the latch. Fig. 3 shows the phase plot of the top dot D_1 of latch L_1, for different scan directions. Electrostatic potential on the dots is measured by first measuring the conductance of the electrometer coupled to the dot. Then using the ratio of the gate to coupling capacitances of the electrometer, change in potential on the dot is calculated. The darker regions represent lower dot potential and the brighter regions represent higher dot potential. The range of dot potentials from the darkest to the brightest regions in the phase plot is -0.2 mV to $+0.2$ mV. Sharp transitions between dark and bright regions represent boundaries between charge states of the latch. It is at these boundaries that electrons tunnel from one dot to another. By combining the phase plots of the three dots, the various charge transitions between dots in the latch can be traced. The white lines in Fig. 3(a) depict the boundaries of these charge transitions. Fig. 3 shows the phase plot with reference to a particular bias setting. Biases are applied to the dots as DC offsets through the same gate capacitors used for the input and clock signals.

It is evident from Fig. 3 that the phase plot in certain regions depends on the direction of the scan. In these regions (dotted line in Fig. 3), the system is bistable. These regions of bistability are critical for the operation of the latch as a memory element. Let us first consider the phase plots where the clock voltage is being scanned [Fig. 3(a) and (b)]. When the clock voltage is scanned, the potential on the middle dot of the latch is being continuously varied. At a certain clock voltage, it becomes favorable for an

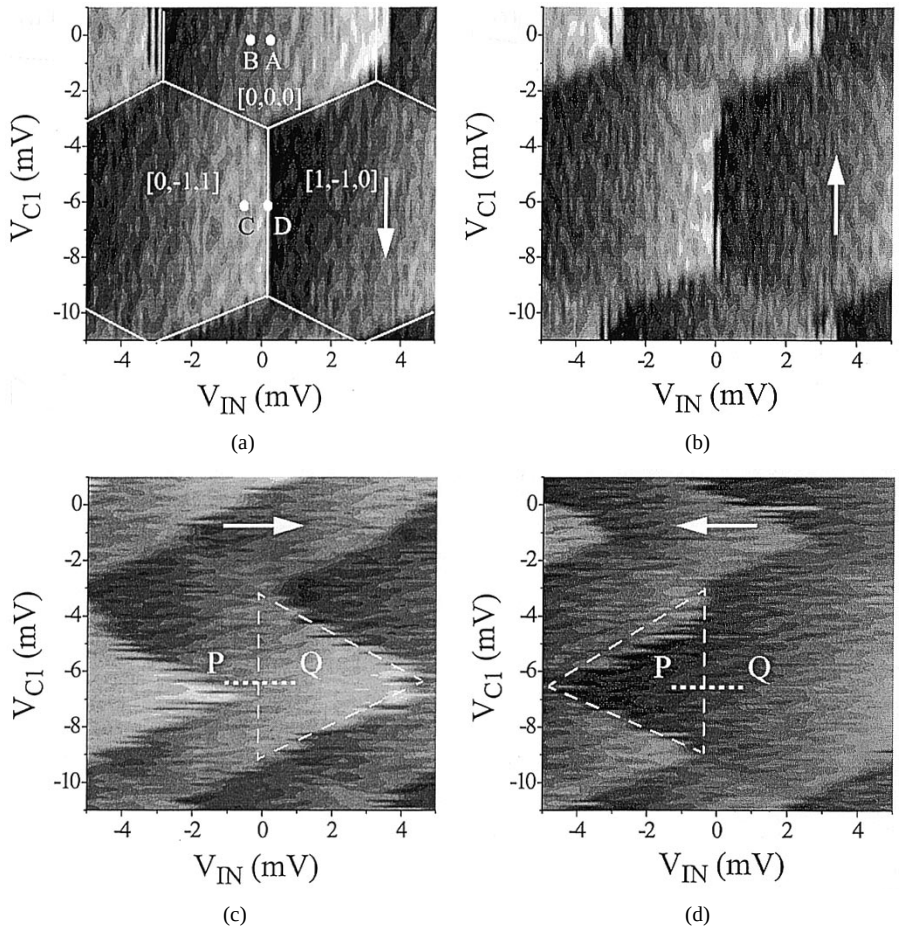


Fig. 3. Phase plot for dot D_1 of latch L_1 for four different scan directions: (a) clock negative, (b) clock positive, (c) input positive, and (d) input negative. Solid white lines represent the boundaries of charge states where electron tunneling occurs. Numbers in brackets (for example $[0, -1, 1]$) denote the number of extra electrons in the top, middle, and bottom dots respectively and represent the charge configuration of the latch in that region. Dotted line shows the extent of the bistable region.

electron to be moved from the middle dot to either the top or the bottom dot. The electron would tunnel into the dot which takes the system to the least energy state which is its ground state. Therefore, when the clock voltage is scanned the phase plot shows the ground state of the latch. However, when the input is scanned [Fig. 3(c) and (d)] in the region of bistability, the system cannot reach its ground state as easily since the middle dot acts as a barrier. Once the input is large enough to force the electron to the other dot, the system reaches its ground state. The region of bistability is discussed further in the section on decay errors.

The operation of the latch involves the following main steps. Initially the latch is in the null state and all the dots are neutral [point A in Fig. 3(a)]. A small input is applied to the latch [point B in Fig. 3(a)] and then by changing the clock, the latch is brought to the ground state for that particular input [point C in Fig. 3(a)]. Once the latch is in the bistable region, it retains its state even after the input is removed [point D in Fig. 3(a)]. When the clock is removed the latch goes back to the initial null state [point A in Fig. 3(a)]. Fig. 4 shows the operation of the QCA latch. Initially, at t_0, no input or clock is applied and so the latch is in the null state which corresponds to the point "A" on the phase plot. When the input is applied at t_1 (point B), the latch remains in the null state and we do not see any change in the dot potentials. At t_2, the clock is applied (point C) and the latch switches into the state defined by the input. At t_3, the input is removed (point D) and the latch remains locked in the same state. To verify that the latch can preserve its state in the presence of disruptive signals, at t_4 and t_5, we apply signals twice as large as the regular input. But these disruptive signals do not affect the state of the latch, demonstrating that once locked, the latch is immune to any large noise signal or erroneous input as long as the clock is on. Finally, when the clock is removed at t_6, the latch returns to the null state. It should be noted that each latch also acts as an inverter as can be seen from Fig. 4.

IV. QCA Shift Register

A shift register consists of a line of latches where each latch, in its locked state, acts as an input to the next. Binary information is transferred sequentially along the line from one latch to the next by applying a sequence of phase-shifted clock signals to successive latches [5], [6]. The clocking sequence and the resulting dot potentials in the shift register are shown in Fig. 5. At time t_0, all the clock signals are off and both latches are in the null state. The latch L_1 remains in the null state even after the input is applied (at t_1), until the clock signal (V_{C1}) is applied at t_2. L_1 then switches into the state

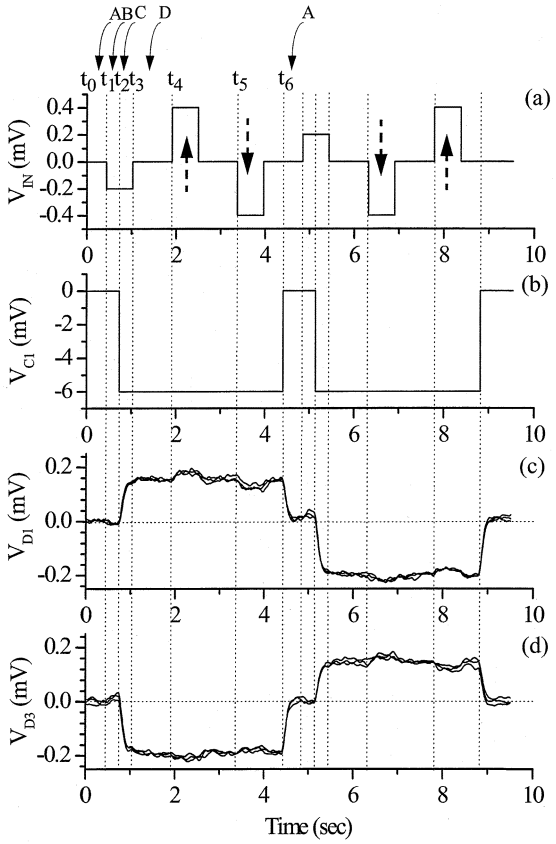


Fig. 4. Operation of a QCA latch. (a) Input applied to D_1 and D_3 (V_{IN} to D_1 and $-V_{IN}$ to D_3). (b) Clock signal V_{C1} applied to the middle dot D_2. (c) Measured dot potential on D_1. (d) Measured dot potential on D_3. Once the latch is in the locked state, disruptive signals (shown by the dotted arrows) twice as large as the original input signal do not affect the state of the latch. Three successive scans are shown in the figure to show the repeatable response.

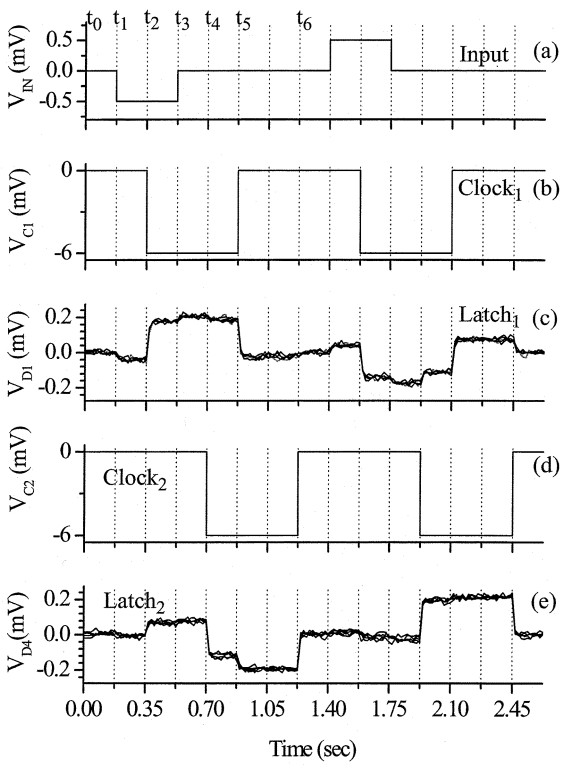


Fig. 5. Operation of a QCA shift register. (a) Input V_{IN} applied to L_1. (b) Clock V_{C1} to latch L_1. (c) Output of L_1 measured by the potential on dot D_1. (d) Phase-shifted clock V_{C2} applied to latch L_2. (e) Output of L_2 measured by the potential on dot D_4.

defined by the input. While L_1 switches, the downstream latch (L_2) is kept in the null state, so that it does not contribute any "back-influence." Once L_1 switches, the input is removed (at t_3), but the latch remains locked in the same state. Then (at t_4) the second clock signal (V_{C2}) is applied to L_2. This copies the information from the first latch to the second. Then (at t_5) the first latch L_1 is switched off and the information is stored in L_2. When the clock V_{C2} is removed at t_6, L_2 switches back to its null state and the system comes back to its initial state. In the second half of the experiment, the same process is repeated for the opposite input. In a multi-stage shift register with more latches, this process can be continued and the bit can be moved along the circuit from one latch to the next by applying such phase-shifted clock signals.

The two-stage shift register can be used to simulate the propagation of a single bit through a multi-stage shift register by moving the bit back and forth from one latch to the other instead of moving it through multiple stages. Fig. 6 shows the timing diagram of the experiment performed for five cycles. Initially, all the signals are zero and the two latches are in the neutral state. Once the input and clock signals are applied to L_1, it switches. The input is then removed and the bit is stored in L_1. The clock signal is then applied to L_2, and it switches using L_1 as its input. L_1 is then switched off, and the bit is now stored in L_2. Instead of applying the clock signal to a third latch in the line, it is applied to L_1 which sees L_2 as an input and switches accordingly. Then L_2 is switched off and the bit is once again stored in L_1. This cycle is repeated five times to simulate a shift register made

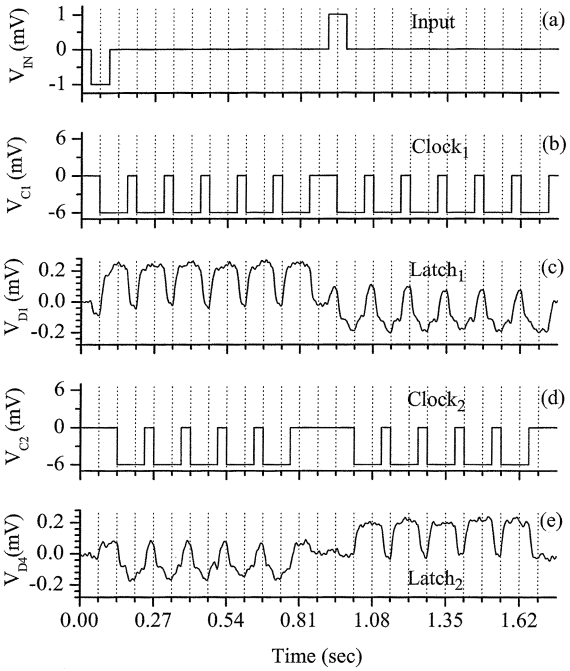


Fig. 6. Simulation of a multistage shift register using a two-stage shift register. A bit is written into latch L_1 by V_{IN} and then by using one latch as input to the other, the bit is copied back and forth to simulate multiple stages. (a) Input applied to L_1. (b) Clock applied to L_1. (c) Output of L_1 measured by the potential on dot D_1. (d) Phase-shifted clock V_{C2} applied to latch L_2. (e) Output of L_2 measured by the potential on dot D_4.

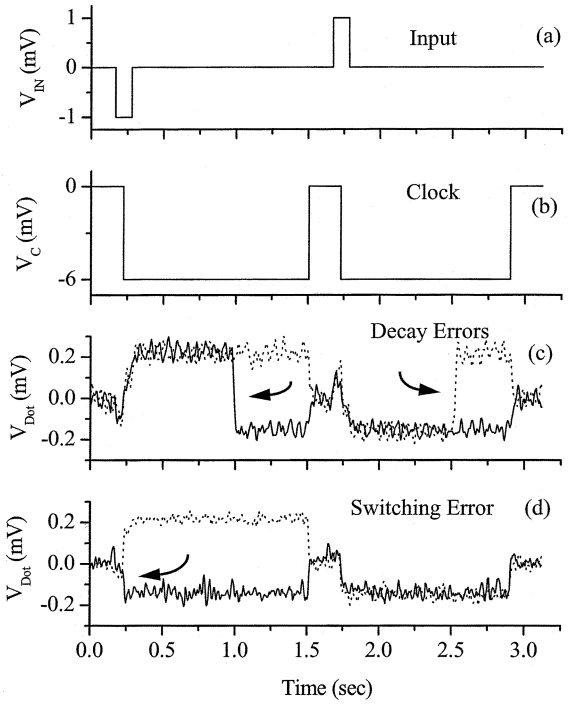


Fig. 7. Errors in the operation of a QCA latch. (a) Input. (b) Clock. (c) Two examples of decay errors (shown by arrows) where information is lost during the clock cycle. (d) Example of a switching error where the latch switches into the wrong state when the clock is applied.

of 11 latches. The above experiment demonstrates that the direction in which a bit moves in the circuit can be controlled entirely by the sequence of clock signals applied to latches. Although the input is applied only once at the beginning of the cycle, we do not see any degradation in the voltage levels as the bit is moved back and forth between the latches, indicating that signal levels would be preserved in multi-stage QCA shift registers. This is expected since clocked QCA devices are capable of power gain and logic level restoration [12], [13].

V. Errors in a Shift Register

While the shift register operates as expected, we do see errors in its operation. Identification of the types of errors and their properties is necessary to estimate and improve the robustness of QCA circuits. Errors encountered in the operation of a QCA shift register can be classified into four types namely "static" or "decay" errors, and "switching" or "thermal" errors, dynamic errors, and errors due to background charge fluctuations. Decay errors occur when the information stored in a latch is lost before the end of a clock cycle. Fig. 7(c) shows two examples of decay errors where the latch switches into the wrong state while the clock is still on. Switching errors occur when the latch switches into the wrong state (opposite to the one suggested by the input signal) when the clock signal is applied. The solid line in Fig. 7(d) shows an example of a switching error. Dynamic errors occur when the switching is performed at speeds higher than the rate of tunneling in the device. Errors due to background charges occur when random fluctuations in charges in the substrate lead to changes in the bias settings of the device.

A. Decay Errors

A decay error occurs when an electron locked in the top dot tunnels out of it into the bottom dot or vice versa when the latch is in its locked state and no external input is being applied to it. Once an electron is locked into the top or the bottom dot and the input is removed, it is equally favorable to be in either dot. However, the electron stays locked since it cannot readily tunnel across the potential barrier set by the middle dot and the multiple tunnel junctions between the top and bottom dots.

We used six tunnel junctions between the top and bottom dots, to reduce co-tunneling and enhance the retention time of the latch to the time scale of our measurement equipment. The characteristic time of the occurrence of such an event at low temperature $(kT < E_c)$ depends strongly on the number of junctions [10]

$$\tau = 2R_jC_j[(N-1)!]^2N^{-2N} \times (2N-1)!\left(\frac{\pi^2R_j}{R_q}\right)^{N-1}\left(\frac{E_c}{eV}\right)^{2N-1}$$

where N is the number of junctions, R_j is the resistance of each junction, R_q is the quantum resistance, C_j is the junction capacitance, E_c is the charging energy of the island, and V is the potential difference between the top and bottom dots.

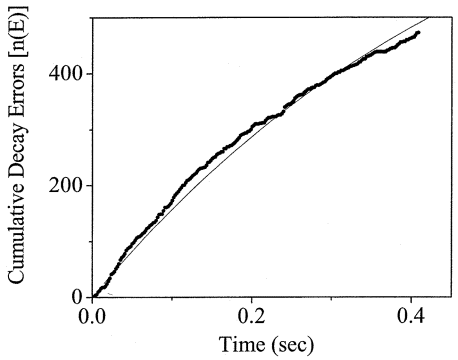
The probability of decay errors follows the equation:

$$P_{DECAY}(t) = n(t)/n_0 = 1 - \exp(-t/\tau)$$

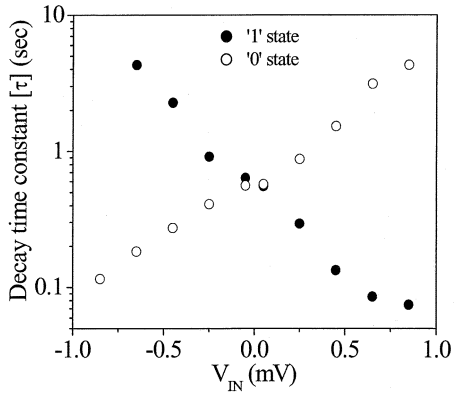
where τ is the retention time constant, $n(t)$ is the total number of decay errors that happened before time t and n_0 is the total number of clock cycles. To measure the retention time constant (τ) of the QCA latch, we repeat the experiment shown in Fig. 7 for 900 clock cycles and determine the time in each case when the latch first decays into the wrong state. The cumulative number of errors as a function of time is shown in Fig. 8(a). By fitting the data to the above equation, the value of τ was found to be 0.52 s.

The time constant measured in Fig. 8(a) corresponds to the lifetime of a bit stored in the latch when the input is removed and there is no preference between either of the binary states [point D in Fig. 3(a)]. Therefore, the lifetimes of both the binary states "0" and "1" would be identical. However, elsewhere in the bistable region there would be a difference in the lifetimes of the two states. To investigate this, we measure the retention lifetimes of the latch at different points along the line PQ in Fig. 3(c). Fig. 8(b) shows the variation of lifetimes measured at different points along the line PQ. In order to measure these lifetimes, we first apply a large input signal to store a "0" or "1" into the latch ("0" being low dot potential on D_1). Then we remove the input, bias the latch at the desired point in the bistable region and measure the time it takes to decay into the opposite state. From the figure we see that the lifetimes of the two states diverge exponentially as we move away from the centre of the bistable region. The lifetime of the ground state becomes much higher than that of the metastable state as we move farther from the centre.

The clock speed of our experiments is limited not by the device but by parasitic RCs in the measurement circuits. Since the



(a)



(b)

Fig. 8. (a) Cumulative decay errors with respect to time, when the experiment in Fig. 7(c) was repeated for 900 clock cycles. By fitting this data to an exponential saturation curve (dashed line), the bit retention time constant for the latch is found to be 0.52 s. (b) Retention time constant in the bistable region of the phase plot, as a function of the input bias setting.

clock rate of our current experiments (1 to 500 Hz) is comparable to the retention time of the latch, decay errors are an important factor in the experiment. However, the device is capable of operating at much higher clock speeds (in the GHz range) and at these speeds, the probability of decay errors becomes negligible. We should also note that the presence of extra junctions will not be necessary for any real application of QCA latches operating at GHz frequencies.

B. Switching Errors

The input applied to a latch creates a preference for one of the two binary states, and the latch switches into the preferred state when the clock is applied. However, in the presence of external noise such as thermal excitation the latch could switch into the wrong state. The probability of such errors would therefore depend on the relative magnitudes of the input signal vs. the noise sources. At a temperature T, the probability for errors due to thermally activated processes is given by

$$P_{SW} = 0.5\exp(-\Delta/kT)$$

where "Δ" is the energy difference between the top and bottom dots caused by the input V_{IN} and is directly proportional to its magnitude ($\Delta = e\alpha V_{IN}$ where "α" is a constant that depends on the voltage distribution between the input and junction capacitances in the latch). The probability of switching errors

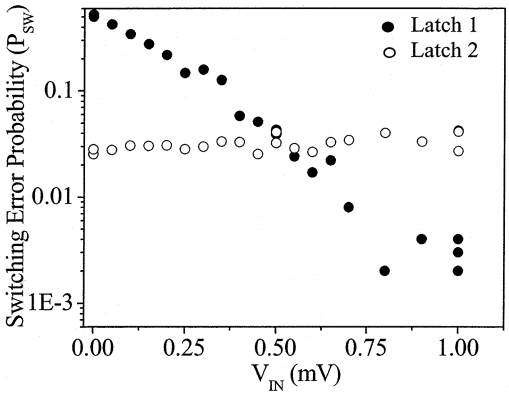


Fig. 9. Variation of the probability of switching errors in a shift register with the magnitude of the input. A bit is written into latch L_1 using the input V_{IN}, and then copied from L_1 to L_2. This process is repeated for 1000 clock cycles at each value of input. The probability of switching errors in L_1 falls exponentially with V_{IN} while it remains constant for L_2 since L_2 uses L_1 as its input.

falls exponentially with the magnitude of input. The presence of other noise sources such as electrical noise or random background charge fluctuations would add additional terms to the denominator of the exponent and raise the effective "noise temperature (T_N)" of the device.

To measure the probability of switching errors at a given input we find the fraction of errors among 1000 switching cycles. Care is taken to ensure that the experiment is not affected by decay errors, by making the time of the experiment much smaller than the retention time of the latch. We see an exponential decrease in switching error probability for L_1 (Fig. 9) with increase in the magnitude of input, as expected. The probability of errors in L_2 remains constant for all values of external input V_{IN} since the input seen by L_2 is the dot potentials on L_1 rather than the external input. We find that the probability of switching errors is higher than that expected from just thermal excitation at the temperature of the experiment. From the data in Fig. 9, and estimating the value of "α" to be 0.08, the effective noise temperature for the experiment is found to be about 330 mK. As devices are shrunk in size, charging energy of the dots would increase and the probability of switching errors reduces dramatically. For example, for a molecular QCA device with charging energy of 1 eV and an operating temperature of 77 K, the expected probability of switching errors is $p_{sw} \sim 10^{-14}$.

C. Dynamic Errors

Dynamic errors are expected to become prominent when the clock frequency approaches the electron tunneling rate across the tunnel barriers. Theoretical estimates [6] predict that the probability of these errors falls exponentially with decrease in switching speeds and faster than exponentially with increase in the magnitude of the input. For devices made from metal tunnel junctions, these errors would not become significant until clock frequencies of about 1 GHz. This value is expected to be much higher for molecular QCA devices where tunneling times are expected to be of the order of femtoseconds. Our current experiments are performed at much lower speeds compared to tunneling times. Therefore we do not encounter these errors in our experiments.

D. Errors Due to Background Charge Fluctuations

Random changes in background charge distribution in the substrate frequently cause errors to occur in the operation of the shift register. These fluctuations typically have a $1/f$ power spectrum. While fluctuations in the frequency range of the clock signal could result in switching errors, there are other random drifts in much larger time scales which cause the potential profile around the device to change, making retuning of the bias point of the device necessary. The time scales of such random bias point drifts in our devices are in the order of tens of minutes to a few hours. While background charge drifts are a continuing problem in metal-based devices, other fabrication techniques have shown some promise in controlling these fluctuations. Recent results on silicon based single electron devices have shown excellent stability over a period of a year [14].

The total probability of digital errors in a QCA latch is the sum of all the errors listed above. In our current devices, decay errors do occur since switching times are close to the retention time of the latches. However, by operating at higher clock frequencies these errors can be minimized. The most dominant form of errors in our devices is the switching errors. The probability of switching errors in latch L_2 is a good indicator of the performance of the shift register, since it gives us an estimate of the relative strength of the input applied by L_1 on L_2 with respect to the noise levels experienced by L_2. This probability is currently at about 4×10^{-2} (Fig. 9) but can be reduced drastically by increasing charging energy of the devices by making them smaller.

VI. Conclusion

We have discussed implementation of clocking in QCA devices and demonstrated the operation of a latch and a shift register. The different types of errors that occur in the operation of a QCA shift register have been identified and their properties have been analyzed. Our results show that by shrinking the size of the devices and operating at high frequencies, the number of errors can be reduced dramatically. The current experiment is the latest in a line of experiments that demonstrate the feasibility of the QCA paradigm. Though the current prototypes operate only in millikelvin temperatures, future devices made from nanostructures or molecules are expected to work at room temperature.

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