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Fanout gate in quantum-dot cellular automata

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Abstract

We present an experimental demonstration of a fanout gate for quantum-dot cellular automata (QCA), where a signal applied to a single input cell is amplified by that cell and sent to two output cells. Each cell is a single-electron latch composed of three metal dots, which are connected in series by tunnel junctions. Binary information is represented by an excess electron localized to one of the two peripheral metal dots of each latch. Fanout is demonstrated by writing a bit to the input latch and then simultaneously transferring the bit to both output latches using two-phase clocking.

S Supplementary data are available from stacks.iop.org/Nano/18/375401

1. Introduction

The modern electronic age is characterized by ever increasing functionality of electronic devices, best exemplified by Moore's law [1]. However, beyond the timeframe of the current International Technology Roadmap for Semiconductors (ITRS) [2], newer information processing paradigms are needed to continue the tremendous improvement in device functionality that has been achieved since the dawn of the IC age. Quantum-dot cellular automata (QCA) [3, 4] is a prominent contender among the possible candidates for future digital nanoelectronics. Absence of continuous current flow in a QCA device results in much reduced power dissipation compared to CMOS, giving this device paradigm a great advantage in the race to scale electronic devices into the quantum realm.

The QCA paradigm includes a clocking mechanism that performs a role similar to that of a power supply in conventional electronics—supplying the power lost in the switching process and thus restoring logic levels. Combined theoretical and experimental studies [5] show that clocking in QCA provides power gain, reduces power dissipation and provides a means for memory features in the cells. Metal quantum dot based implementations of clocked computational schemes were proposed in [6] and various experiments have highlighted the key features of clocked QCA architectures [7–9].

Fanout is a necessary capability for implementing logically significant QCA arrays, as it provides a mechanism for signal splitting, with the power gain in QCA [5] ensuring signal level restoration. In a QCA fanout circuit (figure 1(a)), an input signal is amplified and emitted as two or more output signals, where each output signal has a power gain greater than or equal to 1 with respect to the original input signal. For a signal to propagate through a fanout gate, it is essential for the input cell's charge configuration to dictate the charge configuration of the two output cells. It was shown earlier that a fanout gate implemented in edge-driven architecture has a high probability of entering an incorrect metastable state [10]. Clocking, in the form of cyclical manipulation of inter-dot tunnel barriers, is used to solve the problem of unwanted metastable states [4, 11]. Here we report the experimental realization of a fanout gate implemented in metal-dot QCA.

2. Fabrication

The fanout gate was fabricated using the Dolan bridge technique [12] and consists of three QCA latches capacitively coupled to each other by inter-latch coupling capacitors C_C (figure 1(b)). SEM micrographs of the fabricated fanout gate are available as supplementary data from

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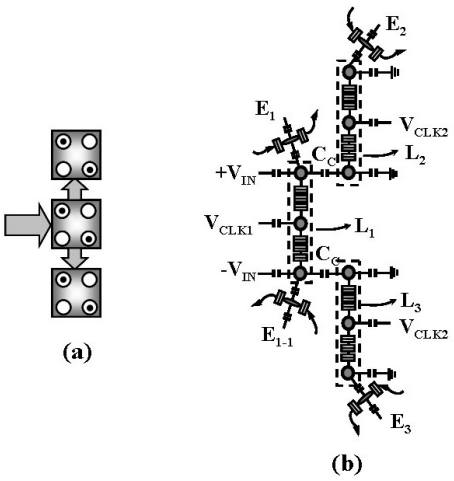

Figure 1. Schematic of a QCA fanout gate: (a) using full QCA cells and (b) a metal-dot based implementation consisting of three QCA latches. Individual latches are delineated with dashed lines.

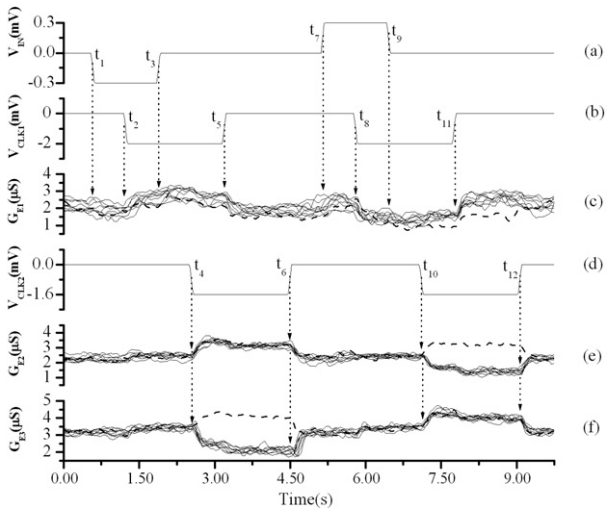

Figure 2. Operation of the clocked QCA fanout gate: (a) differential input signal applied to the first-stage latch (input latch), (b) clock signal CLK1 to the input latch, (c) measured signal showing switching of the input latch as detected by the electrometer E_1, (d) clock signal CLK2 applied to the second-stage (output) latches (note: no external differential input signal is applied to the second-stage latches), (e) measured signal showing switching of the output latch L_2 in the fanout gate as detected by the electrometer E_2, and (f) measured signal showing switching of the output latch L_3 detected by the electrometer E_3. Switching of the latches is detected by monitoring the conductance through the SETs coupled to the respective latches. Note the opposite phase of signals measured by electrometers E_2 and E_3. Multiple curves are shown to illustrate the reproducibility of the measurement. An error trace is shown as a bold dotted line.

stacks.iop.org/Nano/18/375401. Each QCA latch comprises three aluminium metal islands ('dots') connected in series by multiple ($N = 3$) tunnel junctions (MTJs). The typical tunnel junction resistance is ∼500 kΩ and capacitance is ∼300 aF. MTJs are needed to suppress undesired tunnelling processes that lead to errors in latch operation (thermal activation, photon-assisted tunnelling and co-tunnelling) [9, 13, 14]. Single-electron transistors (SETs) coupled to the end dots of each latch are used to detect electron switching in the latch [7]. Each electrometer is biased on the midpoint of the rising slope on its I_{ds}–V_g characteristic to provide a linear response to a change in electron population on the dot coupled to the electrometer. To achieve maximum symmetry in inter-latch coupling and to minimize mutual influence between electrometers coupled to the first-stage latch (labelled E_1 and E_{1-1} in figure 1(b)) and those coupled to the second-stage latches (E_2 and E_3), the electrometers E_2 and E_3 are connected to the opposite end dots in the output latches L_2 and L_3 (figure 1(b)). Therefore if latches L_2 and L_3 are switched to the same polarization (say, an electron is latched in the top dot in L_2 and L_3), the signals in the corresponding electrometers (E_2 and E_3) will be out of phase. For signal detection in the input latch either electrometer (E_1 or E_{1-1}) can be used. Electrometer E_1 is used in the experiment described below. Lock-in amplifiers are used to measure currents through the electrometers biased with an excitation bias of $\leqslant 100$ μV at 3 kHz. The bandwidth of the experimental system (∼5 kHz) limits device characterization at a higher clocking frequency. However, the maximum clocking frequency for QCA devices is much higher (e.g. for molecular QCA it is expected to be in the 100 GHz range [15]). For high-speed characterization of QCA, radio frequency SETs [16] will be used in the future. Measurements are conducted in a dilution refrigerator with a base temperature of 15 mK. A magnetic field of 0.5 T is applied to suppress the superconductivity of aluminium.

3. Measurements and discussion

The aim of the experiment is first to switch and latch *one* electron in L_1 and then to use this latched electron in L_1 as an input to latch *two* electrons (one each) in L_2 and L_3. A single latched electron in L_1 creates a potential difference between the end dots in L_1, which sets the direction of switching of latches L_2 and L_3. Figure 2 shows the operation of the clocked fanout gate as pulsed input (figure 2(a)) and clock signals (figures 2(b) and (d)) are applied to the latches. The operation of the device is accomplished in two clocking cycles and can be divided into two phases for both polarities of the applied input signal, representing binary 0 and 1. In phase no. 1, a negative (positive) input signal is first applied to the input latch L_1 at $t_1(t_7)$, and then on the application of the clock signal CLK1 to the middle dot of latch L_1 at $t_2(t_8)$ it becomes energetically favourable for an electron to switch from the middle dot to the end dot, to which a positive input signal is applied and an electron switching occurs in L_1. (Note that both CLK HIGH signals are negative.) The removal of the input bias applied to L_1 at $t_3(t_9)$ leaves the latch L_1 in the locked state where the switched electron in the end dot is retained as long as the CLK1 is set HIGH, as the negative bias on the middle dot prevents the locked electron from returning to the middle dot.

From the moment when L_1 is locked, it acts as an input to the output latches (L_2 and L_3). In phase no. 2, the clock signal CLK2 is simultaneously applied to L_2 and L_3 at $t_4(t_{10})$ and the Coulomb repulsion caused by the latched electron in L_1 leads to latching of electrons in L_2 and L_3. The polarization of the output state in L_2 and L_3 depends upon the polarization of the input latch L_1. Note that no separate input pulses are applied to input leads of L_2 and L_3 in this process (a small fixed

bias is applied to these leads to compensate for the random background charge effect on these latches [7]). Resetting the clock signal of L_1 at $t_5(t_{11})$ does not affect the electrons switched in L_2 and L_3 as they are now in the locked state. L_2 and L_3 remain in the locked state until CLK2 is removed at $t_6(t_{12})$. Multiple measured experimental traces shown in figures 2(c), (e) and (f) demonstrate fanout gate operation as described above.

However, errors in signal propagation through the fanout gate are also seen, with an example of a measured error trace shown by a dotted line among the electrometer signal traces in figure 2. While the electrometer signal from L_1 indicates correct switching of the electron in the input latch, the electrometer signals E_2 and E_3 demonstrate incorrect switching, with electrons in both L_2 and L_3 preferring one of the end dots of each latch irrespective of the input (polarization state of L_1). Switching error in a fanout device occurs when at least one of the output latches switches into the wrong polarization state, as defined by the input applied by the polarization of the input latch. Thermal excitations are a common source of switching errors in individual latches operating close to the thermal limit where the difference in energy between the two binary states is of the order of k_BT (which is the case for the device described here). If the applied input to a latch does not cause sufficient difference between two possible energy states in the latch (with an electron being trapped on the top or bottom dot), then thermal fluctuations may result in a switching into a 'wrong' state. Switching errors were studied earlier in a shift register composed of two latches symmetrically connected by coupling capacitors [9], with the individual latches having similar device geometry as in the fanout gate described here. It was experimentally observed that the switching error probability in a latch (P_{latch}) depends exponentially on the magnitude of the input signal relative to an effective temperature, which was higher than the temperature of the device. In a fanout gate (as demonstrated here) with one input latch and two output latches (both of which, independently of each other, have a switching error probability, P), the switching error probability of the fanout operation (P_{FO}) is given by

$$P_{\text{FO}} = P_{\text{latch1}} + P_{\text{latch2}} - P_{\text{latch1}} \times P_{\text{latch2}},$$

where P_{latch1} and P_{latch2} give the individual switching error probabilities of the two output latches which depend on the magnitude of the driving signal provided by the input latch. If both output latches are similar by design and the input signal affects the latches equally, then the switching error probabilities of the latches will be similar.

For the demonstrated fanout gate, despite a relatively high error rate due primarily to the asymmetric coupling from the first to the second-stage latches, the error rate is significantly better than random chance. Random switching in *a latch* corresponds to the probability of a certain output occurring when a vanishingly small input is applied. In this case, the error probability is $P_{\text{latch}} = 0.5$, and therefore the error probability for a one input–two outputs fanout gate with random switching of both output latches due to a vanishingly small input is $P_{\text{latch}} + P_{\text{latch}} - P_{\text{latch}} \times P_{\text{latch}} = 0.5 + 0.5 - 0.5 \times 0.5 = 0.75$. The observed switching error probability $P_{\text{FO}} \approx 0.26$–$0.32$ is therefore much better than random switching.

The higher error rate in the fanout device as opposed to the shift register ($P_{\text{SWSR}} \approx 0.02$) [9] is caused by the asymmetric coupling of the input latch (L_1) to the second-stage latches (L_2 and L_3). As mentioned earlier, the input to the second-stage latches is provided by the latched electron in L_1 which changes the potential on both of the end dots of L_1, with a positive change on one end dot and a negative change on the other. In the case of a shift register, the second-stage latch sees as an input the full differential bias between the end dots of the first-stage latch and is not affected, to a first approximation, by a common mode signal caused by V_{CLK1}. However, in the implementation of a fanout gate shown here, the coupling between stages is asymmetrical. In such a case, the change in V_{CLK1} (say negative as in our experiment) will first result in the increase of negative potential on L_1 due to capacitive voltage division. Further increase of negative V_{CLK1} will cause the switching of an electron in L_1, and thus to the redistribution of potentials between the end dots in L_1. The total potential on the end dots of L_1 in the latched state is the sum of the common mode negative signal induced by V_{CLK1} and the voltage generated by the switching electron. As a result, the output voltages on the end dots of L_1 are affected adversely: the negative voltage is enhanced and the positive output voltage is attenuated. To estimate the reduction of the input signal applied to the second-stage latches we calculated the voltages on the dots of L_1 as a function of V_{CLK1}. For each value of V_{CLK1}, the minimum energy charge configuration is calculated subject to the condition that the island charge be an integer multiple of the electron charge. The calculations show that positive output signal is reduced by as much as 80% for the clock swing of -2 mV compared to the case of symmetric coupling. (This value of V_{CLK1} is a result of a compromise: it provides enough bias to securely 'lock' an electron in L1 and at the same time does not completely annihilate the positive output to the second-stage latches.) To overcome the destabilizing effect of the first stage clock, the set-points of the second-stage latches were further adjusted to minimize the switching errors in these latches. After optimization the error rate for each individual second-stage latch is measured to be about 0.2.

Assuming the same inter-latch coupling as in [9], the expected switching error probability in each of the second-stage latches for the adjusted input signal becomes close to $P_{\text{latch}} \sim 0.2$. When two latches with an individual switching error probability of $P_{\text{latch}} = 0.2$ are operated simultaneously as in the fanout gate it results in a net switching error probability of the fanout gate of $P_{\text{latch}} + P_{\text{latch}} - P_{\text{latch}} \times P_{\text{latch}} = 0.2 + 0.2 - 0.2 \times 0.2 = 0.36$, in good correlation with the observed value.

A dramatic reduction in the errors can be achieved by utilizing the symmetrical configuration of a different yet much more complex (to fabricate by the Dolan bridge technique) fanout gate as schematically depicted in figure 3. This design provides for a full differential input bias at the terminals of the output latches, thus exponentially decreasing the error rate [9]. This is possible as this device design implements the input latch (L_1) using a full QCA cell composed of six dots as shown in figure 3. Initially, information from the first half-cell of latch L_1 (the first three dots in figure 3 coupled to the signal inputs $+V_{\text{IN}}$ and $-V_{\text{IN}}$ and the input clock V_{CLK1}) is transferred to the

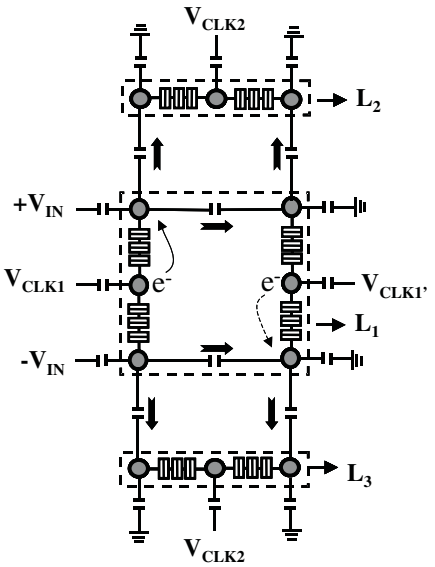

Figure 3. Schematic of an alternative fanout gate implementation using metal tunnel junctions. Latch L_1 is composed of a full QCA cell, for effective coupling of information from the first-stage latch to the second-stage latches (implemented by half-cells). Electrometers coupled to individual latches are not shown for the sake of clarity. Electron switching in the input latch (cell) for a particular input is illustrated to indicate the full differential bias that is applied by the input latch on the output latches.

second half-cell on the application of $V_{\mathrm{CLK1'}}$. Electron transfer in L_1 is indicated for the case of a positive input signal V_{IN} in figure 3. After the information is transferred to the second half-cell of L_1 and the electron latched, the first latch L_1 serves as a full differential input stage for the output latches. Both end dots of each output latch are coupled to the input latch and see the input signal, unlike in the case of the asymmetric coupling fanout gate shown above. This design ensures that effective input signal to the second-stage latches is not reduced as in the asymmetrically coupled case, leading to better error performance as in the shift register [9]. Further reduction of the switching error in clocked QCA logic gates to levels acceptable in modern digital applications ($<10^{-10}$) can be achieved in molecular QCA [17], where the characteristic charging energy is much higher leading to much larger difference (compared to kT) in the energy of individual logic states as opposed to that in metal tunnel junction prototypes.

4. Conclusions

This experiment demonstrates the operation of a clocked fanout gate for QCA architecture and makes an important contribution to the family of the functional prototypes of QCA devices. The fanout gate was fabricated in the Al/AlO_x system and integrates two output latches with an input latch. We demonstrate switching of two electrons in the output latches driven only by one electron in the input latch, made possible by power gain in the output latches. This power gain is seen clearly in the greatly improved signals in the output latches as compared to that in the input latch. In the QCA architecture, the number of output cells driven by a single cell is normally two, a fanout gate. However, since the cells have power gain, they could in principle drive more than two outputs, limited only by the error rate. These extra outputs could be readily added to the existing output latches (to make, for example, a fanout gate with one input driving four outputs).

The current implementation features asymmetric coupling between the input and output latches which leads to higher error rate in the operation of the device. Symmetric coupling between the input and the output latches in a more complex device implementation for the QCA fanout gate is proposed which would lead to a reduced error rate in the device operation. The current implementation is only a proof of concept demonstration in the well known Al/AlO_x system. A future fanout gate probably implemented in silicon nanodevices and/or molecular devices could operate at room temperature and with a much reduced error rate.

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