Reversible and Adiabatic Computing: Energy-Efficiency Maximized

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Abstract. Emerging devices promise energy-efficient computing on a massively parallel scale, but due to the extremely high integration density the previously insignificant dissipation due to information erasure (destruction) becomes a prominent circuit design factor. The amount of heat generated by erasure depends on the degree of logical reversibility of the circuits and successful adiabatic charging. In this paper, we design an adiabatic arithmetic-logic unit to prototype the locally-connected Bennett-clocked circuit design approach. The results indicate one or two orders-of-magnitude energy savings in this physical circuit implementations vs. standard static CMOS. Previous work on computer arithmetic suggests that common hardware implementations erase much more information than would be required by a theoretical minimal mapping of the addition operation. A Bennett-clocked approach can reach the theoretical minimum number of bit erasures in the binary addition, though simulations show that a transistor technology has energy loss due to parasitic components that can exceed the information loss heat. In this paper, we describe the relationship between adiabatic and logically reversible circuits, and predict the potential of the arithmetic implementations based on quantum-dot cellular automata, which enable the full benefits of reversible, locally connected circuits to be realized.

Keywords: Reversibility · Addition · Arithmetic · Adiabatic circuit design

1 Introduction

The computing performance of integrated circuits has been tightly connected to the energy-efficiency of the underlying device technology, and this connection also exists for the emerging circuits [1]. In fact, due to their inherent efficiency in conserving the signal energy, technologies such as quantum-dot cellular automata (QCA) and nanomagnetic logic (NML) will potentially have the dissipation due to physical state compression and irreversibility as the limiting factors for their overall dissipation, which in turn influences the maximum operating frequency or battery life. The combination of molecular circuits and switching frequencies reaching the terahertz regime makes the dissipation associated with the logical and physical irreversibility a

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significant circuit design factor [2, 3]. With QCA, the irreversibility-induced heat dissipation may present surprisingly tight operating frequency limits for computer arithmetic based on high-density nanoscale components. Recent work suggests that binary adders and multipliers might have maximum operating frequency in tens of gigahertz instead of hundreds expected of the pipelined designs, with a typical power density constraint of 100 W/cm^2 [4, 5]. While NML circuits do not reach molecular device densities or gigahertz operating frequencies, their inherent signal energy conservation suggest use in battery-life limited applications, where the energy dissipated due to information loss could make the difference between a battery life of months vs. years.

Computer arithmetic circuits represent highly optimized logic designs usually laid out with extreme care, but the optimization goals have traditionally been the result latency, throughput, circuit area, or CMOS power. Logical reversibility has not been one of the goals, and this has the consequence that the existing or proposed arithmetic circuits are highly sub-optimal from the perspective of information loss. Our recent study suggests that typical QCA adders generate multiple times the number of bit erasures than the theoretical minimum for the addition operation [6], and that QCA multipliers erase a square-law number of bits vs. operand word length, compared to the potential sub-linear loss of the theoretical operation [7]. For an introduction to irreversibility induced density and frequency limits in QCA, the reader is referred to [8].

We believe that logical reversibility is connected to the physical reversibility of the system, that is, the physical, thermodynamically described state of the system has to mirror to some degree the computation that is performed. Fifty years ago, Rolf Landauer proposed this connection in [9], and finally in 2012, the Landauer's Principle was confirmed with a generic one-bit memory experiment [10]. A bit erasure at the room temperature has an inevitable energy cost of at least 3 zJ, which must be dissipated as heat into the environment. To achieve a lower dissipation circuits have to utilize adiabatic charging in forming the logic or clock signals, and achieve a degree of logical reversibility. An erasure-aware, partially reversible circuit involves tradeoffs between performance, timing, circuit area, and power, and must balance the effects of the erasures and adiabatic operation.

This paper explores the tradeoffs in a prototype arithmetic-logic (ALU) unit and is organized as follows: Sect. 2 gives an introduction into adiabatic circuit operation, logical reversibility, and the related heat generation. Section 3 describes our adiabatic transistor circuit, highlighting the challenges and gains of locally connected adiabatic operation. Section 4 describes the simulation setup and Sect. 5 the corresponding results on the power consumption. Section 6 presents predictions for the future technologies, while Sect. 7 the concludes the discussion.

2 Signal Energy Recovery

The energy-efficiency of any integrated circuit technology is closely related to the method of signal representation and the associated signal energy, which must be larger than the thermal noise floor by a significant margin [1]. In standard static CMOS, every switching event leads to the dissipation of all the signal energy stored on the

circuit node. Most of this loss can be avoided by utilizing adiabatic charging principles, which can be fully implemented only by logically reversible circuits. Logically reversible circuits save energy by avoiding the bit erasures and the related heat, but in addition, these circuits have to avoid the other types of loss, like static leakage and dynamic signal energy loss related to the switching mechanism. The operating principle must not lead to the loss of all signal energy during every switching event, like in traditional CMOS. One key property in QCA and NML is the signal energy conservation: the cells settle to the ground state while the signal energy is transmitted from cell to cell. In these technologies, the loss is low and the signal level high [2, 3].

2.1 Adiabatic Charging

Adiabatic charging is one of the pre-requisites of practical reversible circuits. For QCA, this implies that the clock field potentials must be switched at a lower rate than the highest possible rate of the cellular automata. The predicted terahertz devices would have adiabatic switching speeds of tens to hundreds of gigahertz. This is a speed vs. power tradeoff.

The energy dissipation in standard circuits occurs when electrical currents are driven through transistors, with a finite on-resistance, and resistive signal lines. The resistive losses are proportional to the voltage drop, for example between the terminals of a transistor device, which points to an approach of limiting this voltage difference and avoiding abrupt currents as a means to limit dissipation. For example, a static CMOS inverter gate in Fig. 1(a) represents information by the output node voltage, and dissipates all of the signal energy at each switching operation. During a switching event, either the pull-up or pull-down network loses

$$E_{\mathrm{CMOS}} = {}^{1}\!/_{2} C V_{\mathrm{DD}}{}^{2}, \tag{1}$$

where C is the output node capacitance including the wiring and next gate input, and V_{DD} is the operating voltage. This energy is practically all the signal energy.

This circuit can be modified to recover signal energy by utilizing ramped power-clock signals instead of the static operating voltage and ground. An example of such energy-recovering 1n1p-logic, or Split-Level Charge Recovery Logic [11, 12] inverter

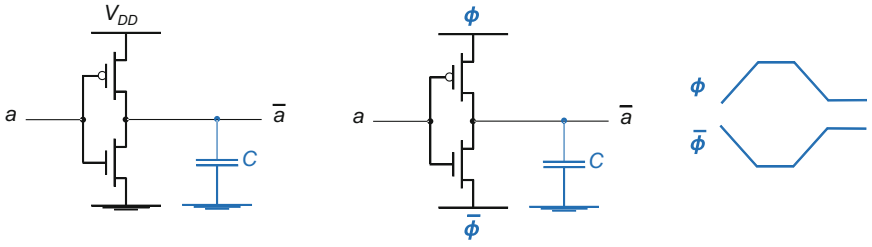

Fig. 1. CMOS inverter. (a) Standard static CMOS implementation, (b) adiabatic 1n1p CMOS implementation, and (c) dual-rail power-clock.

is shown if Fig. 1(b) with the corresponding dual-clock waveforms in Fig. 1(c), which can input energy into the circuit and recover it back. The adiabatic energy loss is

$$E_{\text{adiabatic}} = RC^2{V_{\text{DD}}}^2/t_{\text{ramp}}, \tag{2}$$

where t_{ramp} is the time duration of the ramp. It should be noted that the split-rail signals ensure that the circuit does not lose the typical minimum energy $E_t = {}^1\!/_2 CV_t^2$ associated with the transistor threshold drop V_t, which a single-rail approach would lose. The pipelining of this type of asymptotically adiabatic logic, where there is no lower bound on the dissipation, is challenging due to the need to utilize reversible gates or include garbage signals. For an introduction to adiabatic circuit families and their classification the reader is referred to [13], which describes also quasi-adiabatic approaches enabling simple pipelining but losing some part of the energy. Our design differs from the previous circuits [12, 14–16], since it has no logic overhead for the reversibility, utilizing the Bennett-clocking scheme described in the next section.

2.2 Reversible Logic and Operations

While the circuits presented here are based on adiabatic operation, we believe that maintaining a high degree of energy conservation requires either reversible logic gates or an operating principle that implements logical reversibility. Fully reversible circuits can be constructed using reversible logic gates, like the Toffoli gate [17], but this results in large circuit area and many "garbage" signals needed to retain the state throughout the computation. Another alternative is to utilize Bennett-clocking [18], where the logic structure of the circuit remains unmodified, but the timing is altered to include a compute step and a de-compute step, at the cost of reduced pipelining and throughput. Recovering the signal energy to any desired extent is possible using asymptotically adiabatic logic, where the energy is transferred inside the circuit avoiding any abrupt charging or discharging of the circuit nodes. However, designing such circuits implies that the utilized logic operations have to be reversible in nature.

Logical reversibility is connected to the physical reversibility of the system, that is, the physical, thermodynamically described state of the system has to mirror to some degree the computation that is performed. Fifty years ago, Rolf Landauer proposed this connection in [9] and the Landauer's Principle was confirmed with a generic one-bit memory experiment recently reported in [10]. A bit erasure at the room temperature has an inevitable energy cost of at least 3 zJ, which usually must be dissipated as heat into the environment. This part of the signal energy cannot be adiabatically recovered, unless we incorporate logical reversibility into the circuit.

In traditional circuits the bit erasure energy is insignificant compared to the other losses. For example, the end-of-the-roadmap CMOS will dissipate about three orders of magnitude higher energy per switching event since it loses the full signal energy at each switching event [1]. Losses in the emerging technologies like quantum-dot cellular automata (QCA) [2] vary, but not counting the information loss, the dissipation in all of them is like friction in nature: it can be made as small as desired by switching more slowly, while the energy-per-bit-erasure is unaffected by the speed.

Therefore, it is necessary to design the system to utilize adiabatic charging for the logic or clock signal to recover the energy, in addition to achieving some degree of logical reversibility. From the circuit design perspective, reversible logic and adiabatic operation are desirable, but they incur various costs. An erasure-aware circuit involves tradeoffs between performance, timing, circuit area, and power, balancing the effects of the erasures and adiabatic operation. There are two approaches for logical reversibility.

The first approach is based on using logically reversible gates like the Toffoli or Fredkin gates gate [17]. The truth table of this type of gate contains only one-to-one mappings between the input and output spaces, and therefore the physical trajectory of the evolving computing system can be logically tracked and reversed. In contrast, the truth table of an irreversible operation can be embedded into a larger logically reversible operation by adding "garbage" outputs. This has significant costs in the circuit area and complexity.

The second approach is based on designing the timing of the circuit in such a way that logical information is retained and energy recovery enabled, following the ideas of Bennett [19]. The circuit first computes from the input side to the output side, the result is obtained, and then the circuit de-computes from the output to the input in reverse order. This can be efficiently implemented by the Bennett-clocking technique [18], which is feasible for both adiabatic CMOS circuits and many emerging technologies. Reversibility is achieved by holding the predecessor parts of the circuits steady while successor stages compute, then relaxing after the whole computation has been finished. This is illustrated in the following example utilizing 1n1p asymptotically adiabatic logic style and dual-rail power-clock signals [11].

A simple circuit of two inverters in series and a 2-level concatenated clock is used to illustrate how Bennett-clocking works. Figure 2(a) shows the circuit schematic and the Bennett clocks at each end-terminal, and Fig. 2(b) the timing diagram of the clocks and voltages V_1 and V_{OUT}. For the purpose of illustration, the input is kept high all the time, and the logic swing of $\text{Clock}_{1..2}$ is $0–(+1/2\text{V}_{\text{DD}})$ and the swing of $\text{Clock}_{1..2\_n}$ is $0–(-1/2\text{V}_{\text{DD}})$. The circuit nodes have three stable states: logic "0" $(-1/2\ \text{V}_{\text{DD}})$, logic "1" $(+1/2\ \text{V}_{\text{DD}})$, and relaxed "R" (0 V). Before transitioning, the clocks are held at 0 V, which turns on M_{N1}, but not M_{P1}. Therefore capacitor C_1, the parasitic capacitance at middle node V_1, is discharged until voltage at V_1 becomes 0 V.

1. **Compute V_1**: Input V_{IN} is at stable logic value "1" $(+1/2\ \text{V}_{\text{DD}})$. When the first level clocks start to ramp, the transistor M_{N1} turns on and transistor M_{P1} turns off. Capacitor C_1 gets discharged through M_{N1} gradually. The voltage level at V_1 drops gradually until the clocks become constant.
2. **Compute V_{OUT}**: When the first level clocks stop ramping and become constant, V_1 has stable logic value "0" $(-1/2\ \text{V}_{\text{DD}})$, and the second level clocks start to ramp. Transistor M_{P2} turns on and transistor M_{N2} turns off. Capacitor C_2 gets charged through M_{P2} gradually. The voltage level at V_{OUT} increases gradually until the clocks become constant. Stable logic value "1" is read $(V_{OUT} = +1/2\text{V}_{\text{DD}})$.

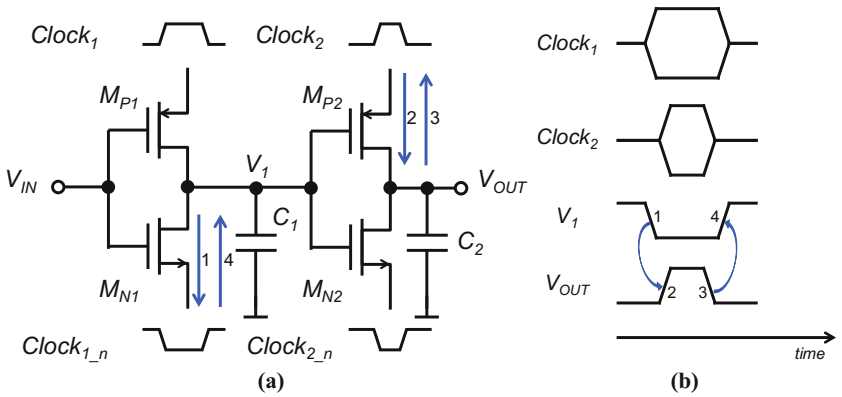

Fig. 2. (a) Schematic of a simple circuit consisting of two inverters connected in series, utilizing 2-level Bennett clock. The blue arrows indicate the current flow during the computation (1 and 2) and de-computation (3 and 4). (b) Timing diagram of the Bennett clocks and the voltages V_1 and V_{OUT}, transitions during the computation (1 and 2) and the de-computation (3 and 4) (Color figure online).

3. **De-compute V_{OUT}**: The second level clocks starts to ramp back to 0 V while the first level clocks are still held constant. Capacitor C_2 gradually gets discharged through M_{P2}, and the voltage level at V_{OUT} gradually drops back to 0 V.
4. **De-compute V_1**: When the second level clocks are relaxed, the first level clocks start to relax back to 0 V. Capacitor C_1 is gradually charged, and the voltage level at V_1 gradually rises back to 0 V. After this, the input V_{IN} is relaxed.

3 Arithmetic-Logic Unit Design

A Bennett-clocked arithmetic logic unit (ALU) was designed based on the commercially available SN74S381N [20], which can perform three arithmetic and three logic operations on two active high unsigned 4-bit words A = (A_3, A_2, A_1, A_0) and B = (B_3, B_2, B_1, B_0), producing the 5-bit result word F = (F_4, F_3, F_2, F_1, F_0). Negative result numbers are represented in the two's complement format. The function mode is set with three additional active high select signals S_2–S_0, to implement an operation from the set {clear/reset, B minus A, A minus B, A plus B, A xor B, A or B, A and B, preset} according to Table 1. The implemented structure is capable of operating either in irreversible standard CMOS mode or the reversible Bennett clocked mode.

3.1 Logical Structure and Implementation

The logic schematic of the ALU using standard gate set {not, nand, nor, xor} is shown in Fig. 3, having the longest combinatorial path of 11 logic levels in the final implementation. In this schematic, no clocks are shown, and only the data signals

Table 1. Functions of the ALU

Control signals			Function mode
S_2	S_1	S_0	
0	0	0	Clear
0	0	1	B minus A
0	1	0	A minus B
0	1	1	A plus B
1	0	0	A xor B
1	0	1	A or B
1	1	0	A and B
1	1	1	Preset

A, B, and F and the select signals S_2–S_0 are included since the structure is inherently combinatorial without any sequential elements.

The design was laid out in 2 μm CMOS to produce the layout in Fig. 4, which was fabricated at the University of Notre Dame. The n-type fabricated transistors have a width/length ratio of 6 μm/2 μm with a threshold voltage of 0.4 V, while the p-type transistors have a ratio of 12 μm/2 μm with a threshold voltage of −1.0 V. The gate oxide thickness is 20 nm, MOSIS Scalable CMOS (Revision 8.00) lambda = 1 μm design rule. To enable Bennett clocking, power to each level of logic is supplied by a separate clock signal. These signals Clk1–Clk11 and Clk1_n–Clk11_n can be configured to run the circuit in either an irreversible or a reversible mode.

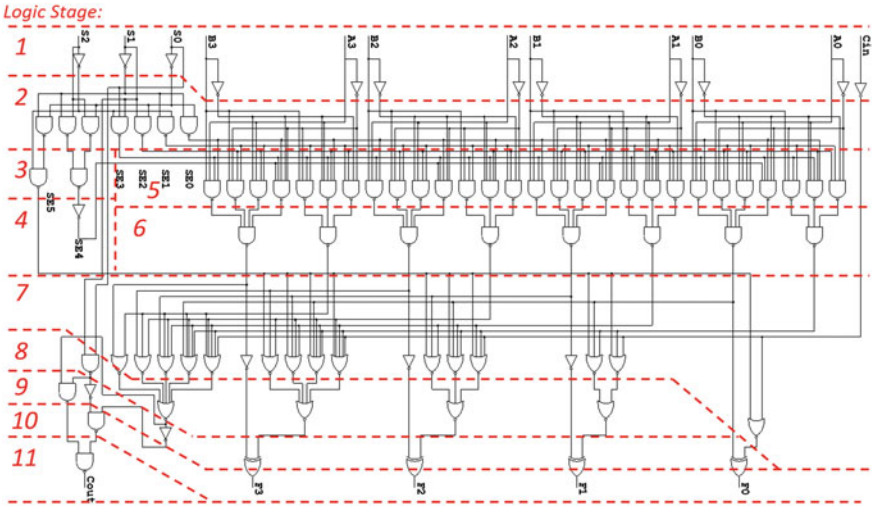

Fig. 3. The logical structure of the ALU, and the 11 stages of Bennett-clocking.

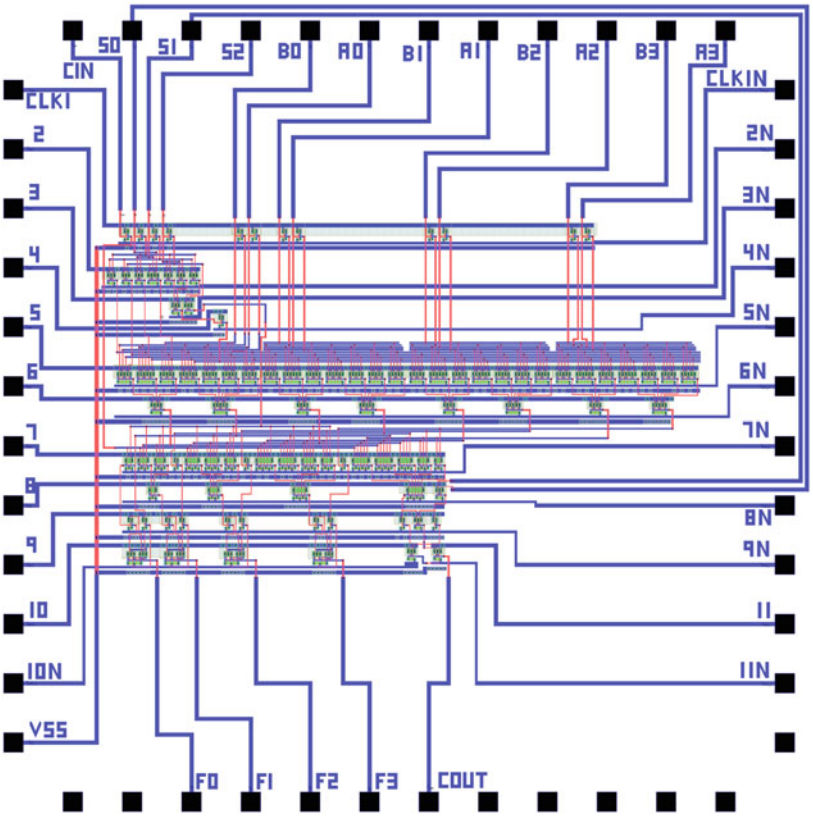

Fig. 4. The layout of the ALU in 2 μm CMOS.

3.2 Irreversible Standard CMOS Operation

The combinatorial ALU unit can be run in irreversible mode like a standard CMOS design by setting the power-clock lines to static values, which are held constant throughout the operation. The positive power-clocks Clk1…Clk11 are tied to the operating voltage V_{DD}, while the negative power-clocks Clk1N…Clk11N are connected to ground GND. In this configuration, the unit implements a standard combinatorial CMOS ALU, without pipelining or any sequential components. This mode of operation erases information and uses energy exactly like traditional irreversible CMOS logic.

3.3 Reversible Bennett-Clocked Adiabatic CMOS Operation

The ALU unit can be configured into fully reversible mode by utilizing the dual-rail power-clock signals with the ramp-up and ramp-down timing defined by the requirements of Bennett-clocking, setting the signals Clk1–Clk11 and Clk1_n–Clk11_n to ramp in concatenation as illustrated in Fig. 5. The design effectively forms

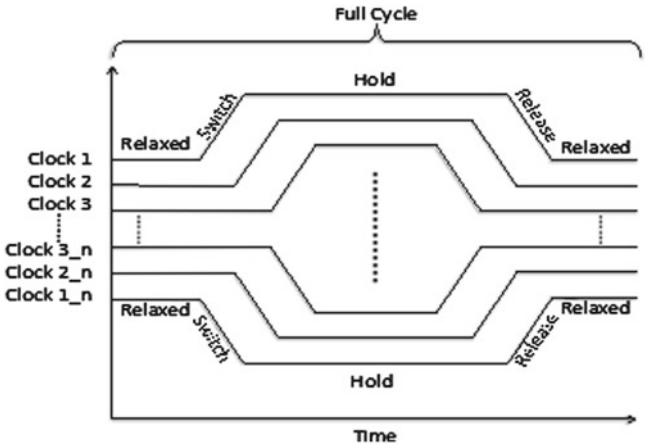

Fig. 5. Reversible Bennett-clocking, the dual-rail power-clock waveforms. The design has 11 positive clocks Clk1–Clk11 and 11 negative Clk1_n–Clk11_n, vertically offset for clarity.

an 11-stage 1n1p-type asymptotically adiabatic logic circuit depicted on logic level in Fig. 3, where the computing part takes 11 steps and de-computing part 11 steps for each arithmetic/logic operation. The design in Figs. 3 and 4 contains all the logic needed for computing and de-computing using the Bennett-clocking scheme, with the only additional overhead the clock generator not shown. By slowing down the frequency, all of the signal energy can be asymptotically recovered, with no additional cost in CMOS logic complexity and area. However, the unit is not capable of pipelining, and the generation of the complicated power-clock signals is challenging.

4 Simulation Setup

The irreversible and reversible ALU were simulated in Synopsys HSPICE 2012, in both the 2 μm and the 20 nm technology. In the **2 μm technology**, the irreversible operation had a static Clk1…Clk11 = V_{DD} = 5 V and Clk1N…Clk11N = GND = 0 V, while the reversible operation had the swing of the Bennett clocks Clk1…Clk11 between 0–2.5 V and the swing of Clk1N…Clk11N between 0–(−2.5) V. A level 3 semi-empirical MOSFET model [21] with parameters extracted from the devices made in the fabrication facility at the University of Notre Dame was used, and a 2 μm gate length was chosen to match the circuits being fabricated. The simulated n-type transistors had a width/length ratio of 6 μm/2 μm and a threshold voltage of 0.5 V, while the p-type transistors had a ratio of 12 μm/2 μm and a threshold voltage of −0.7 V. The gate oxide thickness was 20 nm, and a series resistance of 120 Ω at both the drain and the source was included in the model. The intrinsic transconductance parameter, which is the product of mobility and gate capacitance was KP_{NMOS} = 100 μA/V^2 for NMOS, and KP_{PMOS} = 80 μA/V^2 for PMOS. The velocity saturation was incorporated into the model by setting the parameter VMAX = 210 k for both NMOS and PMOS, and the channel length modulation was excluded by setting the

field correlation factor KAPPA = 0. The effective fast surface state density parameter was NFS = 0.01, in order to turn on the flow of the subthreshold current. The following directives were used for NMOS and PMOS:

```
.model nmos nmos LEVEL=3 KP=100u Vt0=0.5 TOX=20n RS=120 RD=120
+VMAX=210k kappa=0 NFS=0.01
.model pmos pmos LEVEL=3 KP=80u Vt0=-0.7 TOX=20n RS=120 RD=120
+VMAX=210k kappa=0 NFS=0.01
```

In the **20 nm tri-gate technology** simulation, the irreversible operation had a static Clk1…Clk11 = V_{DD} = 0.9 V and Clk1N…Clk11N = GND = 0 V, while the reversible operation had the swing of the Bennett clocks Clk1…Clk11 between 0–0.45 V and the swing of Clk1N…Clk11N between 0–(−0.45) V. A 20 nm LSTP transistor model from Arizona State University Predictive Technology Model library was used [22]. This is a level 72 model based on the BSIM_CMG model for multi-gate devices, and we used the default parameter values in the simulation.

5 Design Analysis

The implemented adiabatic CMOS design can be viewed as a prototype of a reversible, locally connected cellular automata based ALU. The Bennett-clocking approach enables the conservation of signal energy and information in the Landauer/Bennett meaning. This prototype design was simulated in both modes of operation with parameters extracted from the devices made at the University of Notre Dame. The actual 2 μm node chips have been fabricated, but the measurements are ongoing, and therefore we report only the simulation results here.

5.1 Importance of Adiabatic Operation

The adiabatic charging approach can be very beneficial, since it will minimize the resistive heat generated by the circuit. The adiabatic CMOS circuit model simulated with Bennett-type clocking demonstrates that while the logic signal level is very high, the losses in the circuit can be kept very low. Comparison of irreversible standard clocking and reversible Bennett-clocking in a 4-bit ALU at the 2 μm node is shown in Fig. 6. The reversible mode generally offers two orders-of-magnitude improvement in average power consumption in the low frequency end up to 3 MHz, and about an order-of-magnitude improvement up to 50 MHz clock frequency, while the modes are equal around 200 MHz frequency. Including the parasitic capacitances affects both modes of operation. The leakage power can be identified in Fig. 6 as the constant value of power at low frequencies: the irreversible mode has high voltages continuously applied over the transistor drain-source, producing a static level up to 1 mW. The reversible mode avoids most of the leakage, since the voltages are ramped and kept at for much of the clock period, producing a static power around 0.01 mW.

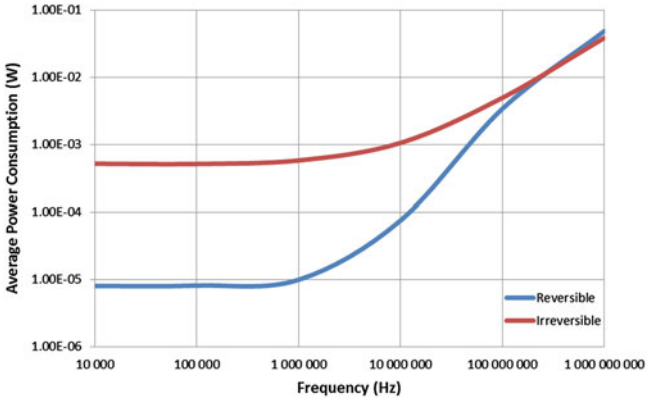

Fig. 6. Simulated average power consumption of the ALU on 2 μm standard CMOS, irreversible vs. reversible mode, as a function of operating frequency.

The comparison of irreversible standard clocking and reversible Bennett-clocking in a 4-bit ALU at the 20 nm node with tri-gate CMOS model is shown in Fig. 7. Although the transistor circuit with reversible/adiabatic operation consumes power approximately with a square-law dependency on the frequency, the approach is still

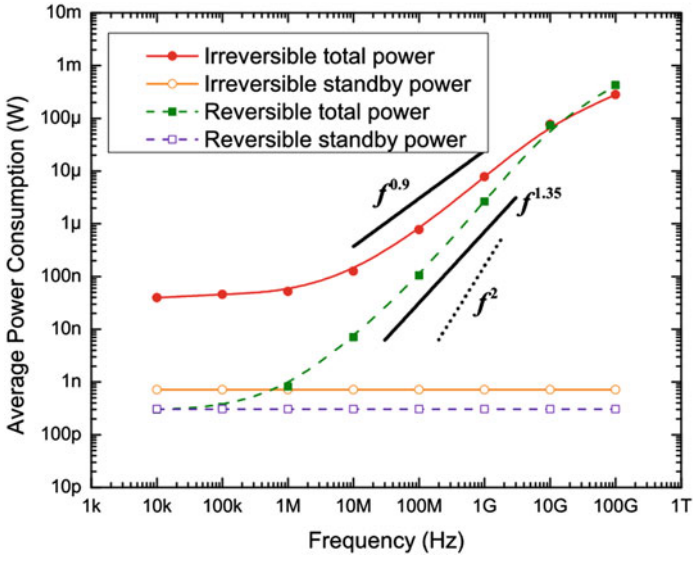

Fig. 7. Simulated average power consumption of the ALU on 20 nm tri-gate CMOS, irreversible vs. reversible mode, as a function of operating frequency

about an order-of-magnitude better at 100 MHz. The leakage/standby power of the irreversible mode reaches 1 nW, and the reversible mode around 0.2 nW.

The cost of the adiabatic approach lies in timing and the complicated clocks, since this design requires eleven clock phases. Adiabatic clocking can recover energy from the logic circuit, but to achieve system-wide energy efficiency the clock generator must be able to recycle the energy. Perhaps the most promising approach for energy recycling is MEMs based resonant clock generators [23]. This is a challenge common to all reversible circuits, including adiabatic CMOS and the QCA.

5.2 Logical Reversibility and Heat Generation

The heat cost of irreversible bit erasures can be approximated and directly related to the logic gates forming the circuit and the timing of the logic operation. We summarize this for the two operating modes of the designed ALU and predict the limits of emerging cellular automata circuits.

Irreversible mode of operation. The irreversible mode has the same information loss as a standard combinatorial static CMOS circuit; for the worst case, an estimate can be based on the worst-case bit erasures of the underlying gates. Assuming the truth tables and per-gate erasures in Table 2, the designed ALU has an upper-bound of logical information loss of

$$N_{\text{not}} \times R_{\text{avg,not}} + N_{\text{nand}} \times R_{\text{avg,nand}} + N_{\text{nor}} \times R_{\text{avg,nor}} + N_{\text{xor}} \times R_{\text{avg,xor}} \approx 85 \text{ bits} \quad (3)$$

per arithmetic/logic operation performed, with N_i the number of each specific gate in the design and $R_{\text{avg},j}$ the weighted average of gate erasures for that gate, with the parameters for each gate type defined in Table 2. The per-gate weighted bound is somewhat pessimistic, since the exact information loss in the logical space depends on the particular operands, as in the various adders modeled in [24]. However, the corresponding worst-case information loss heat of $E_{\text{erasures}} = 85$ bits $\times$ 0.003 aJ/bit $\approx$ 0.250 aJ per arithmetic/logic operation is insignificant, compared to the other losses in the CMOS circuit, the dissipation of the signal energy and static loss. Operating at 1 GHz, the information loss heat power is $P_{\text{erasures}} = (10^9 \text{ Hz} \times 1 \text{ s}) \times 0.250 \text{ aJ} = 250 \text{ pW}$ in the irreversible mode, which is comparable to a quarter of the static leakage power using 20 nm technology.

Reversible mode of operation. The Bennett-clocked mode of operation avoids all the internal bit erasures of the combinatorial ALU structure, leaving only the input operand words A and B to be erased after the de-computing sequence. With the ALU-design, this corresponds to the loss of 8 bits, with $E_{\text{erasures}} = 8$ bits $\times$ 0.003 aJ/bit $\approx$ 0.024 aJ per arithmetic/logic operation, which is an order-of-magnitude better than the irreversible worst-case bound. However, since the Bennett-clocked structure has 11 stages, the heat power at 1 GHz clock frequency is $P_{\text{erasures}} = (10^9 \text{ Hz} \times 1 \text{ s}) \times 0.024 \text{ aJ}/11 = 2.2 \text{ pW}$ in the reversible mode, about 1 % of the static leakage using 20 nm technology. It should be noted, that also the computing throughput is only 1/11 of the throughput of the standard implementation at the same clock frequency.

Table 2. Bit erasures of the standard gate set {not, nand, nor, xor} for each operand combination, and the number N_i of each gate in the design and the weighted average gate erasures $R_{avg,j}$.

Inputs	Output	Information loss
a	*not(a)*	
0	1	$log_2(1) = 0$ *bits*
1	0	
$N_{not} = 18$, $R_{avg,not} = 0$ *bits/gate*		

a	*b*	*nand(a,b)*	
0	0	1	$log_2(3) \approx 1.585$ *bits*
0	1	1	
1	0	1	
1	1	0	$log_2(1) = 0$ *bits*
$N_{nand} = 49$, $R_{avg,nand} = (3 \times 1.585 + 1 \times 0)/4 \approx 1.19$ *bits/gate*			

a	*b*	*nor(a,b)*	
0	0	1	$log_2(1) = 0$ *bits*
0	1	0	$log_2(3) \approx 1.585$ *bits*
1	0	0	
1	1	0	
$N_{nor} = 19$, $R_{avg,nor} = (1 \times 0 + 3 \times 1.585)/4 \approx 1.19$ *bits/gate*			

a	*b*	*xor(a,b)*	
0	0	0	$log_2(2) = 1$ *bit*
0	1	1	
1	0	1	
1	1	0	
$N_{xor} = 4$, $R_{avg,xor} = 1$ *bit/gate*			

6 Predictions for Future Technologies

Reversible logic has great potential in the *Beyond-CMOS* technologies, while quasi-adiabatic CMOS can operate reasonably well with less concern for the information loss [13]. For asymptotically adiabatic circuits in either CMOS like our ALU, or in one of the emerging technologies including QCA [2], logical reversibility is a prerequisite for reaching the full potential of recovering all energy. Our previous work on QCA arithmetic units can be used to predict the operating frequency limits of the studied ALU, if implemented in the emerging extreme low-power technologies [8].

We determined the average logic density of adders and multipliers based on cellular automata, assuming a constant-width square cell as the basic device conceptualized in Fig. 8(a). The cell width w was used as a measurement unit similar to λ

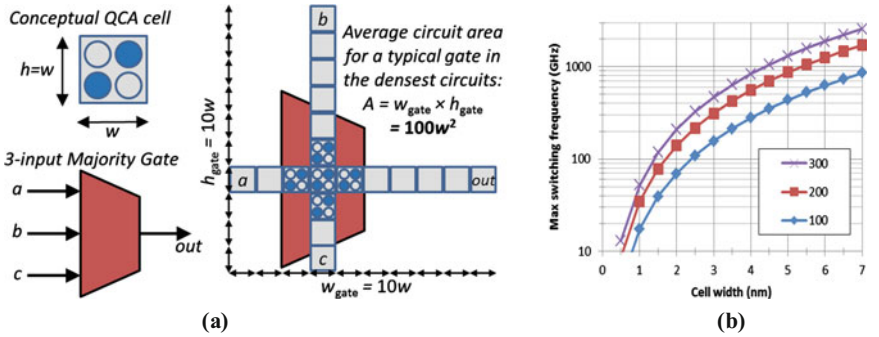

Fig. 8. (a) Definition of logic density in QCA, the average gate area expressed as a multiple of molecular cell footprints. (b) Maximum operating frequency of QCA circuits as a function of cell width, for $A = 300w^2$, $200w^2$, and $100w^2$ dissipation area per majority gate. High-density computer arithmetic designs found in the literature typically use about 200 cell footprints of circuit area per each logic gate (the middle curve) [8].

in standard CMOS layout rules, enabling us to express scalable QCA layout lengths/distances as a multiple of w. Based on the selection of arithmetic units found in literature, we calculated the average area A available for each standard gate, which in QCA is a 3-input Majority Voter Gate (MG) residing in an imaginary layout rectangle of area A, as illustrated in Fig. 8(a). We found that the average area per gate inside the densest core logic (e.g. a full adder) was around $A = 100w^2$, while the wiring overhead of an optimized multi-bit arithmetic unit increased the area per gate typically to $A = 200w^2$. In random logic, the area per gate was typically to $A = 300w^2$ [8].

Figure 8(b) shows the resulting maximum operating frequency vs. QCA cell width w, when the heat generation is limited to 100 W/cm^2. In this comparison, the nominal area per logic gate was considered to be $A = n_{fp}w^2$, where the gate span n_{fp} was 300, 200, or 100 cell footprints, corresponding to the studied relative gate densities.

Table 3. Estimates for the worst-case bit erasures in QCA arithmetic units, vs. operand word length n. The logical operations must perform only a linear number of erasures, but the adders discard 2–6 times that much and the multipliers a square-law amount of information [8].

Binary addition with unsigned n-bit operands *(typically linear)*	
Theoretical addition operation	n
Ripple carry adder, lower bound	$2n$
Ripple carry adder, upper bound	$6n$
Binary multiplication with unsigned n-bit operands *(typically square-law)*	
Theoretical complete multiplication	$n + 1$
Theoretical non-trivial multiplication	$123 \times \log(n + 241) - 673$
Array multiplier	$8n^2$
Serial-parallel multiplier	$16n^2$
Serial-parallel optimized multiplier	$16n^2 - 12n$
Radix-4 recoded multiplier	$26n^2 + 86n - 2$

The typical gate span was $n_{fp} = 200$ footprints and the area $A = 200w^2$ in the studied optimized arithmetic layouts. The results indicate that irreversibility heat is limiting the operating frequency of nanometer-scale molecular QCA cells, while possible sparser implementations will suffer less.

The existing computer arithmetic designs have not been optimized for logical reversibility, which is apparent from the conclusions of our previous study summarized in Table 3. The fundamental baseline information loss for binary addition is n bits, where n is the operand word length of the arithmetic unit. The 4-bit CMOS ALU unit in this paper discards about 85 bits per operation in the irreversible mode, while the known basic adder structures for QCA would have between 8–24 bit erasures per operation. However, the Bennett-clocked reversible CMOS ALU discards only 8 bits, which appears to be the ultimate lower bound even for the future technologies.

7 Conclusion

The adiabatic charging and reversible computing approaches are related to each other, and both will eventually be necessary for the efficient design of future digital circuits in the emerging technologies. In this paper, we considered the relationship between adiabaticity and information loss and designed a configurable CMOS ALU with irreversible and reversible operation modes. The results indicate that even using standard CMOS devices, adiabatic charging and reversible Bennett-clocking together would potentially yield, on average, one or two orders of magnitude improvement in power consumption, compared to the standard static CMOS approach.

The presented adiabatic CMOS design relies on local interaction between the consequent states and we consider it a prototype for future reversible circuits especially based on quantum-dot cellular automata. The existing computer arithmetic structures appear sub-optimal from the perspective of information loss, even though the Bennett-clocked circuit can reach the theoretical lowest bound of loss in the addition operation. The cost in throughput and clocking complexity suggests that a block-reversible scheme should be utilized in larger designs, to seek a compromise between information conservation and the design complexity.

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