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Experimental studies of quantum-dot cellular automata devices

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Abstract

The ultimate nanodevice is the "quantum dot" since that implies confinement in all three dimensions. Heretofore, no Boolean logic scheme has been proposed that is based on coupling of quantum dots. A team of researchers at the University of Notre Dame has devised and demonstrated the fundamental properties of a computing paradigm called "Quantum-dot Cellular Automata (QCA)" QCA could be accomplished in several different material systems, including semiconductor dots, metal dots, nano-magnets, or molecules. In this paper we review a series of experiments demonstrating the fundamental properties of QCA devices implemented in metal dots. Devices include basic cell, majority and other logic gates, latches, and shift registers. The chapter concludes with a discussion of sources of errors in QCA logic circuits.

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1. Introduction

During the last three decades, the microelectronics industry has enjoyed enormous growth in the development and production of digital integrated circuits (ICs). The exponential increase of IC complexity is possible due to the success of the "work-horse" of modern electronics, the field-effect transistor (FET). So far, the performance of FETs has steadily improved in spite of severe size reductions, but as feature sizes encroach upon quantum limits, the ensuing fundamental effects will make further scaling difficult. Deleterious effects such as sub-threshold and gate-leakage currents (to name two) and increasing device density lead to nearly intolerable levels of power dissipation per unit area, which for an Intel® Pentium® 4 chip is comparable to that of a home electric range-top unit, and for the next generation of Pentiums might exceed the heat emission of nuclear fuel [1]. This stems from the fact that despite vast improvements in IC fabrication technology over the last three decades, the role played by FETs has been essentially to mimic a current switch much like the mechanical relays used since the 1930s.

Therefore, the search for an alternative computational paradigm with minimal achievable power dissipation becomes imperative. Naturally, the sought after paradigm must be compatible with the inherent properties of nanostructures as it should exploit the effects that accompany small sizes rather than battling against them.

One such nanostructure-compatible paradigm that proposes a radically new approach to computation is Quantum-dot Cellular Automata (QCA) [2]. QCA uses geometrically arranged arrays of quantum wells (quantum dot cells) to encode and process binary information. Logic levels in QCA are represented by the configurations of single electrons in arrays of coupled quantum-dots. A typical QCA cell consists of four dots located at the vertices of a square (Fig. 1). When a cell is charged with two excess electrons, they occupy diagonal sites due to mutual electrostatic repulsion. The two diagonal electron arrangements ("polarizations") are energetically equivalent ground states of the cell. Lent *et al.* [2] considered several cell designs with cells consisting of four and five dots with different tunneling channels (Fig. 2). They show that either cell design can be used for the realization of QCA with only minor differences in performance.
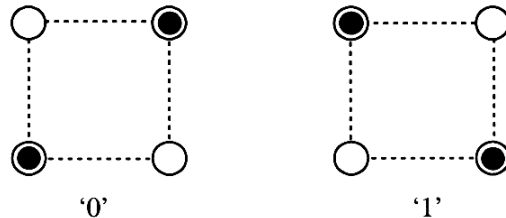
Figure 1. A four dot QCA cell. Two diagonal polarizations represent two possible binary states.

Since binary logic operations in QCA are performed by manipulation of the spatial configurations of single electrons, and do not involve significant current flows, the power dissipation in such a system is greatly reduced compared to conventional, FET-based logic. By changing the barriers between dots slowly compared with the characteristic settling time of the system (i.e. quasi-adiabatically), the energy dissipated in the process can be further reduced and thus the goal of minimal energy dissipation can be achieved [3]. The fabrication of QCA arrays could be accomplished in a number of

ways. While the goal of making the minimal size QCA device working at room temperature could be achieved using molecular implementations, the technology to fabricate molecular QCA (MQCA) arrays is not yet available. However, it is possible to build working prototypes to verify the theoretical predictions using any system exhibiting Coulomb blockade [4] in electron transport between dots forming the cells.
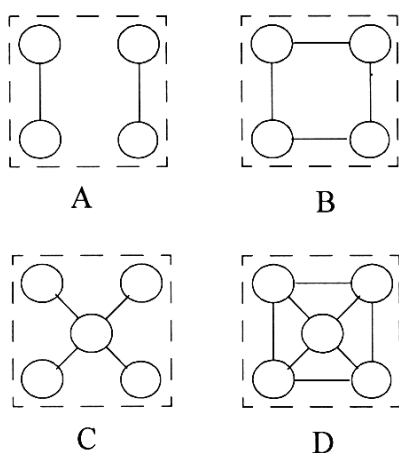
Figure 2. Various designs of QCA cells. Circles represent dots, and lines represent tunneling channels.

Though the original proposal of QCA [2] considered the cells composed of generic quantum dots populated with two electrons, Lent and Tougaw later suggested [5] the use of metal dots separated by aluminum oxide tunnel junctions (TJ) for QCA fabrication. The Fermi sea of electrons in the metal dots is electrically neutralized by the ions of the crystalline lattice. Hence, for the QCA cell to operate, it must be charged with two excess, noncompensated electrons, and the neutral background may be disregarded.

There are several important advantages of the metal TJ QCA system compared with the more-common semiconductor quantum dot technology. First, many uniform tunneling barriers that form the dots can be produced using metal TJ technology. The fabrication process is relatively simple, with only 3 major processing steps: electron beam lithography (EBL), development, and metal deposition through a suspended mask [6] with *in-situ* oxidation. Finally, high yield of the fabricated devices allows the realization of rather complex circuits. In comparison, the fabrication of semiconductor dots requires much more complex processing (typically more than 10 fabrication steps [7]), each tunneling barrier usually requires extra gates to operate, and it is difficult to produce a large number of the quantum dots with similar parameters due to unavoidable influences of impurities and defects. Therefore, we chose aluminum TJ technology for experimental demonstrations of QCA devices.

One disadvantage to the devices produced by the metal TJ process is the smaller charging energy, E_C, of the Al "dots" ($\sim$ 1 meV) compared to the semiconductor quantum dots ($E_C \sim$ 10 meV [6]). This results from the larger barrier (TJ) capacitance, which in turn is defined by the resolution of EBL. To prevent temperature smearing of

charge quantization, the condition $E_C >> k_B T$ (where k_B is Boltzmann's constant and T the absolute temperature) must be satisfied, limiting the operational temperature to below 4K. (Recently, single electron devices fabricated using metal TJ techniques [6] operating at room temperature were reported [8]. However, these devices are single metal dots, weakly coupled to external leads, which prevents effective coupling between the dots neccessary for QCA cells).

It is important to point out that the major advantage of the QCA paradigm compared with conventional FET-based logic is the improvement in performance as the device sizes shrink. As appropriate technologies become available, it should be possible to make complex QCA arrays operating at higher temperatures (>300K) with much better performance in speed (picosecond switching times) and reliability than existing metal TJ prototypes.

2. Fabrication and electrical measurement techniques

Fabrication of Al/AlO$_x$ /Al tunnel junctions is accomplished using standard EBL procedures with double layer resist (PMMA/MMA) and double angle shadow evaporation [5] of Al on Si or Si/SiO$_2$ substrates. The bottom electrode metal, 25 nm thick, is oxidized *in situ* by introducing oxygen into a deposition chamber (for 5 to 15 min at 30-60 mbar) followed by 50 nm of Al to form the top electrode. The resistance of junctions with sizes from 30x30 nm^2 to 60x60 nm^2 varies between 30 kΩ and 2 MΩ at room temperature, depending on the overlap area and oxidation conditions.

Junction resistances should be large enough to fulfull the condition $R_J > R_Q$, where $R_Q = h/e^2$ (*h* is Planck's constant, and *e* is the electron charge) in order to prevent quantum charge fluctuations [4]. At the same time, devices with $R_J > 10$ MΩ have low cut-off frequency ($<10^2$ Hz) due to a large time constant in the measurement circuit and therefore are not suitable for higher frequency applications.

Junction capacitance, C_J, is in the range of 100 to 200 aF. The "dots" of the QCA cells are formed by Al islands with a length of 1-3 μm and width of 50-100 nm. To provide a means for electrical measurements, Ti/Au wires and bonding pads are fabricated on the substrate by optical lithography. To prevent the phenomenon known as "purple plague" at the Au-Al junctions, we use a thin (10 nm) Pt/Ti film between the Al and Au. The samples are then glued into chip carriers and gold wires are bonded to connect the chip carrier to the bonding pads. Measurements are performed in the dilution refrigerator with a base temperature of about 15 mK. To suppress the superconductivity of Al, a magnetic field of 1T is applied to the sample.

Critical to the implementation of QCA is a means of detecting the positions of individual electrons in the output cells. The detector must, therefore, be capable of measuring changes of charge corresponding to the removal or addition of a single electron to the nearby dot. The most natural detection scheme for this application is a single-electron tunneling transistor (SET) [4] situated in close proximity to the dot experiencing the charge change, and coupled to the dot by a non-leaky capacitor. The detailed operation of the SET-electrometer was first presented by Lafarge *et al.* [9]. Two such electrometers coupled to metal dots are shown in Fig. 3.

Conductance of the SET electrometers is measured using standard AC lock-in techniques with an excitation voltage of 5-50 μV. A computerized data acquisition and control system is used to run the experiment. In order to minimize the parasitic coupling

to the system from external noise and coherent interference sources, we use filters in the cryostat wiring, battery powered preamplifiers, and analog opto-isolators. Measurements are performed in the frequency range from 10 Hz to 10 kHz. This allows to reach a temporal resolution of about 0.1 ms.

Capacitances between gates and dots are extracted from measurements of Coulomb blockade oscillation, and are used in theoretical simulations of the device characteristics using orthodox Coulomb blockade theory [4].

The effects of unintentional cross-talk capacitances between the inputs of the cell and electrometers are compensated using feedback circuitry with coefficients defined by the inverse capacitance matrix (see [10] for the details). By this compensation technique, SET electrometers are rendered immune to the input gate signals, and detect only the signals of interest - single electron switching events. In order to determine the coupling capacitance (C_C in Fig. 3) separate SETs are fabricated with gate geometries identical to the coupling capacitor, and used to directly extract its value.
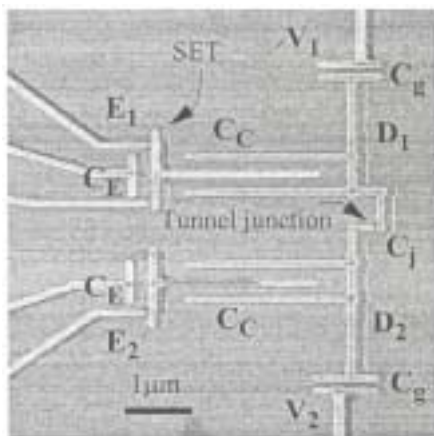
Figure 3. SEM micrograph of the floating double-dot with two SET electrometers. C_J is the junction capacitance, C_g is the double-dot input gate capacitance, C_E is electrometer gate capacitance, and C_C is coupling capacitance between the dot and the electrometer.

3. Experiments with basic QCA devices

In the past several years, a number of key QCA elements were experimentally demonstrated using TJ technology. We start our review with experimental demonstrations of the basic building blocks of QCA architecture: a cell [10-12] and a majority logic gate [13].

3.1 A four-dot QCA cell

Theoretical work on QCA considered several possible implementations of the basic cell (Fig. 2). The simplest configuration, shown in Fig. 2A, consists of two capacitively coupled double-dots, each charged with one electron, which can tunnel within its double-dot. Coulomb repulsion forces electrons to occupy opposite corners of the square (Fig. 1). Here we present the results of the experiments on the QCA cell shown in Fig. 2A. In

the metal TJ implementation of a QCA cell, two islands connected by a tunnel junction form a double-dot (Fig. 3). Here, two isolated metal islands D1 and D2 are connected by a tunnel junction. In this case, single electron transfer occurs in a "floating" system, with no DC connection to the environment. As a result, the total number of electrons on the double-dot is fixed. No electrons can be added to the double-dot from outside, however electrons may be transferred between dots by applying biases to the gate electrodes (V_1, V_2) that are sufficient to over-come the Coulomb blockade for tunneling between the dots. The only transitions possible are those when one dot loses an electron and the other acquires it. Two such double-dots are then coupled using interdigitated capacitors to form a QCA cell (Fig. 4). In early QCA experiments [10-11], the double-dots forming the cell were connected to the source and drain leads by two extra tunnel junctions. This was instructive for initial studies of single-electron tunneling within the cell, but reduces the charging energy of the dots due to extra junction capacitances.
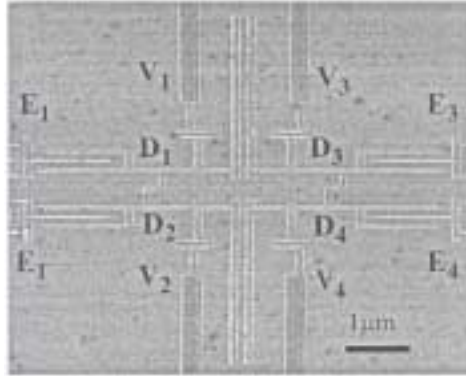

Figure 4. SEM micrograph of the four-dot floating QCA cell with four SET electrometers.

Figure 5 shows a "charging phase diagram" (CPD) - a gray-scale map of the electrostatic potential on the floating double-dot, measured by SET electrometer E1 (Fig. 4). White on the map corresponds to positive voltage on D1, and black corresponds to a negative voltage (the magnitude of this voltage is shown in Fig. 6). The abrupt transition from white to black corresponds to an electron transferred from D2 to D1 as Coulomb blockade is lifted by the input bias. (The respective map measured by E2 coupled to D2 looks inverted compared to Fig. 5.) If a differential input bias is applied to the input gates (in the direction shown by the arrow in Fig. 5), the signals on the detectors have sawtooth shapes [9] with linear change of the potential between the abrupt transitions corresponding to electron transfers from one dot to the other. The average double-dot potential in this case is always zero with respect to ground due to the push-pull nature of the input. If only one of the input voltages (say, V_1) is continuously changing while the other (V_2) is kept at 0, the resulting average potential on the double dot changes as $V_1/2$ (we assume input gate capacitances to be the same). The charge cancellation technique [10] used in the detector circuit, however, removes the monotonic background. This allows the observation of single-electron transitions not only for the "diagonal" direction V1= -V2, but for an arbitrary combination of input biases.
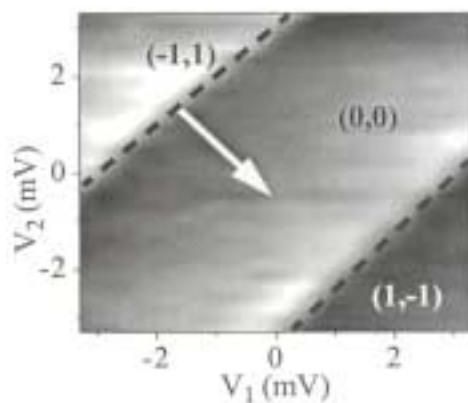
Figure 5. CPD of the floating double-dot measured by E1. Indices in the brackets correspond to the number of excess electrons on D_1 and D_2, respectively. Dashed lines delineate the borders between charge states. The arrow shows the trajectory corresponding to differential bias applied to the gates.
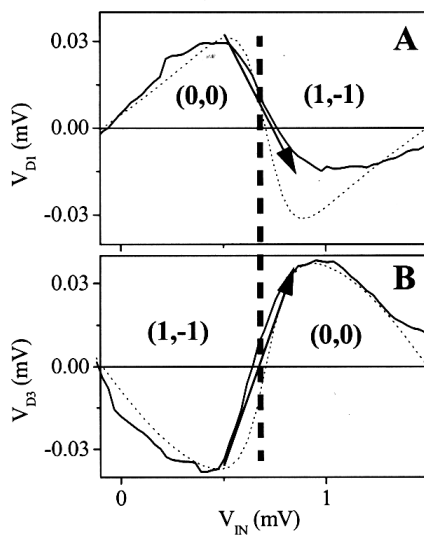
Figure 6. Measured (solid line) and calculated (dotted line) potential of (A) D_1 and (B) D_3, with applied differential bias ($V_{IN} = V_1 = -V_2$). The dashed line marks the position of the border between charge states (see Fig. 5). Note that at the border region the dot potential is close to zero. This corresponds to the electron switching between the dots.

Either floating double-dot could be used as input or output, but for clarity, we will refer to the double-dot on the left as the input double-dot and the double-dot on the right as the output double-dot. In cell switching, an electron transfer in $D_1 D_2$, such as $(0, 0)$ $\rightarrow (1, -1)$, induces an opposite electron switching event in $D_3 D_4$, such as $(0, 0) \rightarrow (-1, 1)$. It is important to point out that since both double-dots are initially neutral, the

application of the initial off-set bias to the input gates is necessary to bring the state of the double-dot to the position of a dashed line in Fig. 5; otherwise electron transfer is prohibited by Coulomb blockade. Since any point on the dashed lines in Fig. 5 could be used for initial biasing, only one common electrode could be used for all cells, provided there is no background charge. The small input bias then drags the state of the input double-dot (Fig. 6A) into one of the two possible charge configurations. As a result, the potential difference produced by the first double-dot D_1 D_2 increases (Fig. 6A), which causes an electron in the second double-dot D_3 D_4 to switch in the opposite direction (Fig. 6B). (The signals shown in Fig. 6 are measured by E_1 and E_3; the signals in E_2 and E_4 are inverted.) The magnitude of the voltage change on the dot at T=0 is $\Delta V = e/C_\Sigma$, where C_Σ is the total capacitance of each dot ($C_\Sigma \sim C_j + C_g + C_C + C_0$, where C_0 is the self-capacitance of the island). Finite temperature smears out the sawtooth resulting in a smaller magnitude of the signal. The theoretical curves shown in Fig. 6 (dotted lines) are calculated for T=70 mK.

Theory results are obtained by minimizing the classical electrostatic energy for the array of islands and voltage leads. The full capacitance matrix is included and the minimum energy charge configuration is calculated subject to the condition that the island charge be an integer multiple of electron charge. Finite temperature effects are obtained by performing the thermodynamic averaging over all nearby charge configurations. A QCA simulation program is used to perform the theoretical calculations here and below.

Thus, the experimental data of Fig. 6 demonstrates QCA operation: a transfer of a single electron in the input half of the cell causes the opposite single-electron transfer in the output half-cell.

3.2 QCA majority logic gate

Binary logic operations in QCA cells are implemented using geometrical arrangements of cells [2]. The fundamental QCA logic device is a three-input majority logic gate (Fig.7), consisting of an arrangement of five standard cells – a central logic cell, three inputs labeled *A, B, C,* and an output cell. The polarization states of inputs *A, B,* and *C* determine that of the logic cell, which is defined by the majority of the three input cells. The output cell polarization follows that of the logic cell. QCA logic gates can be cascaded, so that in a more complex QCA circuit the three inputs would be driven by the outputs of previous gates. Similarly, the output of the majority gate can be connected to drive a subsequent stage of logic gates [2].
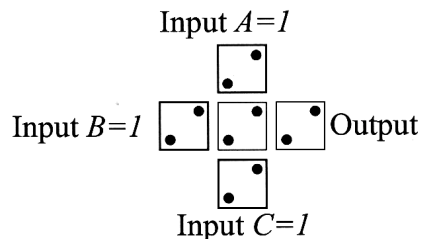
**Figure 7.** QCA Majority logic gate. The cell in the center performs the "voting."

A majority gate can be programmed to act as either an OR gate or an AND gate by fixing one of the three inputs as a program line. If the programming input is a 0 (1), the AND (OR) operation is performed on the remaining two inputs. In experiments, the cell performing the majority gate function consists of four Al dots, $D_1 - D_4$, connected in a ring by tunnel junctions, as shown in Fig. 8 (this corresponds to the cell design of Fig. 2B). In initial biasing of the cell, two excess electrons enter the cell through tunnel junctions, which for simplicity are not shown. Each dot is also coupled to a gate, via capacitance C_g, that influences the charge state of its respective dot.
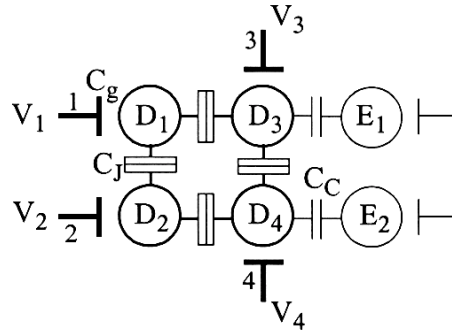
Figure 8. Schematic of the QCA majority gate experiment. The cell is defined by dots $D_1 - D_4$ connected in a ring by tunnel junctions. E_1 and E_2 are the electrometers. External leads and tunnel junctions for the cell and the electrometers are not shown.

To determine the cell polarization, we measure electrostatic potentials on D_3 and D_4 using electrometers E_1 and E_2. First, the logic cell is biased using gates 1 - 4 to the "unpolar-ized" state where logic 1 and 0 are equally probable, and the electrometer outputs are set to 0 V for this condition. This procedure also cancels the effect of the substrate background charge. Figure 9 shows the correspondence between the majority gate test setup (top figure) and its experimental implementation (bottom figure). Differential signals A (between gates 1 and 3), B (between gates 1 and 2), and C (between gates 2 and 4) constitute the inputs to the central cell. The negative (positive) bias on a gate, Φ^- (Φ^+), mimics the presence (absence) of an electron in the input dots as shown by the shaded regions. The amplitudes of Φ^- and Φ^+ are chosen to mimic the potentials due to the polarization of an input cell. Differential signals $A, B,$ and C are converted into logic levels 1 and 0 based on the convention used in Fig. 7. Since D_1 and D_2 are coupled to only one gate electrode each, voltages corresponding to inputs A and B on gate 1, and inputs B and C on gate 2, are added in order to mimic the effect of two input dots. For instance, the input configuration shown in Fig. 9 (i.e. $ABC = 111$) is achieved by setting $V_1 = 2 \Phi^-$, $V2 = 2\Phi^+$, $V_3 = \Phi^+$, and $V_4 = \Phi^-$.

We perform two experiments to demonstrate that our input voltages have the same effect as that of actual electron switching in input cells $A, B,$ and C. First we find the potential swing due to an electron switching from one dot to another. We apply a differential voltage between gates 3 and 4 ($V_3 = -V_4$) to induce electron switching in D_3 D_4. As an electron moves from D_4 to D_3, the potential on D4 undergoes a positive shift due to removal of an electron, while the potential on D3 undergoes a negative shift due
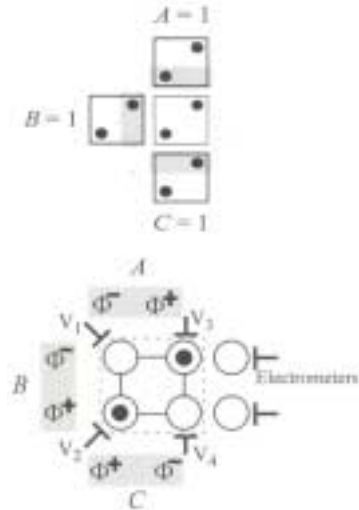
Figure 9. Majority gate experiment - input interfacing. Inputs *A, B,* and *C* (shaded on top figure) are replaced by voltages on the gates (shaded on bottom figure) that are equivalent to polarization states of the input cells.

to addition of an electron. The differential potential swing (Φ_{D4}-Φ_{D3}) for this switching is positive (Fig. 10), with theory closely matching the measured data (the calculated differential potential swing ((Φ_{D1}-Φ_{D2}) is the same when the bias is applied between gates 1 and 2). Next, to demonstrate that the application of "simulated" dot potentials to the gates of the cell mimics an electron switching a neighboring cell, we apply the differential potential extracted in the previous experiment directly to gates 3 and 4 (with the weighting factor C_J/C_g), and measure the differential potentials between D_3 and D_4.
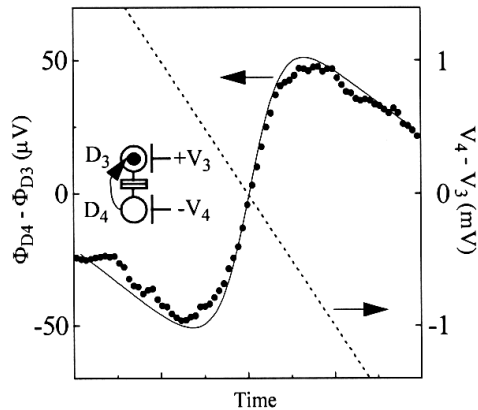
Figure 10. Differential potential change on the dots as an electron switches from D_4 to D_3. The dashed line represents the differential input voltage applied to gates 3 and 4 as a function of time. Solid circles - the measured data, the solid line - theory for 70 mK.

This result is compared to that due to an actual electron switching in nearby dots D_1 D_2. Figure 11 shows the change in differential potential of D_3 D_4 caused by the two mechanisms as a function of time (see the cartoons in Fig. 11), with the data confirming that the response of D_3 D_4 is similar when switched by either the simulated potential or a real electron. These results suggest that using the simulated dot potentials for the inputs in our majority gate experiment are indeed a reliable indicator of how a majority gate would respond when integrated in a QCA circuit. Therefore the input signals applied to the gates in the majority gate demonstration (Fig. 12) have the same amplitudes as that shown in Fig. 11, scaled by C_J/C_g to compensate for differences in capacitance.
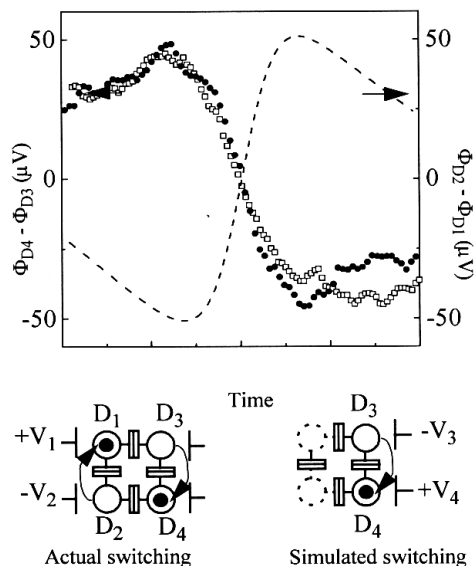
Figure 11. Switching induced in D_3 D_4 by two mechanisms. Solid circles show the measured differential potential change of D_3 D_4 caused by the simulated dot potential, as depicted by inset at right. The dashed line shows the differential potential applied between gates 4 and 3 (scaled by C_J/C_G): $V_3 = (C_J/C_g)\Phi D_1$, and $V_4 = (C_J/C_g)\Phi D_2$. Open squares show the measured differential potential change in D_3 D_4 caused by an electron switching in D_1 D_2, as depicted by the left cartoon.

To perform the majority gate experiment the inputs *A, B,* and *C* are changed as a function of time (Fig. 12 a-c) according to the truth table Table 1, and the differential potential between dots D_4 and D_3, $\Phi_{D4}-\Phi_{D3}$ is measured using the electrometers E_2 and E_1 (Fig. 10). (The transient characteristics are determined by the low cutoff frequency of the data acquisition system, not by the switching time of the cell). The theoretical results are calculated for the electron temperature in the experiment (70 mK). Though no adjustable parameters are used in the theory, the agreement between the experimental and theoretical results is good. The output high (V_{OH}) and output low (V_{OL}) show a clear separation as required for digital logic. The first and last four input steps are grouped separately, with *A* as the programming input, to illustrate AND and OR operations. The AND operation is carried out for *A* = 0, for which we see that the output is high only

when the remaining two inputs are also high. The OR operation is performed when $A = 1$, for which the output is high when either of the other two inputs is high. This data confirms majority gate operation in QCA, and thus demonstrates a logic gate that requires only two electrons to function.
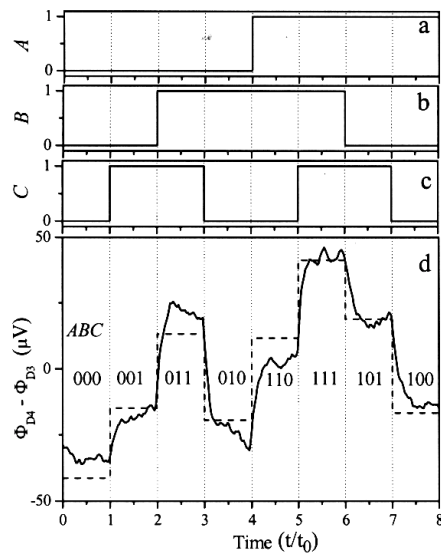
Figure 12. Demonstration of majority gate operation. (a) - (c) Inputs in Gray code. The first and last four inputs illustrate AND and OR operations, respectively. (d) Output characteristic of majority gate where $t_0 = 20$ s is the input switching period. The dashed line shows the theory for 70 mK, solid line represents the measured data.

Table 1. Gray code truth table for the majority gate.

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	1	1
0	1	·0	0
1	1	0	1
1	1	1	1
1	0	1	1
1	0	0	0

To achieve better performance for majority gate operation one would need to improve the separation between V_{OH} and V_{OL}. Thermal smearing of the charge states of the dots results in a less than complete polarization of the cell, leading to only marginal binary level separation. Therefore, the performance of the device could be improved by reducing the total dot capacitance, which will raise the energy of the excited states. For example, when all capacitances are reduced by a factor of 5, the calculated output characteristic shows an increased separation between V_{OH} and V_{OL} (Fig. 13). Therefore, future MQCA logic gates, for which energy separation between the ground and excited states is many orders of magnitude greater compared to metal TJ prototypes, are expected to yield greater separation in the logic levels at much higher operating temperatures.
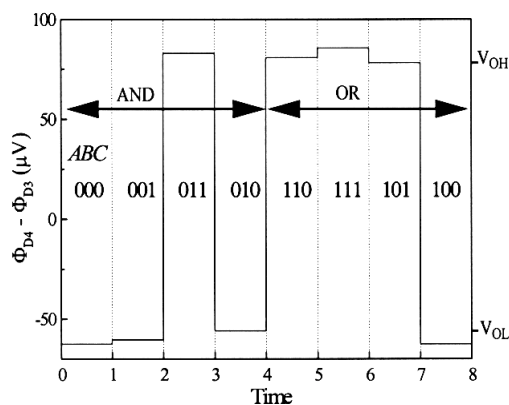
Figure 13. Calculated output characteristic of majority gate when all capacitances are reduced by a factor of 5. Note the improved separation between V_{OH} and V_{OL}.

4. Clocking in QCA

Experiments with QCA cells and majority logic gates [10-13] have demonstrated the basic premise of the QCA paradigm, i.e. coding of information in the position of single electrons. From the early stages of QCA development, however, it was clear that one important issue had to be addressed to allow larger arrays to operate. As the size of a QCA array increases above a certain limit, defined by the energy separation between the ground and first excited state, the QCA paradigm fails to produce a thermodynamic ground state corresponding to the correct calculational result. This is a feature of the so-called edge driven cellular architecture, where the only source of energy driving the entire array into a new ground state is the signal input [3]. It was also pointed out [3,14] that in the case of edge driven arrays, switching of the cells corresponds to a thermally assisted random walk. As a result, for certain intercell coupling parameters it might take an impractically long time for an array to settle to the ground state. Structures such as fan-out attracted some criticism since the energy flow is split, and therefore the propagation of data is more susceptible to defects in the cells [14].

To address this issue, Lent *et al.* [3,15,16] suggested a modified version of QCA where the energy is supplied to each cell by means of clock lines, thus achieving major

improvements in performance. The detailed discussion of the theory of operation and experimental results of clocked QCA are presented below.

4.1 Clocked QCA - Principles of operation

Clocking using cyclical manipulation of quantum wells to perform binary operations was first discussed in detail by Keyes and Landauer [17], who credited the original idea to von Neumann from the 1950's. The idea is to use systems that can be transformed continuously and cyclically from a monostable state into a bistable state and back to monostability (MBM clocking scheme). A particle (*e.g.* an electron) in a time-varying potential in this scheme represents a binary "0" or "1" by the position of the particle (Fig. 14). The clocking sequence is RESTORE-SWITCH-HOLD-RESTORE. At the initial phase, RESTORE, the system is in a monostable ground state. During the SWITCH phase, first the input potential is applied, biasing the cell, and then the system is converted from a monostable to a bistable state by altering the potential profile of the well. This work is done by means of an external energy source - the clock. The particular binary state (corresponding to a particle in the left or right well in Fig.14) is selected by the external input, which creates an asymmetry in the emerging double-well and thus forces the particle to choose either the left or right side. The magnitude of the input signal is small, so that the particle cannot be moved by the input signal alone. By the end of the SWITCH phase, binary information becomes stored in the system. During the HOLD stage the information is preserved, and the particle in the well acts as an input for the subsequent stage (*e.g.*, by means of Coulomb interactions). Finally, the system is returned to its initial, monostable state, RESTORE, and is ready to receive a new input.

|		
E	E	E
x	x	x
Switch	Hold	Restore
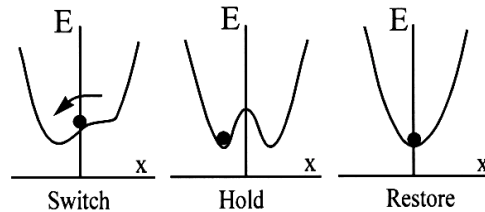
Figure 14. Keyes-Landauer clocking scheme. (E - energy, X- coordinate). Black circle represents particle in the potential profile. Binary 1(0) is defined when particle is confined in the left (right) well.

Using MBM-wells charged with electrons as elementary building blocks, and Coulomb interaction to couple wells, a QCA type architecture could be realized. To implement clocking in QCA, Lent *et al.* [15,16] suggested to electrostatically modulate the barriers between quantum dots within the QCA cell (shown by lines in Fig. 1 and Fig. 2).

As mentioned previously, the use of single electrons in QCA reduces the power dissipation compared with conventional FETs by many orders of magnitude. Moreover, if the potential profile in Fig. 14 changes slowly enough so that the particle remains all the time close to its ground state (quasi-adiabatically), the energy dissipated in the process can be lowered to the well-known Boltzmann's limit of kT ln2 per binary operation (compared to $10^6 kT$ in contemporary FET-based logic [18]).

   Another important advantage of clocked QCA architecture is its inherent ability to realize digital latches. This stems from the fact that the information represented by the position of single electrons within a cell remains stored for as long as the clock signal keeps the barriers high (STORE phase in Fig. 14). As a result, the locked electron provides a firm input signal for the next cell. Latches could be used to break a large QCA array into sub-arrays with each sub-array working on different parts of a computational problem (pipelining). Pipelining in QCA resolves the limitation on the size of non-clocked, edge-driven QCA architecture imposed by thermodynamical considerations. By contrast to the edge-driven QCA architecture where the source of energy driving the whole array is the signal inputs, the primary source of energy in clocked QCA is the clock, which acts as a power supply in conventional electronic circuits. In this manner, clocked QCA exhibits power gain needed for logic level restoration [19].

   The sequence of operations in a clocked QCA cell is shown in Fig. 15. The cell is composed of semiconductor quantum dots where clocking is performed by a common back gate controlling an array of QCA cells [16]. First, prior to the application of new inputs, the cells are brought to a depolarized ("null," RESTORE) mode. In the second ("active," SWITCH) mode, inputs are applied to the QCA array, and the barriers are
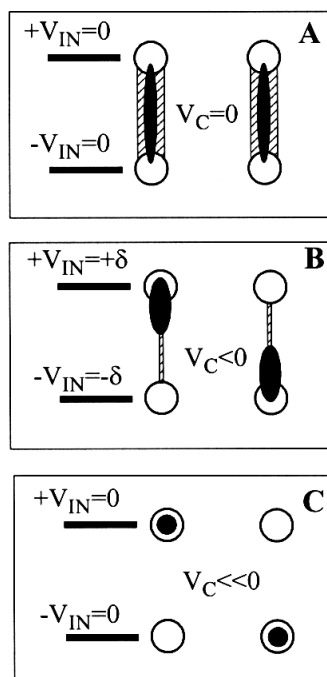

Figure 15. Clocking in a QCA cell. (Cell design from Fig. 2A is used). Lightly shaded area represents tunneling channel. Dark shaded area represents electon density. (A) Null, depolarized mode. Interdot barriers are low, no input is applied. (B) Active mode. Input bias is applied, interdot barriers are slowly rising by changing clock bias. (C) Locked mode. Electrons localized on the dots by clock bias set high. Inputs can now be removed.

slowly raised, moving the system to its new ground state. Finally, the barriers are raised high enough that tunneling between the dots is suppressed, and electrons are confined in the dots ("locked" or HOLD mode). In this mode of operation, the electrons remain trapped on the dots regardless of the state of the input signal.

For QCA arrays implemented in metal islands coupled by capacitors and oxide tunnel junctions, control over barrier heights is much different from that in semiconductor QCAs because oxide barriers cannot be varied by gate potentials. The first implementation of the MBM scheme for the classical Coulomb blockade system with tunnel barriers ("single-electron parametron") was suggested by Likharev *et al.* in [20] and later refined in [21]. A similar design was used by Toth *et al.* [22] for clocked control of the switching in metallic QCA cells, which we now discuss in detail.

In this design (Fig.16), a modulated barrier is replaced with an extra dot, D2, situated between the two end dots, D1 and D3. The system, which we call a QCA half-cell, or QCA latch, is precharged with one electron through a TJ connected to ground. Each dot of the device is capacitively coupled to a corresponding gate, and the differential input signal (which comes from either external leads, V_{IN} in Fig. 16, or an adjacent latch, *e.g.* L1 driving L2 in Fig. 16) is applied to the top and bottom dots. The clocking signal on the middle gate controls the potential on D2, varying the effective Coulomb barrier between D1 and D3. The three operational modes of such a device, null, active, and locked, are defined by the combination of input and clock biases.
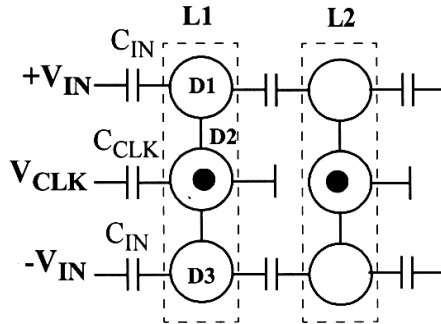
Figure 16. Schematic diagram of a clocked QCA with fixed barriers [22]. The triple dot in the dashed-line box forms a QCA latch. Each latch is pre-charged with one extra electron through the grounded tunnel junction. Two latches form a QCA cell. The null mode is shown.

In the null mode, the input signal is zero and clock bias is such that an electron is localized on D2 (clock LOW). For this combination of gate voltages, the charge state (0,1,0) has the minimal energy configuration. (The numbers in the parentheses are the numbers of excess electrons on D1, D2 and D3 respectively). In the active mode, a small input signal is first applied to the top and bottom gates. The magnitude of the input signal, ΔV_{IN}, is small, so it cannot lift the Coulomb blockade for tunneling from D2 to the end dots. The subsequent variation of the clock signal to HIGH forces an excess electron to switch to D1 or D3, with the direction of the switching defined by the input signal. As a result of switching, the charge distribution between the dots reaches its minimal energy configuration.

In the locked mode, were an electron to be localized in D2, the energy of the configuration would be much higher than for the other two configurations in which it is localized on the end dots. As a result, the electron remains trapped on one of the end dots, regardless of the input signal. The excess electron in the locked mode is in the metastable state when the reverse input bias is applied, or in the ground state when input bias stays the same as in the active mode. In either case, the Coulomb barrier created by the clock HIGH prevents an excess electron from switching.

Finally, as the clock signal is set back to LOW, the Coulomb barrier is removed, the electron switches back to D2, and latch returns to the null state.

To analyze the energy distribution in the QCA half-cell in the switching process we consider the energies supplied to the half-cell by the clock and the input signals:

$$E_{CLK} = C_{CLK} * (V_{CLK} - V_{D2})^2 / 2 \tag{1}$$

$$E_{IN+} = C_{IN} * (V_{IN}^+ - V_{D1})^2 / 2 \tag{2}$$

$$E_{IN-} = C_{IN} * (V_{IN}^- - V_{D3})^2 / 2 \tag{3}$$

It is clear that $E_{CLK} >> E_{IN}$, since $V_{CLK} >> V_{IN}$, $V_{IN} > V_D$, and $C_{CLK} \sim C_{IN}$. Thus, the clock circuit supplies most of the energy needed for the single-electron transitions in the half-cell. The role of the input signal is to only define the direction of the switching. As the clock signal is set back to LOW most of the energy stored in the capacitors goes back to the clock line.

4.2 Experiments with a QCA latch

4.2.1 Single electron charging processes in a QCA half-cell -equilibrium charging diagrams

The basic element of the clocked QCA family fabricated using metal TJ technology, a half-cell, is shown in Fig. 17. It consists of three Al dots, D1-D3 separated by two tunnel junctions. Each dot is also coupled to the SET electrometers E1, E2 and E3. Three leads capacitively coupled to the dots act as signal ($+V_{IN}$, $-V_{IN}$) and clock (V_{CLK}) inputs.

To study the operation of the QCA half-cell, we analyze the single-electron switching processes (measured by SET electrometers) as the functions of input and clock biases and compare it to theory [21, 22]. Calculations of Toth *et al.* [22] were performed for QCA cells pre-charged with one extra electron. Although our device is initially electrically neutral, any change of the initial charge of the cell is, in fact, equivalent to a fixed offset of the biases V_{IN} and V_{CLK}. Therefore, the considerations of [22] can also be applied to the initially neutral half-cell.

In the locked mode an electron must be trapped in one of the end dots so that it is not influenced by changes in the input signal. However, several physical mechanisms could result in the escape of the trapped electron from the metastable state that forms if the input signal is reversed after the application of the clock signal. One possible source triggering this effect is the thermal excitation of an electron over the Coulomb barrier. However, the probability of this process, $p \sim \exp(-E_B/kT)$, becomes small for $E_B >> kT$. Here, $E_B \sim e^2/C_J$ is the height of the Coulomb barrier and C_J is the junction capacitance.
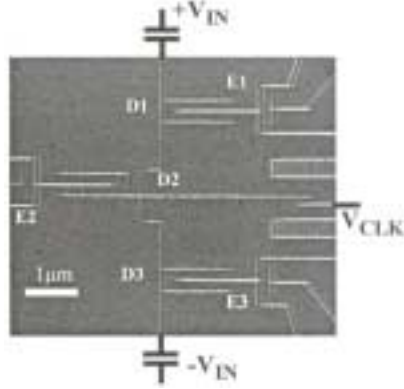
Figure 17. SEM micrograph of a QCA half-cell with two TJs separating three dots with three SET electrometers. Input gates are shown schematically.

For our device $E_B \sim 0.5$ meV, so for T=70 mK $E_B >> kT=6$ µeV, and direct tunneling is suppressed. In that case, the second-order processes (cotunneling) [23] are responsible for the escape of the trapped electrons. The average lifetime of an electron in the metastable state, τ, can be estimated using 0 K approximation [23] for the line of N tunnel junctions biased across with potential difference V:

$$\tau = 2R_j C_j [(N-1)!]^2 N^{-2N} \times (2N-1)! \left(\frac{\pi^2 R_j}{R_q}\right)^{N-1} \left(\frac{E_c}{eV}\right)^{2N-1} \tag{4}$$

For $R_J = 200$ kΩ, $C_J = 0.3$ fF, V = 250 µV, we arrive at an estimate for a retention time, τ. For a latch with two such junctions $\tau \approx 100$ ns, and in the latch with six TJ connected in series, τ exceeds 10^6 s.

Following [22] we first consider the "equilibrium" charging of the QCA half-cell [24]. "Equilibrium" charging is realized when the trapping time of an excess electron in the metastable state (locked mode) is much shorter than the data acquisition time.

In our experimental setup this is the case for a half-cell with two TJs, because the typical data acquisition time, $t_{acq} \approx 10^{-1}$ s $>> \tau \approx 10^{-7}$s. Therefore no trapping can be observed, and the electron distribution on the dots reaches an equilibrium ground state by the time the measurement is completed.

Figure 18 shows an equilibrium CPD measured by electrometer E3. Superimposed with the experimental data are the results of theoretical calculations [22] showing the borders between ground state charge configurations. For the calculations, we use experimentally extracted capacitances with offset background charge as the only adjustable parameter. Due to the random background charge the whole picture is offset with respect to zero, so the point of neutrality, N, is not positioned exactly at zero gate voltages. Numbers of excess electrons shown in the brackets correspond to the local (within the area delineated by hexagons) ground states. Negative numbers mean that electrons are missing from the respective dots. The center of each hexagon corresponds

to a monostable (null) state (Fig. 14C). The inset in Fig. 18 shows the relative electrostatic energies of the three adjacent charge configurations for the ideal case (no random background charge) with no voltages applied to the gates.
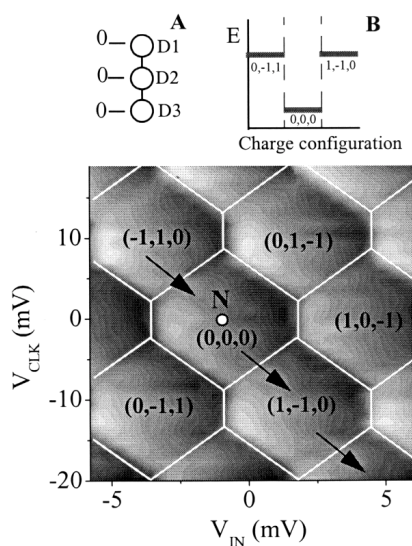
Figure 18. CPD of the half-cell made with two TJ separating the dots, measured by an electrometer attached to D3 in Fig. 16. Differential bias, V_{IN}, is applied as shown in Fig. 17. Numbers in the brackets are the excess electrons on top, middle, and bottom dots respectively. Inset: (A) half-cell with no bias applied (and zero background charge). (B) In this case the lowest electrostatic energy configuration is (0,0,0). Other charge configurations have higher energies [22].

In this case, charge configuration (0,0,0) has the lowest electrostatic energy because of charge neutrality. For classical metal systems with continuous energy spectra CPD is e-periodic, and similar energy considerations are applicable to each hexagon in Fig. 18 (the off-set voltages compensate excess charges on the dots). Note that there are no transitions (resulting in change in brightness) along the directions shown by the arrows. The charge on D3 remains constant along this direction.

(The absence of a monotonic slope along the clock voltage axis in the phase diagram results from a charge cancellation technique used in the experiment. It cancels out the effect of monotonic change of the electrostatic potential on the half-cell and thus allows the observation of only events of interest - the single-electron transitions.)

Now that we have reviewed the general properties of charging in a QCA half-cell, let us now concentrate on a specific region of the CPD to demonstrate clocked control. Figure 19 shows a small region of the CPD measured simultaneously by three electrometers E1-E3 in all three dots of a half-cell. Using the CPD, we will trace single-electron transitions within the half-cell. Here and below we consider clock "HIGH" to be negative, though a positive clock signal could equally be used. In this case, an excess positive charge ("hole") on the end dots is used to manipulate the binary information.

We start at the neutrality point, $V_{CLK} = 0$, $V_{IN} = 0$. (The CPD is offset to place it at $V_{CLK} = V_{IN} = 0$ for clarity.) For $V_{CLK} = 0$, changing the input signal from $V_{IN} = -0.2$ mV to $V_{IN} = 0.2$ mV (path from *a* to *b* in Fig. 19) does not cause a single electron transfer, and the system remains in the same charge state (0,0,0). In the vicinity of this point the charge configuration (0,0,0) has the lowest energy. This is the null mode where a cell remains unpolarized even when the small input signal is applied. A change in the clocking bias towards clock HIGH polarizes the half-cell. For instance, if an input bias is set to $V_{IN} = -0.2$ mV and the clock bias changes from $V_C = 0$ mV to $V_C \approx -6$ mV, then D3 gains an electron, and this electron comes from D2 leaving a "hole" (missing electron) behind (path from *a* to *c* in Fig. 19). Thus a transition (0,0,0) to (0,-1,1) occurs along this trajectory.Note that the number of electrons on D1 does not change, though the potential on that dot becomes more positive. Similarly, by moving from *b* to *d*, a transition from (0,0,0) to (1,-1,0) state is accomplished. The transition from the null into the active mode occurs *at* the dotted line when the clocking signal changes the charge configuration in the half-cell, where the final state is determined by the polarity of V_{IN}.

Further change of the clock signal towards *c* (or towards *d*) brings a half-cell into the locked mode. Here it is energetically unfavorable for an electron to move to D2, so D2 keeps its positive net charge, and an electron stays either on D1 or D3, depending on the polarity of the input bias in active mode. If the polarity of the input signal is reversed, the electron is trapped in a metastable state [21, 22] which has higher energy than a true
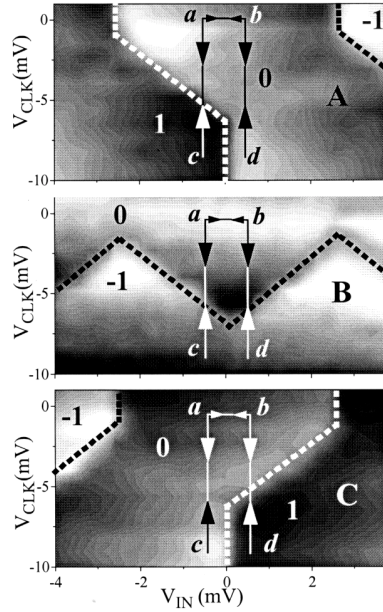

Figure 19. Equilibrium CPD of the clocked QCA half-cell, measured by electrometers E1-E3. (A) D3; (B) D2; (C) D1. Numbers on the graphs represent the number of excess electrons on the respective dots within the areas confined by the dashed lines. Dashed lines on the plots are calculated using the modeling algorithm described in [22] and define the borders between equilibrium ground state charge configurations.

ground state. As discussed above, the trapping time for a half-cell with two TJs, shown in Fig. 19, is much smaller than the acquisition time and the metastable state in the locked mode cannot be observed for the conditions of this experiment.

To summarize, the analysis of CPD in Figs. 18 and 19 confirms the results of theoretical calculations [21, 22] and shows that single electron switching can be accomplished by clock signals with switching direction defined by the input. The CPD in Figs. 18 and 19 correspond to the equilibrium ground state, and do not show any metastability within the experimental time resolution. To demonstrate latching, the lifetime of an electron in the metastable state should be made significantly longer. This can be achieved, for example, using multiple TJs to connect the dots.

### 4.2.2 Single electron charging processes in QCA half-cell with multiple tunnel junctions

The SEM micrograph of a QCA half-cell with multiple tunnel junctions (MTJs) is shown in Fig. 20. It consists of three Al dots D1, D2 and D3 connected in series by MTJs. Each MTJ in turn consists of three tunnel junctions and two small extra islands. To minimize parasitic coupling to these islands from the gates, the area of the islands in MTJs (0.3×0.08 μm^2) is made much smaller than the area of dots D1-D3 (5×0.08 μm^2). To detect the electron transfers in the half-cell, the end dots are coupled to SET electrometers E1 and E2.
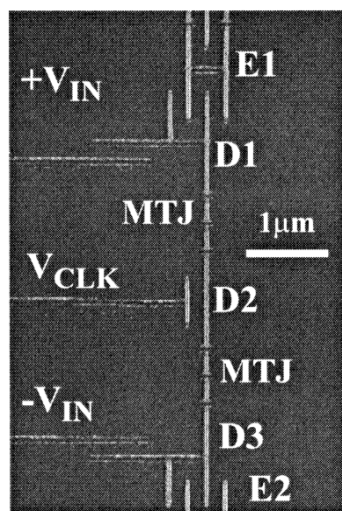
Figure 20. SEM micrograph of a QCA latch fabricated with multiple tunnel junctions (MTJ) separating the dots. Note three junctions and two extra islands in each MTJ.

The addition of extra tunnel junctions effectively suppresses cotunneling, so that the lifetime of an electron in locked mode becomes about four orders of magnitude longer than the data acquisition time. This creates favorable conditions to observe metastability in a locked mode. The resulting CPD depends on the direction of the input voltage sweep, as predicted in [21, 22]. Figure 21 shows a CPD for two scan directions of the

input bias. The areas within the hatched triangles in Fig. 21 correspond to metastable states of electrons in the half-cell. In Fig. 21A the region of metastability expands to the right from the equilibrium border, and in Fig. 21B it expands to the left. This occurs because the Coulomb barrier, *i.e.* the potential on the middle dot, separating the two charge configurations, (0,-1,1) and (1,-1,0), suppresses the switch to the new minimal energy configuration as the equilibrium border is crossed [22]. Note that the point of neutrality is offset from zero by 1.8 mV along the input voltage axis and by -0.5 mV along the clock bias due to the random background charge. *Here and below in the text, the differential input bias δ, and clock signal are considered to be applied relative to this initial offset point.* Figure 22A illustrates the experiment in Fig. 21A. Here, we plot the energy diagrams as the input differential voltage in Fig. 21 changes from negative to positive. Corresponding points α , β , γ are shown in Fig. 21A.
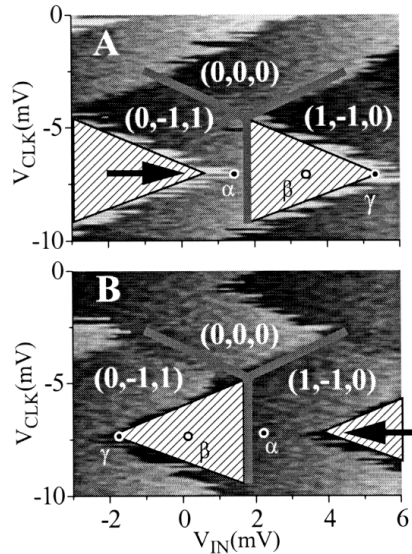

Figure 21. QCA latch charging phase diagram measured by E1. To obtain the plot, the input differential bias is scanned in the direction shown by the arrows. The clock signal is stepped with the increment of 100 μV. Numbers in the brackets are the ground state charge configurations on D1, D2, and D3. Hatched triangles mark the areas of metastability. Equilibrium borders separating the charge configurations in the area of interest are shown as thick lines.

At point α, where the input voltage δ = - 0.3 mV (the equilibrium border is δ = 0), an excess electron on D3 is in the ground state, because (0,-1,1) is the minimal energy configuration. As the input bias increases to point β (δ = + 1.5 mV), the minimal energy configuration changes to (1,-1,0), but the Coulomb barrier prevents the excess electron from switching, so it remains trapped on D3. Finally, at δ = +3.4 mV (point γ), the two electron configurations (0,-1,1) and (0,0,0) become energetically equivalent. As a result, there is no more Coulomb barrier to hold an excess electron, and, with a slight increase in δ, it switches from D3 to D1. At this point, charge configuration (0,-1,1) has changed to (1,-1,0).

Figure 21B illustrates the charging process for the input bias scan in the opposite direction. In this case for the point at δ = +0.3 mV (α),the configuration (1,-1,0) with an electron on D1 has the lowest energy, metastability exists at δ = -1.5 mV (β), and an electron is pushed from D1 to D3 at δ =-3.4 mV (γ). It is clear that only when the combination of voltages on the gates is such that the Coulomb barrier separating the two charge configurations is eliminated, an electron can switch into a true ground state. The electrostatic potentials on D1 and D3 in these regions, therefore, show hysteresis for the forward and reverse scans of the input bias (Fig. 23). The lower (upper) branch of the hysteresis loop corresponds to an electron trapped on D1 (D3).
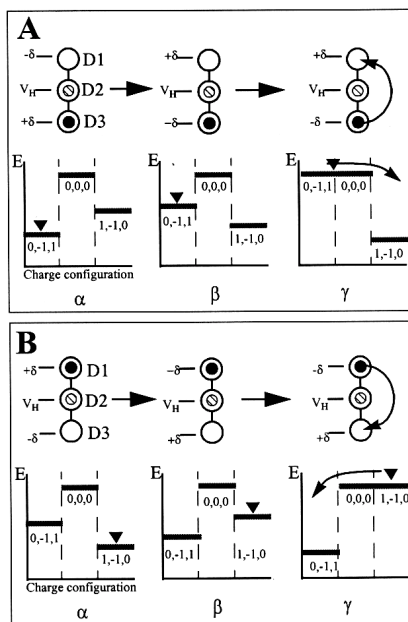

Figure 22. Switching processes in a triple dot for two directions of the input bias scan shown in Fig. 21 with clock voltage set HIGH. E is the electrostatic energy of the configuration, δ is input differential signal. Black circle represents an excess electron, and hatched circle represents a missing electron. Black triangles in the energy diagrams mark the current charge configuration of the system.

To study the influence of the random junction offset charge, CPDs were obtained over a wider range of clock and input biases. Ideally, all of the small islands forming MTJs are in the Coulomb blockade regime independent of the input bias. However, due to the random offset charge on the junctions of the MTJs, the Coulomb blockade conditions within islands of MTJs are affected in a different way for different combinations of gate biases. Figure 24 shows a large-scale CPD measured over several electron periods. It demonstrates that in some areas, the CPD does not show any meta-stability. This is likely due to non-symmetrical offset charge on the junctions of the MTJs so that the tunneling rate from D2 to the end dots differs significantly. Such
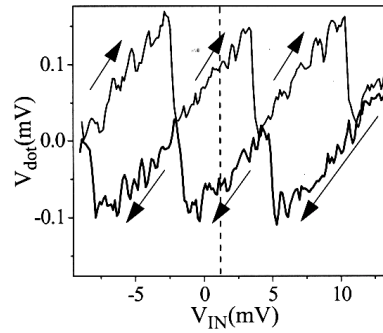
Figure 23. Signal in the detector E1 for two directions of the scan in the bistable region (V_C = -7.5 mV). The dashed vertical line delineates the position of an equilibrium border between charge configurations in Fig. 19. Arrows indicate the scan direction.
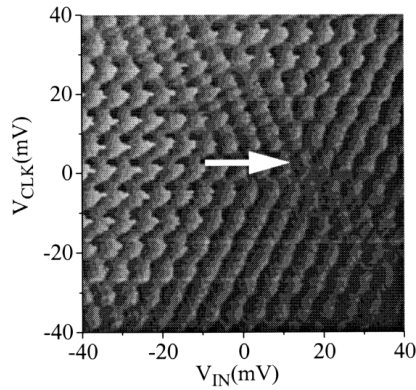

Figure 24. Larger scale CPD measured by E1. Arrow shows the direction of the scan. Triangular shaped areas are metastable regions.

effects, caused by random offset charges on the multiple TJs are commonly observed in single-electron turnstiles and pumps [25] and require extra gates to compensate for random offset charges. The fact that the large-scale CPD changes upon recooling implies that the major effect is caused by random offset charges. Also, the double-dot behavior (as in Fig. 5) of the CPD is due to the fact that the Coulomb blockade is lifted for only one end of the half-cell at a time.

4.2.3 Operation of QCA latch - information storage and processing

To understand the operation of the QCA latch it is instructive to look at the charging events occurring for the changing clock and fixed input voltages, as these are conditions for the latch operation. For this purpose we measure the CPD with the clock signal scanned for different settings of the input differential bias (Fig. 25). Note that this CPD differs dramatically from that in Fig. 21, and resembles that of Fig. 19 in the absence of metastability regions.
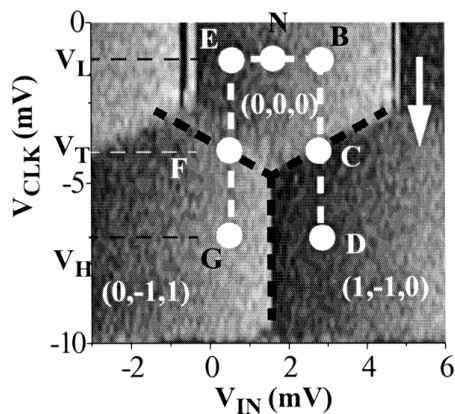
Figure 25. Latch CPD for the clock scans measured by E1. Input differential bias is stepped in 100 µV increments. Scan direction is shown by the arrow. Equilibrium borders between states in the area of interest are shown as dark dashed lines.

As before, the initial (LOW) clock bias is set in the monostable region of the map (point N in Fig. 25). With an input at points E or B, as the clock bias changes, a transition from monostability to bistability takes place, and at the same time a bit represented by a switching electron gets stored in the latch.

Fig. 26A illustrates single-electron transitions occurring along the path B-C-D in Fig. 25. Here, at point "B," $V_{IN}^{+} = -V_{IN}^{-} = +\delta = 0.5$ mV is applied while the clock bias is low, $V_{CLK} = V_L = -1$ mV. (In the ideal case with no background charge, this value is 0 mV). The ground state configuration remains (0,0,0) because the input bias is small and the latch is still in the monostable null state. As the clock voltage changes, at a transitional point "C" ($V_{CLK} = V_T = -4$ mV) the two charge configurations (0,0,0) and (1,-1,0) have the same energy, so the transition (0,0,0) → (1,-1,0) is allowed. From C to D the charge configuration (1,-1,0) is more energetically favorable. Further change of the clock voltage towards $V_{CLK} = V_H = -7.5$ mV leads to energy separation of charge configurations (0,0,0) and (1,-1,0). At point "D" the minimal energy configuration is (1,-1,0), and D1 and D3 are now separated by a Coulomb barrier. The electron is now locked on D1 even if input bias, δ, is set zero, or even reversed, because in order for an electron to switch to D3 the system would go through the charge state (0,0,0) which now has much higher energy. This case is illustrated in Fig. 21B. Note that the latch is most stable when point D is situated along the vertical midpoint of the triangle in Fig. 21B since that represents the condition of largest Coulomb barrier. Further change of the clock voltage will reduce the barrier due to periodicity of the electrostatic energy of the system [21,22].

We may easily visualize the behavior of the CPD for D3 relative to that of D1 as shown in Fig. 25. To do this, merely flip Fig. 25 about the middle vertical axis, i.e. the equilibrium border. The potential on D3 behaves like the path EFG while the potential on D1 follows the path BCD. No abrupt transition on D3 occurs, but rather a monotonic increase in potential is observed. This is because as D1 gains an electron and its potential decreases abruptly, point C, the potential on D2 increases abruptly due to the loss of an electron. Further increases in V_{CLK} through point F do not cause a switch in D3 even

though its potential continues to increase. Therefore, the difference in potentials between D1 and D3 provides the inputs for driving subsequent stages in a line of QCA latches.

Figure 26B illustrates the switching process for inverted input voltage (δ = - 0.5 mV): the respective points E-F-G show how the charge configuration changes from (0,0,0) to (0,-1,1).

Analysis of Figs. 21 and 25 shows that in order for a QCA latch to function, the input signal should be confined within the area of the two hatched triangles containing βs in Figs. 21A and B, while the clock signal should change by the amount corresponding to the vertical size of the hexagons in Fig. 18 to maximize the Coulomb barrier separating D1 and D3. Thus, by analyzing the CPD in Figs. 21 and 25, one can find appropriate magnitudes of the clock and input signals and choose the working point for latch operation.
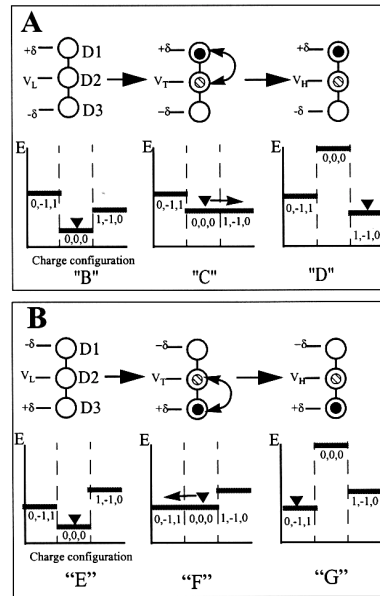

Figure 26. Single-electron transitions in QCA latch operation. (For legends see Fig. 22). Note that δ is not changing throughout this sequence.

Let us now consider the operation of the QCA latch in the time domain for two polarities of the input signal (Fig. 27). At t_1 (t_5) the input signal is applied. In Fig. 25 this corresponds to the deflection from the null point N to the point E(B), resulting only in small variation of the potential in D1, proportional to V_{IN}. As the clock voltage is set HIGH (note that CLK LOW=0, and CLK HIGH=-6 mV) at t_2 (t_6), it pushes an electron from D2 to D3(D1). This results in a large shift of the electrostatic potential on D1(D3). The resulting potential difference between D1 and D3 provides a signal to drive an adjacent latch which is activated by a separate clock line. Once the clock is set HIGH, the input signal can be removed, and the electron remains trapped on D3(D1), until the clock is returned to low at t_4 (t_8). Thus, a cycle describing the operation of a latch based on a QCA half-cell is as follows: null $\rightarrow$active locked $\rightarrow$active $\rightarrow$null.
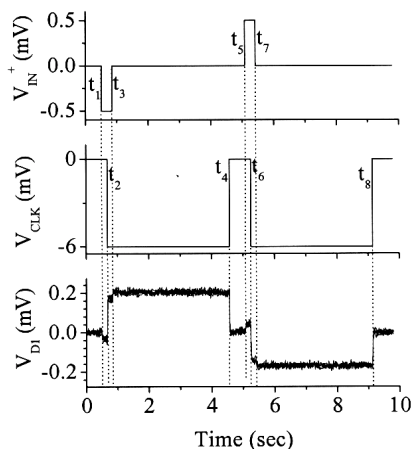
Figure 27. Operation of a QCA latch [26]. A small input signal defines the direction of switching in the latch, while the clock signal triggers the switching. The latch retains the bit as long as the clock is applied. Five successive traces are shown to delineate the noise margins.

Figure 28 demonstrates the ability of the latch to retain the stored electron in the locked phase regardless of the input signal ("error rejection") [26]. Here the input voltage of both polarities with magnitude four times greater than the initial input bias is applied to the input gates after the clock is set high. The electron remains latched regardless of the input signal. (Note that the input signal should stay within the area of hatched triangles in Fig. 21. This defines the maximum disruptive input signal to be rejected by the latch). A small change in the amplitude of the output voltage, which is seen in Fig. 28, is the result of the sawtooth shape of the dot potential (Fig. 23).
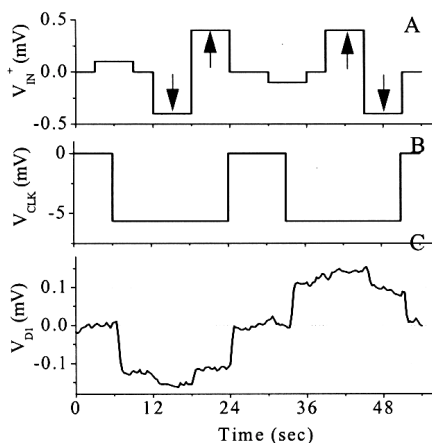
Figure 28. Demonstration of a QCA latch error rejection ability for the two input polarities. Once the latch is set into a locked state, the disruptive input signal, marked by arrows, does not affect the state of the latch.

One of the most important parameters which determine the success of any logic device is the speed of switching for binary operation. The operational speed of the latch is determined primarily by the tunneling time of an electron ($\tau \sim R_J C_J \sim 10^{-10}$ s, where R_J ~ 10^6 Ω, and C_J ~10^{-16} F are the resistance and the capacitance of the junction, respectively). For quasiadiabatic operation the switching speed needs to be reduced by approximately one order of magnitude [16]. Thus, for the current Al/AlOx QCA prototype, the estimate for the switching "speed limit" is on the order of 1 ns. For future molecular implementations due to much smaller total capacitance ($C \sim 10^{-19}$ F) the expected switching speed is on the order of ps.

It is worth noting that the clock speed in our current experiment is set not by the switching speed in the latch, but by parasitic RCs in the electrometer circuits. Since the temporal resolution of the SET readout is limited to about 0.1 ms, any events occurring at a higher rate simply are not detected. To solve this problem a radio frequency SET [27] electrometer will be used in the future experiments.

4.3 Two stage QCA shift register

So far, the operation of a basic element in the clocked QCA architecture, a latch, has been successfully demonstrated [26]. Next, the operation of a coupled system where one latch drives the other by means of single electron switching, and powered by the clock, a shift register (SR), is considered. The simplified circuit diagram of the device is shown in Fig. 29, and an SEM micrograph is shown in Fig. 30. The device consists of two QCA latches (delineated by dashed lines in Fig. 29) and two readout electrometers E1 and E2. The two latches are capacitively coupled to each other using lateral capacitors C_C. Each QCA latch consists of three dots D1-D3, and D4-D6, separated by MTJs. SET electrometers E1 and E2 are used to measure the state of each latch. Operation of the QCA shift register is performed using a two-phase clock (CLK1 and CLK2).

The details of the operation of the two-stage SR in the time domain are shown in Fig. 31 [28]. First, the differential signal V_{IN} corresponding to logical "0" (logical "1") is applied to the inputs V_{IN}^+, and V_{IN}^- at t_1 (t_7) (Fig. 31A). As described above, L1 remains in the monostable null state until CLK1 is set HIGH at t_2 (t_8) (Fig. 31B). When CLK1 is activated, it causes a transition of an electron in L1 (Fig. 31C). After that the signal input
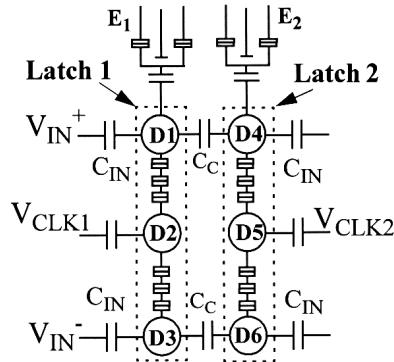

Figure 29. Circuit diagram of a QCA two-stage SR.
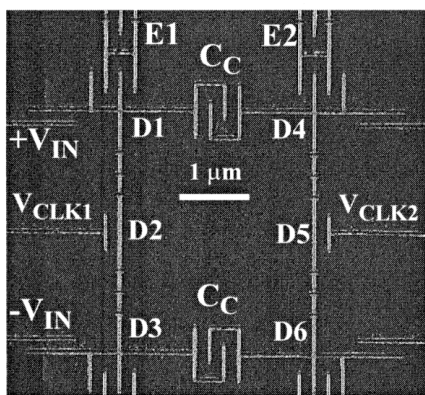
**Figure 30.** SEM micrograph of the two-stage QCA SR.

is removed at t_3 (t_9) and the state of L1 no longer depends on the input signal. Then CLK2 is applied to L2 at t_4 (t_{10}) (Fig. 31D), and an electron in L2 switches in the direction determined by the state of L1 (Fig.31 E). L2 holds the bit after CLK1 is removed at t_5 (t_{11}) for as long as CLK2 is high (until t_6 (t_{12})). The cycle describing the operation of a QCA SR is as fol-lows: monostable $\rightarrow$ input applied $\rightarrow$ CLK1 applied and L1 is active $\rightarrow$ input removed $\rightarrow$ CLK2 applied and L2 is active $\rightarrow$ CLK1 is removed. At this time, L1 becomes inactive and is ready to receive new information. The information encoded in the position of a single electron is shifted to L2 and stored there. The QCA SR operates as predicted in [21, 22].
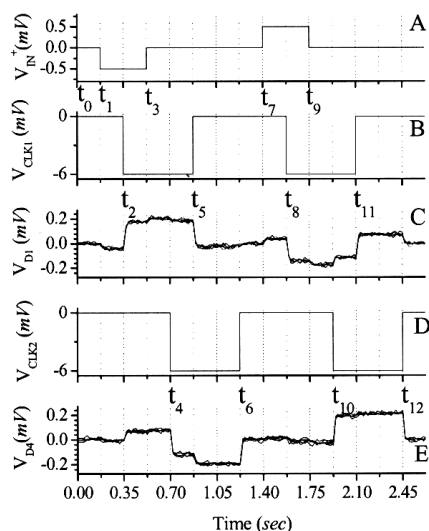
Figure 31. Operation of a QCA shift register. Two phase-shifted clock signals are applied to two capacitively coupled latches to shift binary information from one latch to the next in a sequential manner controlled by the clock. Five successive traces are shown.

## 4.4. Simulation of a multi-stage shift register

The ultimate utility of a SR would be in large-scale QCA circuits to control the flow of binary information through the circuit. Hence, the performance of a multi-stage SR, especially with regard to preservation of logic levels and vulnerability to digital errors, is of considerable interest. The current device can be used to replicate the propagation of a single bit through such an SR. In a multi-stage SR, a bit is first written into the circuit by the input and then moved along the circuit using each latch as an input to the next (Fig. 32A). The same situation can be simulated using the two-stage SR by moving the bit back and forth from one latch to the other (Fig. 32B). Initially, a bit is written into the first latch by the input. Then, using L1 as input, the bit is copied into L2 after which L1 is turned off. Then using L2 as input, the bit is copied back into L1, and L2 is turned off. This process can be repeated a number of times to achieve the same effect as transferring a bit through a long line of latches.
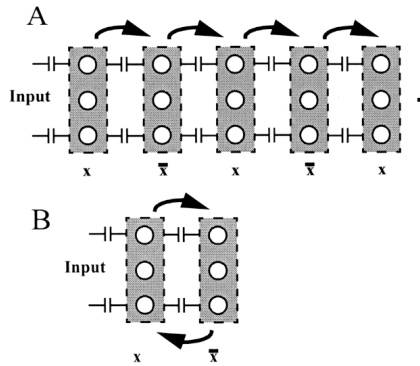
Figure 32. Using a two-stage SR to simulate a multi-stage SR. (A) In a multi-stage SR, a bit is moved sequentially in a single direction from one latch to the next. The bit is inverted at each step. (B) The two-stage SR can be used to simulate a longer SR by moving the bit back and forth from one latch to the other instead of moving it in a single direction.

Figure 33 shows the timing diagram of the experiment performed for 5 cycles [28]. Initially, all the signals are zero and the two latches are in the neutral state. Once the input (binary "1") and clock signals are applied to L1, it switches. The input is then removed and the bit is stored in L1. The clock signal is then applied to L2, and it switches using L1 as its input. L1 is then switched off, and the bit is now stored in L2. Instead of applying the clock signal to a third latch in the line, it is applied to L1 which sees L2 as an input and switches accordingly. Then L2 is switched off and the bit is stored once again in L1. This cycle is repeated 5 times to simulate an SR made of 11 latches. In the second half of the experiment, this scheme is repeated with an input of the opposite sign (binary "0"). This is necessary to verify that bit inversion at the input indeed leads to the bit inversion at the output. The above experiment demonstrates that the direction of the information flow in the circuit is controlled by the sequence of clock signals applied to latches. Another observation that can be made from Fig. 33 is that, although the input is applied only once at the beginning of the cycle, we do not see any degradation in the voltage levels as the bit is moved back and forth between the latches,

indicating that signal levels would be preserved in multi-stage QCA SRs. The major reason for this stems from the ability of clocked QCA to exhibit power gain [19] - the clock signal in QCA provides the energy needed for digital level restoration just as a conventional power supply does it for FET circuits.
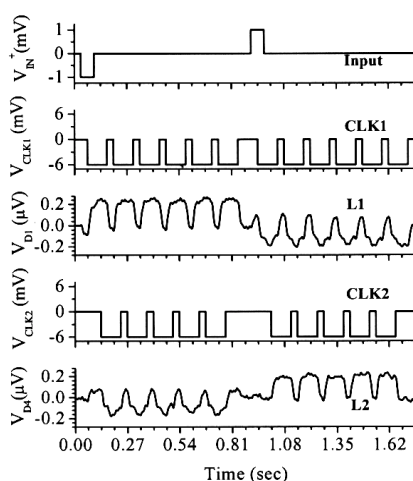
Figure 33. Experiment to simulate a multiple stage SR [28]. The input is applied only at the beginning, to write a bit into the SR. Then the bit is transferred from one latch to the other for five cycles. In the second half of the experiment, the sequence of events is repeated with an input of the reversed polarity. This experiment can be used to investigate the propagation of errors in a multi-stage SR.

4.5 Bit error rate (BER) in clocked QCA

As shown above, the basic elements of the clocked QCA architecture have been successfully built and tested. A number of issues are yet to be addressed regarding the robustness of the proposed paradigm. It is well known, for example, that the reliable operation of any digital device sets the limits on the acceptable BER. What limits the number of error-free switching operations in a QCA SR? How many bit-shifting operations can be performed before a digital error occurs?

We start our analysis with a consideration of errors occurring in the QCA latch and then look at the error propagation in QCA arrays.

Errors in the binary operation of a QCA latch can be divided into three categories:

(a) static, or "decay," errors corresponding to the loss of information during the retention time;
(b) switching errors, occurring during the transition from monostable to bistable state and caused by the finite probability for a system to switch to the energetically unfavorable state;
(c) dynamic errors, which occur when the switching speed is too high compared to the tunneling rate, so that the relaxation to the final state cannot be accomplished.

4.5.1 Static decay errors

An escape of an electron from a locked state results in loss of information. Errors occurring during the retention period of the latch, when an electron is in a metastable state, are defined by its lifetime, τ. As discussed above, the major mechanism causing the static errors in our device is cotunneling, which could be effectively suppressed by using the MTJ design. The estimate for the value of τ using the zero-Kelvin approximation (4) is imprecise since the actual parameters of the MTJ for the floating device could not be measured directly. To measure τ, the experiment of Fig. 27 is repeated N times (N~1000) and then the time interval between the application of the clock signal to the first escape from the latched state is measured (an example of one such measurement is shown in Fig. 34C). After averaging, the value of τ is extracted. For several such latches τ is found to be between 1 and 100 s and to weakly depend upon temperature for T < 200 mK.
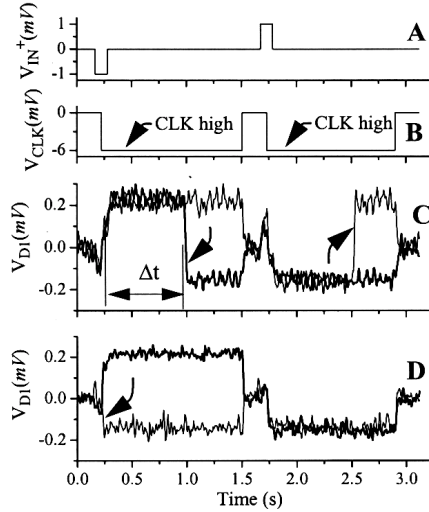
Figure 34. Errors in QCA latch operation. (A) input signal; (B) clock signal; (C) static, or decay errors (two errors for two traces are pointed by arrows); (D) Switching error (arrow points the switching into the wrong polarization for one trace).

The static BER depends on the retention time as

$$p_{stat} = 1 - \exp(-t/\tau), \tag{5}$$

which for t $\ll \tau$ is reduced to $p_{stat} \approx t/\tau$. At a clock rate of 100 MHz this gives the static BER of about $\sim 10^{-9}$ for $\tau = 10$ s.

4.5.2 Switching errors

Due to the excitations caused by finite temperature and external noise, there is always a finite probability for an electron to switch to a "wrong," energetically unfavorable state. One obvious solution for reducing the switching error is to maximize

the applied input voltage, thus moving two binary states apart in energy. The input signal cannot be increased infinitely, because otherwise the Coulomb barrier separating these states would be overcome by the input and the whole MBM operational scheme would no longer apply. The condition $V_{IN} < e/C_{IN}$ sets the limit on the maximum possible signal.

The probability of a "thermal" switching error in the case where excitations are caused only by the finite temperature, T, of the electron subsystem is given by [21]:

$$p_{sw} = A \exp(-\Delta/kT) , \tag{6}$$

where $\Delta = e\alpha\Delta V_{IN}$ is the energy difference applied between the end dots caused by the input differential voltage, and α is a constant defined by the voltage distribution between the input and junction capacitances in the latch. The pre- exponential factor $A=1/2$ is due to the 50% probability of switching to either end dot with no input applied.

For normal latch operation, $\Delta \sim 0.2 E_C$, where E_C is the charging energy of a dot, is a practical value. Inputs greater than this risk causing an electron to switch between end dots, even with the clock LOW, as mentioned above. In addition, since power gain is an objective of clocked QCA [19], the energy supplied by the inputs would be comparable to that supplied by the clock, which is undesirable. For a latch with junction capacitance of 300 aF, and corresponding charging energy $E_C \sim 250$ μeV, a reasonable Δ for latch operation is 50 μeV.

Formula (6) does not take into account any other possible excitations which also might lead to switching errors. In the presence of external noise at the input gates, switching errors occur even at 0 K. For example, noise can reach the sample through the wires or by means of radiation due to insufficient shielding [29]. Other sources of random signals are internal, for example, random background charge (RBC) fluctuations. Therefore, the temperature dependence of the switching error might deviate significantly from expression (6), although the exponential dependence on the size of the input signal will still be correct. To account for this deviation we used an empirical formula:

$$p_{sw} = 1/2 \exp(-\Delta/kT_N), \tag{7}$$

where T_N is some effective "noise temperature." The experiment of Fig. 27 is used to determine p_{sw}. To do this, the number, n, of electron transitions into a wrong state is accumulated for the N clock cycles. The probability of a switching error is given by the ratio $p_{sw} = n/N$. Special care is taken to make sure that the outcome of the experiment is not affected by decay errors. For this purpose we used clock pulses with rise time, t_R, much shorter than the average lifetime, τ, of an electron in a metastable state so that $t_R/\tau > 10^{-4}$. The working point of the latch is initially set to provide $p_{sw} = 1/2$ at $V_{IN} = 0$.

The results of switching error measurements are shown in Fig. 35. It is clear that the probability of an error drops exponentially as the size of the input is increased. The parameter T_N corresponding to the best fit of data is found to be 250 mK.

Note that the output signal produced by a QCA latch that acts as an input for a subsequent latch in a line of latches is fixed due to the discreteness of the electron switching mechanism. The interaction between the two latches is set by the latch-to-latch

coupling, and the corresponding switching error remains constant independent of the input.

The reduction of the switching error in clocked QCA to BER levels acceptable in modern digital applications (<10^{-10}), can be achieved in MQCA devices having much higher charging energy and therefore much higher energy difference between logic states.
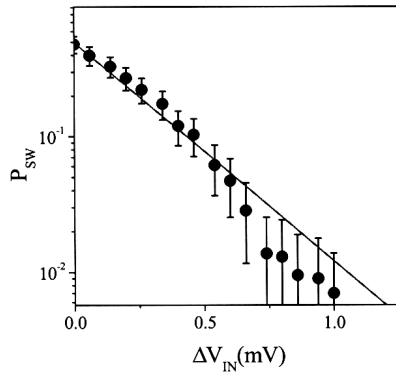
Figure 35. Switching error in a QCA latch vs the input voltage difference. Solid line - fitting (7) for T_N =250 mK, α =0.08. Dots - experiment. The mixing chamber temperature T = 100 mK. Error bars correspond to $(P_{sw})^{1/2}$.

4.5.3. Dynamic errors

The dynamic errors [21] will become a limiting factor as the frequency of the input signal approaches the tunneling rate. This type of error cannot be measured in the current experimental setup due to the bandwidth limitations mentioned above. The estimate based on the parameters of the junctions shows that for the metal TJ latch, dynamic errors will become significant for clock frequencies approaching 10^8 Hz [21]. For MQCA, the switching speeds are expected to be on the order of fs. This would allow acceptable levelsof dynamic errors for clock speeds in the ps range.

4.5.4 RBC fluctuations and digital errors

The most serious problem causing digital errors in single-electron logic devices stems from their susceptibility to the RBC fluctuations [30] (*e.g.,* the allowed fluctuations for a single-electron latch are only on the order of 0.01*e* [21]). The RBC noise have typical 1/*f*-like power spectrum causing random shifts in the charging responses of single-electron devices vs time. In our experiment, a typical time ("stability time") during which the device remains within the 0.01*e* charge tolerance limit is on the order of 10^{3}s. After that period some adjustments need to be done to the device settings to keep it in the operational mode. As mentioned above, the higher frequency RBC fluctuations occurring at a rate comparable with the clock raise time can cause switching errors even during the stability time interval. By using other device fabrication techniques the goal of well defined background charges seem to be achievable in principle. For example, recent results on Si SET devices [31] showed excellent stability over a period of a year, which brings some optimism to the problem.

4.5.5 Total BER in QCA latch

The total probability of digital error in a latch, p_{tot} , is given by the sum of the errors listed above. For the MTJ QCA latch described above $\tau \approx 10$ s, so the static error is p_{stat} $\approx 10^{-6}$ for the clock rate of 10^5 Hz. At this clock rate we estimate $p_{dyn} < 10^{-6}$ [21] and the effect of "static" RBC fluctuations can be neglected if the experiment is performed during the stability time interval. An experimentally obtained value for the probability of switching errors in the latch controlled by the neighboring latch, is $p_{sw} = 4 \times 10^{-2}$. Therefore it is clear that p_{tot} in the TJ implementation of the QCA latch is dominated by switching errors.

This number is rather high compared to error rates achievable in other low-switching energy digital circuits, such as single-flux quantrons, with $p < 10^{-12}$ [32]. But as QCA elements shrink (and the corresponding charging energy grows) the p_{sw} is expected to drop dramatically. Estimates [21] show that for the metal TJ single-electron "parametron"-latch with a dot size of about 5 nm ($E_C \sim 0.15$ eV) operating at 15 K, the total BER can be kept below 10^{-10} for clock speeds up to 10^9 Hz; and for an MQCA latch ($E_C \sim 1$ eV) operating at 77 K, the expected level of BER is $\sim 10^{-14}$ at the clock speed of 10^{10} Hz.

5. Conclusion

The experiments so far showed the feasibility of the QCA architecture, demonstrating functional cells, logic gates, latches and SRs. Future research includes the search for possible QCA cell candidates using metal nanoclusters and molecular complexes, interfacing and assembling of QCA devices [33,34]. This is headed towards significantly higher operating temperatures. Another important field of experimental QCA research lies in the area of the high-speed QCA studies. With the use of RFSET-electrometers, probing of single-electron QCA events in real time becomes possible. This allows the determination of the limiting parameters for QCA switching, and thus opens the door to the real-world application of nanostructures to computation and signal processing. Once this is achieved, real QCA applications can be contemplated that employ nanoscale size devices for logic and computation.

Acknowledgements

References

1. S. Borkhar, private communication.
2. C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, Nanotechnology, Vol. 4, 49 (1993).
3. C. S. Lent, P. D. Tougaw and W. Porod *PhysComp '94*: Proceedings of the Workshop on Physics and Computing, IEEE Computer Society Press (1994).
4. D. V. Averin and K. K. Likharev. Chapter 6 in *Mesoscopic Phenomena in Solids*, ed. B. L. Altshuler, P. A. Lee, and R. A. Webb. Amster-dam: Elsevier (1991).
5. C. S. Lent and P. D. Tougaw, J. Appl. Phys. Vol. 75, 4077 (1994).
6. T. A. Fulton and G. H. Dolan, Phys. Rev. Lett., Vol. 59, 109 (1987).

7. L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, *Proceedings of the NATO Advanced Study Institute on Mesoscopic Electron Transport,* edited by L. L. Sohn, L. P. Kouwenhoven, and G. Schön (Kluwer Series E345, 1997).
8. Yu. A. Pashkin, Y. Nakamura, and J. S. Tsai, Appl. Phys. Lett., Vol. 76, 2256 (2000).
9. P. Lafarge, H. Pothier, E. R. Williams, D. Esteve, C. Urbina, and M. H. Devoret, Z. Phys. B, Vol. 85, 327 (1991).
10. G. L. Snider, A. O. Orlov, I. Amlani, G. H. Bernstein, C. S. Lent, J. L. Merz, and W. Porod, Jpn. J. Appl. Phys, Vol. 38, 7227 (1999).
11. A .O. Orlov, I. Amlani, G. H. Bernstein, C. S. Lent, and G. L. Snider, Science, Vol. 277, 928 (1997).
12. I. Amlani, A. O. Orlov, R. K. Kummamuru, G. H. Bernstein, C. S. Lent, and G. L. Snider, Appl. Phys. Letters, Vol. 77, 738 (2000).
13. I. Amlani, A. O. Orlov, G. Toth, C. S. Lent, G. H. Bernstein, and G. L. Snider, Science, Vol. 284, 289 (1999) .
14. M. P. Anantram, V. P. Roychowdhury, J. Appl. Phys., Vol. 85, 1622 (1999) .
15. C. S. Lent, P. D. Tougaw, and W. Porod, *PhysComp '96*, edited by T. Tofoli, M. Biagfore, and Joao Leao (New England Complex Systems Institute, Cambridge, MA, 1996), p. 186.
16. C. S. Lent and P. D. Tougaw, Proceedings of the IEEE., Vol. 85, 541 (1997).
17. R. W. Keyes and R. Landauer, IBM J. Res., Vol. 14, 152 (1970).
18. The 2001 edition of the Semiconductor Industry Association's International Technology Roadmap for Semiconductors (ITRS) (http://public.itrs.net).
19. J. Timler and C. S. Lent, J. Appl. Phys., Vol. 91, 823 (2002). R. K. Kummamuru, J. Timler, G. Toth, C. S. Lent, R. Ramasubramaniam, A. O. Orlov, G. H. Bernstein, and G. L. Snider, Vol. 81, 1332 (2002).
20. K. K. Likharev and A. N. Korotkov, Science, Vol. 273, 763 (1996).
21. A. N. Korotkov and K. K. Likharev, J. Appl. Phys., Vol. 84, 6114 (1998).
22. G. Toth and C. S. Lent, J. Appl. Phys., Vol. 85, 2977 (1999).
23. D. V. Averin and A. A. Odintsov, Phys. Lett. A, Vol. 140, 251 (1989).
24. A. O. Orlov, I.Amlani, R. K. Kummamuru, R. Ramasubramaniam, G. Toth, C. S. Lent, G. H. Bernstein, and G. L. Snider, Appl. Phys. Lett., Vol. 77, 295 (2000).
25. L. J. Geerligs, V. F. Anderegg. and J. E. Mooij, Physica (Utrecht) 165&166, 973 (1990).
26. A. O. Orlov, R. K. Kummamuru, R. Ramasubramaniam, G. Toth, C. S. Lent, G. H. Bernstein, and G. L. Snider, Appl. Phys. Lett, Vol. 77, 295 (2001).
27. R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, Science, Vol. 280, 1238 (1998).
28. A. O. Orlov, R. Kummamuru, R. Ramasubramaniam, C. S. Lent, G. H. Bernstein, and G. L. Snider, unpublished.
29. J. M. Hergenrother, M. T. Tuominen, J. G. Lu, D. C. Ralph, M. Tinkham, Physica B 203, 327 (1994).
30. A. N. Korotkov, R. H. Chen, and K. K. Likharev, J. Appl. Phys. 78, 2520 (1995)
31. N. M Zimmerman, W. H. Huber, A. Fujiwara, and Y. Takahashi, Appl. Phys. Lett, Vol. 79, 3188 (2001).
32. Q. P. Herr, and M. J. Feldman, Appl. Phys. Lett, Vol. 69, 694 (1996).
33. M. Lieberman, S. Chellamma, B. Varughese, Y. Wang, C. Lent, G. H. Bernstein, G. Snider, and F. C. Peiris, *Annals New York Academy of Sciences*, Vol. 960, 225 (2002).
34. Q. Hang, Y. Wang, M. Lieberman, and G. H. Bernstein, Appl. Phys. Lett., Vol. 80, 4220 (2002).