Experimental demonstration of clocked single-electron switching in quantum-dot cellular automata

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A device representing a basic building block for clocked quantum-dot cellular automata architecture is reported. Our device consists of three floating micron-size metal islands connected in series by two small tunnel junctions where the location of an excess electron is defined by electrostatic potentials on gates capacitively coupled to the islands. In this configuration, the middle dot acts as an adjustable Coulomb barrier allowing clocked control of the charge state of the device. Charging diagrams of the device show the existence of several operational modes, in good agreement with theory. The clocked switching of a single electron is experimentally demonstrated and advantages of this architecture are discussed. © *2000 American Institute of Physics.* [S0003-6951(00)03428-8]

The computational approach known as quantum-dot cellular automata (QCA) uses single electrons in interacting quantum dots to encode and process binary information.[1] In the last few years, several experiments confirming QCA operation and demonstrating basic logic units have been reported.[2] Recent theoretical work suggested an important improvement in QCA architecture, in that by periodically modulating interdot barriers, clocked control of QCA circuitry could be accomplished.[3]

Clock controlled QCA systems have many advantages such as power gain, pipelining, and reduced power dissipation. Power gain is possible because energy can be supplied to each cell directly by the clock lines rather than passed from the inputs alone. Pipelining is possible because clocked cells can be placed in a locked state which acts as a latch, allowing an array to be broken into subarrays, with each working on different parts of a computational problem. If the clock modulation rate is slow compared to interdot tunneling times, the system remains close to the ground state during the entire switching process, leading to minimal power dissipation.

Clocked control of QCA arrays is accomplished in three phases. First, prior to applying new inputs, the cells are brought to a depolarized (''null'') mode. In the semiconductor version of QCA circuits, for example, this can be accomplished by lowering the interdot barriers using gates. In the second (''active'') phase, inputs are applied to the QCA array, and the barriers are slowly raised, moving the system to its new ground state. Finally, the barriers are raised high enough that tunneling between the dots is suppressed, and electrons are ''locked'' in the dots. In this mode of operation, the electrons remain trapped on the dots regardless of the state of the input signal.

Although semiconductor implementations of clocked QCA arrays were suggested first, a clocked architecture utilizing metal tunnel junction technology was recently proposed.[4] For QCA arrays implemented in metal islands coupled by capacitors and oxide tunnel junctions, control over barrier heights is a much harder task than it is in semiconductor QCA arrays because oxide barriers cannot be varied by gate potentials. Toth and Lent[4] suggested a scheme for clocked control of the switching in metallic QCA cells where a modulated barrier is replaced with an extra island, or dot, situated between the two dots forming a QCA half cell[5] [Fig. 1(a)]. Each dot of the device is capacitively coupled to a

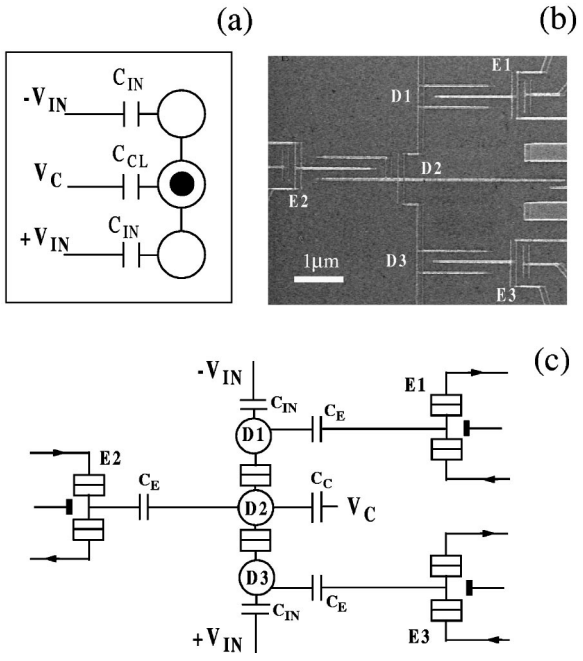

FIG. 1. (a) QCA half cell with extra dot used as an adjustable barrier. (b) Scanning electron microscopy micrograph of the device. Input gates are not shown. (c) Schematic diagram of experiment. $D1..D3$ form a half-cell, $E1..E3$ are electrometers.

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corresponding gate, and the differential input signal (which comes from either external leads or an adjacent half cell) is applied to the top and bottom gates. In the Toth–Lent scheme, the half cell is charged with one excess electron. The input signal is much smaller than the period of the Coulomb blockade oscillations $\Delta V_{\mathrm{IN}}=e/C_{\mathrm{IN}}$. The clocking signal on the middle gate sets the potential on the middle dot, varying the effective barrier between the top and bottom dots. The three operational modes of such a device, null, active, and locked, are defined by the combination of input and clock biases. In the null mode, the minimal energy configuration occurs when an electron is localized on the middle dot, even if the signal input is applied. In the active mode, even a small input signal can polarize the half cell and an electron moves either to the top or the bottom dot to minimize the energy of the system. For this reason this mode is also called ''the evaluation mode.'' Finally, in the locked mode, the energy of the configuration where an electron is in the central dot is much higher than for the other two configurations in which the electron is localized on the top or the bottom dot. As a result, the electron remains trapped on the top or the bottom dot, regardless of the input signal. This mode provides ''memory,'' or latching, for a half cell since it remains polarized independent of the input signal.

In this letter, we report the fabrication and characterization of a clocked QCA device implemented in the Al–AlO_x system. The device we study consists of three micron-size Al islands, or ''dots,'' $D1$, $D2$, and $D3$. They are connected by two tunnel junctions forming a clocked QCA half cell. Three leads capacitively coupled to the dots serve as signal $(+V_{\mathrm{IN}},-V_{\mathrm{IN}})$ and clock V_C inputs. A micrograph of the device is shown in Fig. 1(b). Each dot is also coupled to a separate single-electron electrometer $E1$, $E2$, and $E3$ by capacitors C_E [Fig. 1(c)]. This configuration allows us to measure the charge on each dot simultaneously. The $Al/AlO_x/Al$ tunnel junctions are fabricated on an oxidized Si substrate by a standard electron beam lithography and shadow evaporation technique.[6] Experiments are performed in a dilution refrigerator with a base temperature of 15 mK. Signals in the detectors are measured using standard ac lock-in techniques, and a magnetic field of 1 T is applied to suppress the superconductivity of aluminum. The values of gate and junction capacitances are extracted using the procedure described in Ref. 2, yielding a typical value of junction capacitance of about 300 aF.

In addition to the extra dot in the half cell, the clocked device has one important difference from QCA devices studied previously,[2] i.e., it has no dc connection to the environment.[7] Therefore, electrons can only be switched between the dots in response to biases applied to the gates, while the total number of electrons on the dots remains constant. Calculations of Toth and Lent[4] were performed for QCA cells precharged with one extra electron. Our device, however, is initially electrically neutral. Though it is simpler to understand the operation of a half cell charged with one electron, any change of the initial charge of the cell is equivalent to a fixed offset of the biases V_{IN} and V_C, so the considerations of Ref. 4 can be applied to the device under study.

To characterize the response of the half cell, we measure

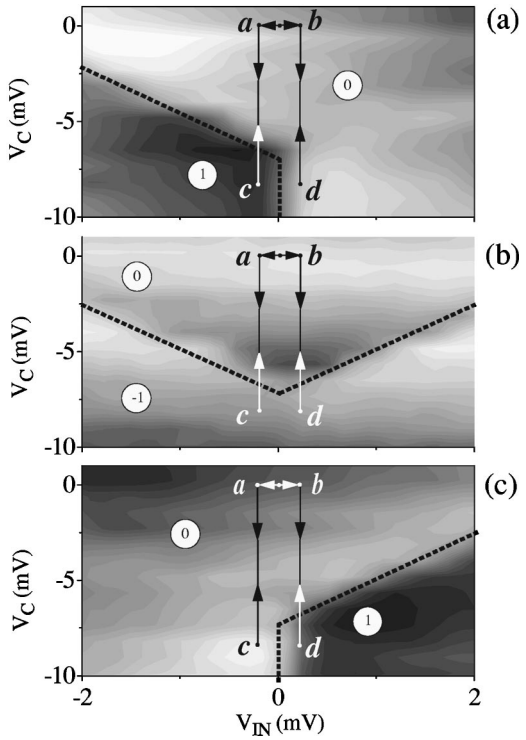

FIG. 2. Equilibrium charging diagram of the clocked QCA half cell, measured by electrometers $E1..E3$. In the black–white color scheme negative dot voltage is dark, and positive dot voltage is light: (a) top dot; (b) middle dot; (c) bottom dot. Numbers in the circles represent the number of excess electrons on the respective dots within the areas confined by the dashed lines. Plus sign corresponds to an excess electron, while minus sign corresponds to a missing electron. Dashed lines on the plots are calculated using the modeling algorithm described in Ref. 4 and define the borders between equilibrium ground state charge configurations.

detector signals in the device as a function of input and clocking signals. Figures 2(a)–2(c) show the experimentally measured potential profiles of each dot as a gray scale map.[8]

The charging diagrams illustrate the electron transitions in a half cell. For example, with the clock biased at $V_C=0$, and if the input signal changes from $V_{\mathrm{IN}}=-0.2\,\mathrm{mV}$ to $V_{\mathrm{IN}}=0.2\,\mathrm{mV}$ (path from a to b in Fig. 2), no single electron transfer happens and the system remains in the same charge state (0,0,0). (Numbers in parentheses represent number of electrons in the top, middle, and the bottom dot, respectively). Around this point ($V_C=0$, $V_{\mathrm{IN}}=0$) this charge configuration (0,0,0) has the lowest energy. Following the definition of Toth and Lent this is a null mode, where a cell remains unpolarized even when the input signal is applied. A change in the clocking bias polarizes the half cell. For instance, if an input bias is set to $V_{\mathrm{IN}}=-0.2\,\mathrm{mV}$ and the clock bias changes from $V_C=0\,\mathrm{mV}$ (state (0,0,0)) to $V_C=-6\,\mathrm{mV}$, then $D1$ gains an electron, and this electron comes from $D2$ leaving a ''hole'' (missing electron) behind (path from a to c in Fig. 2) [state (1, −1, 0)]. At the same time the number of electrons on $D3$ does not change, although the potential on that dot becomes significantly more positive. Similarly, by moving from b to d, a transition from (0,0,0) to (0,−1,1) state is accomplished. The transition from the null into the active mode occurs at the dotted line when the clocking signal produces a transition between two states, where the final state is determined by the polarity of V_{IN}. Further change of the clock signal towards c (or towards d)

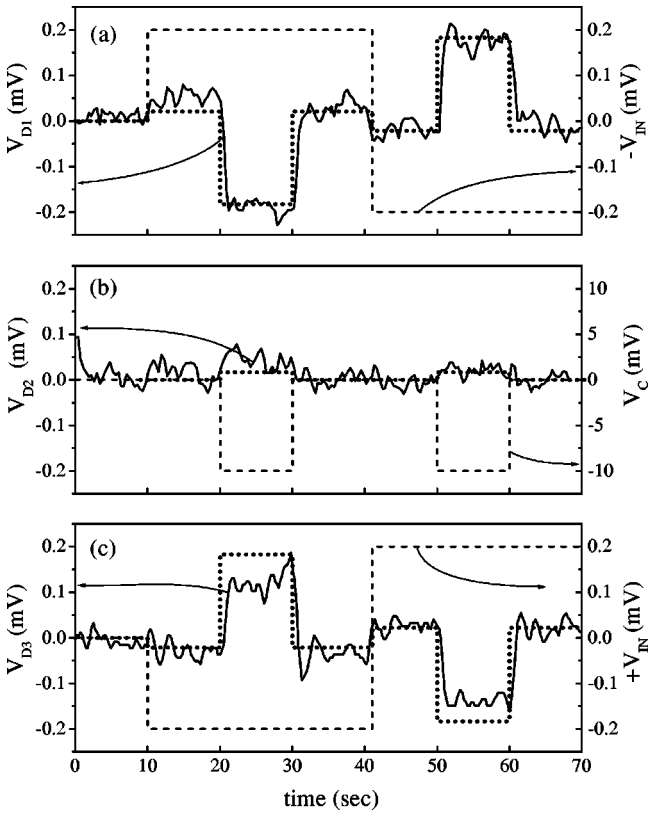

FIG. 3. Clocked switching of the QCA half cell. Measured (solid line) and calculated (dotted line) response to the input and clocking signals along with applied input signals (dashed line). Finite slopes in the experimental curves are defined solely by the time constants of the phase detectors, and do not characterize the speed of electron switching: (a) top dot; (b) middle dot; (c) bottom dot.

in Fig. 2 brings a half cell into the locked mode. Here it is energetically unfavorable for an electron to move to the middle dot, so the middle dot keeps its positive net charge, and an electron stays either on the top or bottom dot, depending on the input bias in the evaluation mode. If the polarity of the input signal is reversed, the electron is trapped in a metastable state,[4] which does not correspond to the minimal energy configuration. The lifetime of this state is limited by cotunneling effects.[9] For the device under study, the estimated lifetime is on the order of 10^{-6} s, which is about seven orders of magnitude smaller than the typical time scale of a scan in our experiment. [For high-frequency ($f > 10$ MHz) applications, however, this would be sufficient to provide latching]. Thus, the phase diagrams in Fig. 2 correspond to the equilibrium ground state and do not show the metastable state in the locked mode. To demonstrate the latching in the existing experimental setup, one would need to increase the lifetime of the metastable state, which can be achieved, for example, using multiple junctions to connect the dots.

An important feature of the clocked QCA architecture is that the polarization of the cell is changed using the clock signal. The small input signal only defines the final cell polarization, while the clocking signal drives the electron transfer. To demonstrate this, the following experiment is performed. First ($t=0$ s) in Fig. 3, the system is set to a null mode. Here $V_C=0$, and $V_{IN}=0$ (input bias is set in the middle of the line connecting points *a* and *b* in Fig. 2). Then ($t=10$ s), the input differential signal $V_{IN}=-0.2$ mV is applied to the input gates. This creates some asymmetry in the energy states on the top and bottom dots (point *a* in Fig. 2), but the system remains in the null mode. As can be seen in Fig. 3, the dot potentials indeed remain very close to zero. Then ($t=20$ s) the clock signal changes from $V_C=0$ to $V_C=-8.5$ mV (corresponding to a movement from *a* to *c* in Fig. 2). Clocking bias drives the system from the null mode with charge configuration (0,0,0) through the transition (the active mode) where an electron moves to $D1$ leaving a hole on $D2$, into the locked mode (charge configuration (1, −1, 0)). At $t=30$ s, the clock signal is set to 0 (movement from *c* to *a* in Fig. 2), and the cell again is driven in the null mode. At $t=40$ s, the polarity of the input voltage is reversed (movement from *a* to *b* in Fig. 2), and at $t=50$ s the clock signal is again applied (movement from *b* to *d* in Fig. 2), so the half cell acquires the opposite polarization (0,−1,1).

To compare the experimental results with theory we perform calculations of the dot potentials in the clocked switching scheme. We calculate the charging energies and the dot voltages for the possible charge configurations using experimentally determined capacitance values. The finite temperature effects are obtained by averaging the dot voltages corresponding to the different charge configurations assuming Boltzmann statistics. Since the device is floating, the net charge is assumed to be zero. Charge configurations which do not fulfill this requirement are excluded from the thermal averaging. The results of calculations shown in Figs. 2 and 3 are in good agreement with experimental data.

In conclusion, we fabricated and tested a clocked metal tunnel junction QCA device which can be used as a building block for the clocked QCA architectures. Charging diagrams for every dot in the half cell were measured simultaneously and show a clear picture of single electrons switching between the dots. We experimentally demonstrate that a clock signal can be used to control the charge state of the QCA cell. Our experimental data show a good agreement with the results of theoretical calculations.

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