Experimental demonstration of a QCA shift register and analysis of errors

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Abstract

Quantum-dot Cellular Automata (QCA) is a device architecture that uses position of electrons in quantum-dot arrays to implement digital logic. We present the experimental demonstration of a two-stage QCA shift register and an analysis of errors encountered in its operation.

Introduction

The microelectronics industry has seen phenomenal improvements in device size, speed and integration for the past four decades. Much of this improvement has been brought about by reducing the channel length of FETs and packing more devices into a smaller area. At gate sizes of tens of nanometers, device non-idealities multiply. As device density increases exponentially, the power dissipated on the chip is reaching intolerable levels. A possible way to continue scaling down devices is to move from an FET based logic architecture to one that is low power and compatible with nanometer scale electronic devices. Quantum-dot Cellular Automata (QCA) is one such logic architecture which is capable of realizing extremely high packing densities since it can potentially be implemented using quantum-dots or molecules, and extremely low power dissipation since it uses the position of electrons in quantum-dot arrays rather than currents to implement digital logic (1).

A QCA cell is a bistable system with two degenerate ground states and is capable of encoding one bit. One way to implement a cell is by using four quantum-dots arranged at the four vertices of a square, connected by tunnel junctions, and sharing two extra electrons among them. Due to electrostatic repulsion, the two electrons in each cell are forced to the opposite corners along one of the two diagonals. These diagonally aligned charge states (polarizations) are the two ground states of the system and are used to encode '0' and '1'. Switching between the two states occurs when discrete electrons tunnel between the dots from one ground state to the other due to an external input. Lent et al. (2) developed a complete set of the basic digital logic gates implemented using arrangements of QCA cells. In recent years, several QCA devices such as a QCA cell, majority gate and a latch (3), have been fabricated and tested. Switching in the four-dot cell described above is controlled solely by the input signal applied to it. However, to make large scale pipelined digital architectures using QCA devices, it is desirable to be able to control switching using a clock signal.

Clocking in QCA devices

Apart from enabling pipelining for large QCA circuits, clocking allows cells to be locked into a state, giving rise to memory, and the clock signal can also provide energy to the cell, making power gain possible (4). Clocking is achieved in QCA devices by controlling the tunnel barriers using an external clock signal. A very simple structure where barriers are modulated to control switching was discussed by Keyes and Landauer as early as 1970 (5). This system consists of a potential well which can be varied from a monostable to a bistable state by varying a barrier within the well. To write a bit into the device, a small input is applied and the barrier is slowly raised. The system settles into the state suggested by the input. To erase the bit, the barrier is lowered. A similar scheme of operation was proposed for QCA devices by Lent et al (2), called adiabatic switching. Here, the barriers between the dots are modulated using a clock signal. The clock signal causes switching in the cell, while a small input signal decides the direction of the switching. In semiconductor based implementations of QCA devices where dots are formed by depletion, tunnel barriers can easily be modulated using external gates. However, in metal based implementations like the current device, the barrier is formed by an oxide layer and hence cannot be controlled externally. Therefore, in this implementation, an extra dot is added to the device, whose potential acts as a barrier that can be modulated using a clock signal.

Device fabrication

The current device was fabricated using aluminum islands and aluminum oxide tunnel junctions on an oxidized silicon substrate (6). Fig. 1(a) shows an SEM image of the

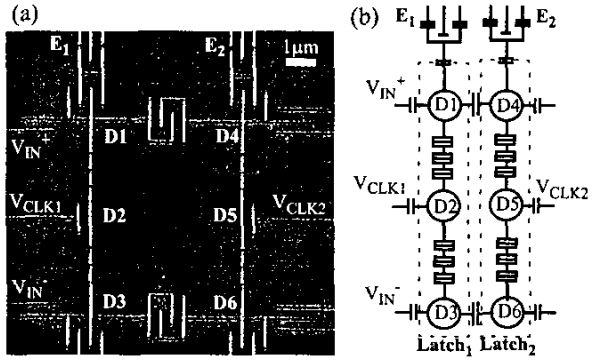

Figure 1. (a) Scanning electron micrograph of the QCA shift register. (b) Schematic diagram of the device.

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device. We use electron beam lithography on a double layer resist and dual angle evaporation with an intermediate oxidation step to form overlaps of about 50nm by 50nm, which form the tunnel junctions. The area of tunnel junctions determines the junction capacitance which dominates total dot capacitance and hence the charging energy of the device ($E_C = e^2/C_\Sigma$). Single electron charging effects are observed when the charging energy of the device is much greater than the characteristic energy of thermal fluctuations i.e., $E_C >> k_BT$. The area of our tunnel junctions limits the temperature of operation of the device to below 200mK. The experiment is performed in a dilution refrigerator with a base temperature of about 15mK, in a magnetic field of 1T to suppress superconductivity in aluminum.

The schematic diagram of the shift register is shown in Fig. 1(b). It consists of two QCA latches capacitively coupled to each other. Each latch is made up of three dots or islands. A clock signal is applied to the middle dot through a capacitor, to modulate its potential and control electron tunneling between the top and the bottom dots. Dots D_1, D_2 and D_3 form latch L_1 while dots D_4, D_5 and D_6 form latch L_2. E_1 and E_2 are the electrometers used to measure the potentials on dots D_1 and D_4 respectively. Inputs V_{IN}^+, V_{IN}^- and clocks V_{CLK1} and V_{CLK2} are applied to the device through capacitors. Three junctions are used between each pair of dots instead of a single junction, in order to reduce second order tunneling effects (co-tunneling), and enhance retention time of the latch.

Operation of QCA shift register

A QCA shift register is a line of latches where binary information can be transferred in a sequential manner from one latch to the next. Each latch is a short-term memory element capable of storing a bit for one or more clock cycles. To understand the operation of a latch, it is helpful to have a nomenclature that classifies its behavior according to the clock voltage. Switching in the latch is controlled by adjusting the effective barrier between the top and the bottom dots. When the effective switching barrier is low, the latch is in the 'null' state and does not have any polarization. In this state the latch holds no information. As the barrier height is increased, the latch becomes 'active' and the polarization takes on a definite value determined by the inputs applied to the top and bottom dots. When the barrier height is large enough to suppress switching over the relevant time scale, we say the latch is in the 'locked' state. In the locked state, the latch polarization is independent of the neighboring latches and it becomes a single-bit memory element. Note that the latch inverts the input since a positive input would attract an electron which brings a negative potential with it.

Phase-shifted clock signals are used to switch the latches sequentially and move bits along the shift register one latch at

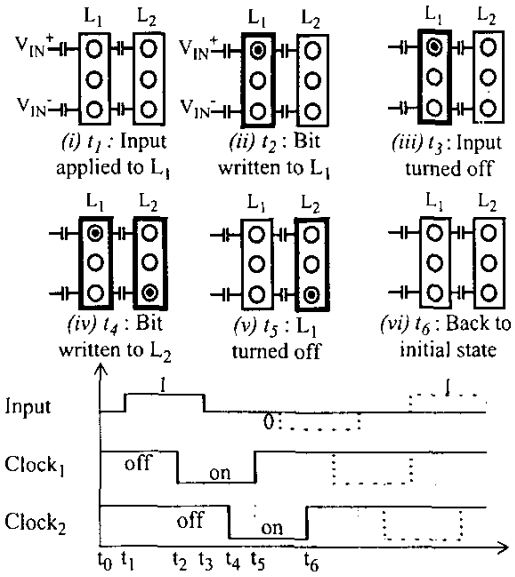

Figure 2. (a) Sequence of events in the operation of a two-stage QCA shift register. (b) Signals applied to the shift register to transfer a single bit (solid line) or multiple bits (dotted line).

a time. The signals applied for the operation of a two-bit shift register are shown schematically in Fig. 2. Differential input signals V_{IN}^+ and V_{IN}^- are applied to the first latch (L_1). When clock signal (clock 1) is applied to the latch, an electron moves from the middle dot to either the top or bottom dot depending on the input. Once latch L_1 switches, the input can be removed without losing the bit stored in it. When clock 2 is

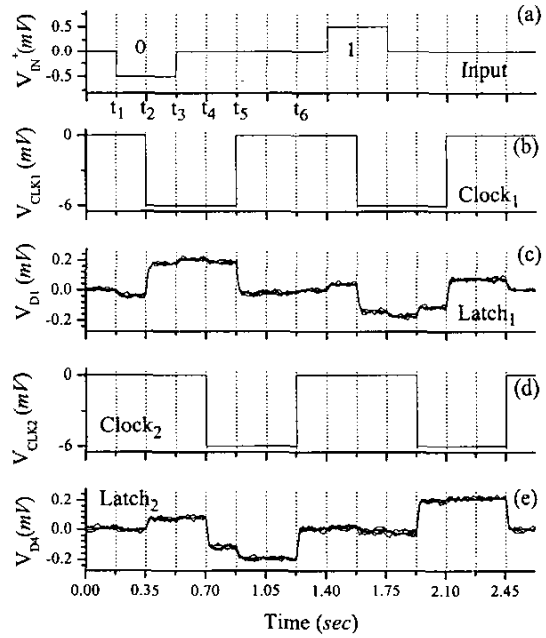

Figure 3. QCA shift register experiment. (a) signal input; (b) clock applied to latch 1; (c) measured potential on dot D1; (d) clock applied to latch 2; (e) measured potential on dot D4.

turned on, L_2 switches in the direction defined by latch 1, and the binary information gets copied into latch 2. Now, latch 1 can be turned off and the bit is stored in latch 2. As new bits appear at the input, older bits move forward along the shift register one step at a time.

To demonstrate the operation of the shift register, an experiment similar to the one described above is performed, as shown in Fig. 3. First, both the latches are biased in their respective null states. At t_1, an input is applied to latch L_1. No switching occurs since the latch is in the null state. When the clock is applied at t_2, L_1 switches and we see a positive potential on dot D_1, showing that an electron has tunnelled into D_3. Note that while L_1 switches, L_2 remains turned off and so does not contribute to any 'back-influence' on L_1. At t_3, the input is removed and L_1 stays in the locked state, and the bit (inverted) is now stored in L_1. At t_4, clock 2 is applied to latch L_2 and it switches, taking L_1 as an input. L_1 is switched off by turning off its clock, at t_5 and the bit is now stored in L_2 until it is switched off at t_6. The same sequence is repeated after t_6, for the opposite input.

Errors in a QCA shift register

While the shift register operates as expected, errors do occur and an identification of the types of errors and their properties is necessary. The errors encountered in the operation of a QCA shift register at low clock speeds can be classified into two types namely 'decay' or 'static' errors and 'switching' or 'thermal' errors (7). Decay errors occur when the information stored in a latch is lost before the end of the clock cycle. Fig. 4(c) shows two examples of decay errors where the latch switches into the wrong state while the clock is still on. Switching errors occur when the latch switches into the wrong state (opposite to the one suggested by the input signal) when the clock signal is applied. The dotted line in Fig. 4(d) shows an example of a switching error.

A. Decay errors

We define decay errors as events where the electron locked in the top dot tunnels out of it into the bottom dot or vice versa when the latch is in its locked state and no external input is being applied to it. Once an electron is locked into the top or the bottom dot and the input is removed, it is equally favorable to be in either the top or bottom dot since the two states have the same energy. However, the electron stays locked in the same dot since it cannot readily tunnel across multiple tunnel junctions between the two dots. The mechanism for tunneling across multiple junctions is called co-tunneling or coherent tunneling, where n electrons tunnel simultaneously across n tunnel junctions with the net effect being transfer of one electron from one end to the other. The probability of the occurrence of such an event depends mainly on the number of tunnel junctions, the resistance of each junction and the temperature. We have used six tunnel junctions between the top and bottom dots, to reduce co-tunneling and enhance the retention time of the latch to the time scale of our experiment which is about hundreds of milliseconds.

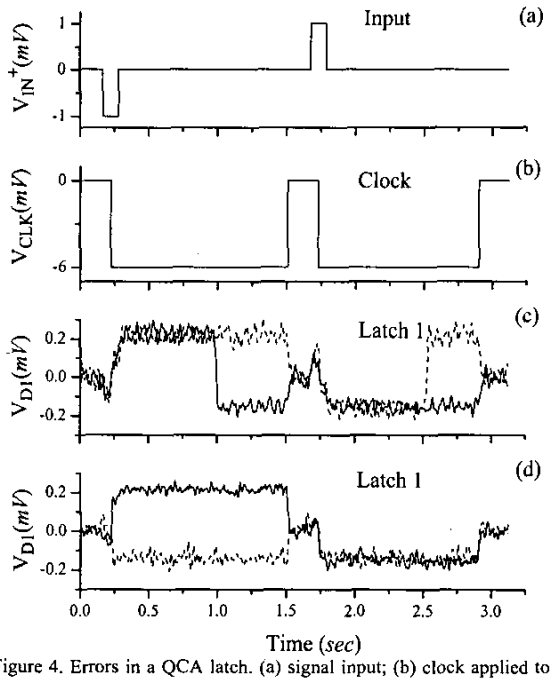

Figure 4. Errors in a QCA latch. (a) signal input; (b) clock applied to the latch; (c) two examples of decay errors; (d) dotted line shows a switching error for the first half while the solid line shows correct switching.

The probability of decay errors follows the equation

$$P_{Decay}(t) = n(t)/n_0 = 1\text{-}\exp(-t/\tau)$$

where τ stands for the retention time constant, n(t) is the total number of decay errors that happened before time t and n_0 is the total number of clock cycles. To measure the retention time constant (τ) of the QCA latch, the experiment shown in Fig. 4 was repeated 450 times. The cumulative number of errors as a function of time is shown in Fig. 5. By fitting the

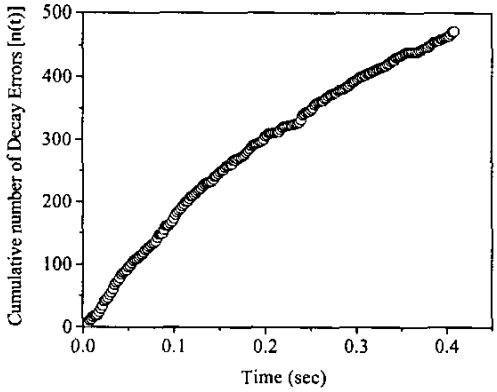

Figure 5. Cumulative decay errors in the QCA latch as a function of time. Total number of clock cycles = 900.

data to the above equation, the value of τ was found to be 0.55 sec for the current device. Since the speed of our current experiments is comparable to the retention time of the latch, decay errors are an important factor in the experiment. However, at higher clock speeds (say 100 MHz), the probability of decay errors becomes negligible.

B. Switching errors

Switching errors are caused when a latch switches into the wrong state when the clock signal is applied. Such errors could be caused due to thermal excitation, interference from external electrical noise or random background charge fluctuations. At a temperature T, the probability for errors due to thermally activated processes is given by

$$P_{SW} = 0.5 \exp(-\Delta/kT)$$

where Δ is the difference in energy between the top and bottom dots (7). 'Δ' is the energy difference between the top and bottom dots caused due to the input V_{IN} and is directly proportional to its magnitude ($\Delta = e\alpha V_{IN}$ where 'α' is a constant that depends on the voltage distribution between the input and junction capacitances in the latch). Therefore the probability of switching errors falls exponentially with the input. The presence of other sources of errors would add to the denominator of the exponent and raise the effective 'noise temperature (T_N)' of the device.

To measure the probability of switching errors at a given input we find the fraction of errors among 1000 switching cycles. Special care was taken to make sure that the experiment is not affected by decay errors, by making the time of the experiment much smaller than the retention time of the latch. We see an exponential decrease in switching error probability for latch 1 with increase in the magnitude of input, as expected. The probability of errors in latch 2 remains constant for all values of external input V_{IN} since the input seen by latch 2 is the dot potentials on latch 1 rather than the external input. From the data in Fig. 6, and estimating the value of 'α' to be 0.08, the effective noise temperature for the experiment is found to be about 330mK. Although thermal excitations, random background charges and other noise sources cause a significant number of errors at small inputs for current devices, as the devices are shrunk in size, charging energy of the dots and hence dot potential swings would increase, resulting in larger inputs from one latch to the next, and hence an exponential reduction in the number of errors.

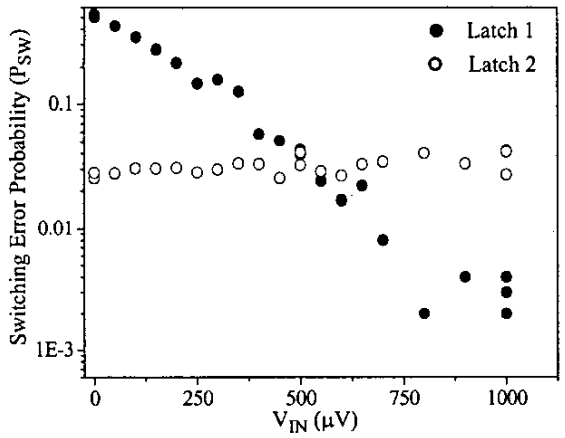

Figure 6. Rate of switching errors vs magnitude of the input signal. V_{IN} is the input applied to latch 1. Solid circles show the number of errors in latch 1 while hollow circles show the number of errors in latch 2. Each data point represents the percentage of errors in 1000 clock cycles.

Summary

We have demonstrated the operation of a shift register based on the quantum-dot cellular automata (QCA) computational paradigm. Errors in the operation of the shift register are classified into two types, 'decay' errors and 'switching' errors. We have discussed the causes of these errors and determined that by shrinking the size of the of the devices and operating at high frequencies, the number of errors can be reduced dramatically.

The current experiment is the latest in a line of experiments that demonstrate the feasibility of the QCA paradigm. Though the current prototypes operate only in millikelvin temperatures, future devices made from nanostructures or molecules are expected to work at room temperature.

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