CLOCKED QUANTUM-DOT CELLULAR AUTOMATA DEVICES: EXPERIMENTAL STUDIES

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Abstract

We present an experimental demonstration of two novel clocked QCA devices – a QCA latch and a QCA shift register. We demonstrate the operation of the devices, and discuss sources and methods of lowering the digital errors in QCA clocked devices.

1. Introduction

Quantum-dot Cellular Automata (QCA) computational paradigm [1] uses interacting quantum dots to encode and process binary information. Logic levels in QCA are represented by the configurations of single electrons in arrays of coupled quantum-dots. In the last few years, several basic QCA elements: a QCA cell, small binary wire, and digital logic gate, have been demonstrated [2]. However, in these devices power gain needed for the operation of large QCA arrays was not achievable since the only source of energy was the signal input.

To overcome this obstacle, clocked control of the QCA circuitry was proposed in [3]. Clock controlled QCA systems have many advantages over edge-driven cellular architectures. The most important of these are the ability to achieve power gain and to use pipelined architectures. Power gain becomes possible because energy can be supplied to each cell by the clock lines rather than passed from the inputs alone [4]. Pipelining is possible because each cell can be used as a latch which acts as a short-term memory. This allows us to break a large QCA array into sub-arrays, with each working on different parts of a computational problem. The original theoretical work [3] applied only to a semiconductor implementation of clocked QCA arrays, where clocking can be performed by a common back gate controlling an array of QCAs. Recently, a scheme for clocked control of metallic QCA cells with fixed barriers separating the dots was proposed [5]. In this clocking scheme an extra dot placed between the two dots of the metallic QCA cell acts as a tunable Coulomb barrier controlled by the clock signal. For a metal system, a similar clocking scheme was proposed by authors of [6] for the device they called the "single-electron parametron"[7].

In clocked QCA devices, the signal input V_{IN}, is much smaller than the clock signal V_{CLK}. The input signal only defines the direction of switching, while the actual electron transfer is accomplished by the clock signal. A very important feature of the clocked QCA architecture is the ability of a cell to provide a short-term memory to adjacent cells so that a cell remains polarized even in the absence of the input signal. This also resolves the issue of unidirectionality [8].

Here we present the experimental demonstration of novel clocked QCA devices - a QCA latch and a QCA shift register.

2. Fabrication and Measurement Technique

To demonstrate clocked QCA devices we use well established Al tunnel junction technology which combines direct E-beam lithography with a suspended mask technique [9]. In this way we fabricate thin-film Al islands separated by tunnel junctions

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on the SiO_2 substrate. The advantage of this type of QCA is relative simplicity (only 3 major processing steps: direct E-beam writing, development, and metal deposition with *in situ* oxidation), good uniformity (junction resistance in one run typically varies by only 20-30 %), and high yield (up to 100%). The disadvantage is the small charging energy $E_C = e^2/2C$ of the Al "dots" (typically < 1 meV) due to relatively large junction capacitance which limits the operational temperature to below 1K. To satisfy the condition $E_C >> kT$ the experiments are performed in the dilution refrigerator at the temperatures 50-200 mK. We use the lock-in technique to read out the electrometer signals.

3. Experimental Demonstration of QCA Latch

The QCA latch consists of three micron-size Al dots (D1-D3, Fig.1a), separated by multiple tunnel junctions (MTJ) with three gates to control the charge state of the device. Single-electron transistor E1 capacitively coupled to the dot D1 serves as an electrometer to measure the state of the latch. We use MTJs to suppress second-order tunneling processes (cotunneling) which can result in the loss of information during the hold time. (See section 5.2)
Figure 2 demonstrates operation of a QCA latch. To operate the latch the differential input signal is applied to the gates V_{IN}, and clock signal is applied to the gate V_{CLK}. As the input pulse is applied (at t_0, t_4) no charge

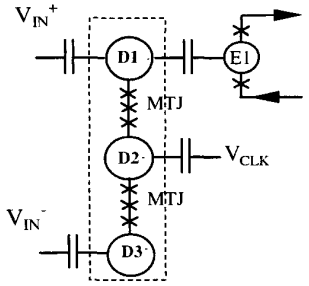

Figure 1. Schematic diagram of QCA latch. MTJ- multiple tunnel junctions, E1- SET electrometer.

transfer happens (and the latch remains neutral) until the clock signal is applied (at t_1, t_5).

The clock pulse provides energy to transfer an electron from the middle dot to the D3 (at t_1) or D1 (at t_5), in accordance with the polarity of the input signal. The input is then can be removed (at t_2, t_6). The electron remains latched in the dot thus providing a source of signal for the next latch until the clock signal is set to low (at t_3, t_7). This demonstrates the operation of a QCA latch as described in [5].

4. Experimental Demonstration of QCA Shift Register

To make a QCA shift register, two QCA latches L1 and L2 are capacitively coupled (Fig. 3) by means of the capacitors C_C. Operation of the QCA shift register requires the use of a three-phase clock (CLK1 and CLK2). The differential signal V_{IN} corresponding to logical "0" (logical "1") is applied to the input IN1-IN2 at t_0 (t_6) (Fig. 4). The latch L1 remains in the neutral state until CLK1 is applied at t_1 (t_7) in Fig. 4. When clock CLK1 is set high, the latch L1 becomes active. Once L1 is set (an electron

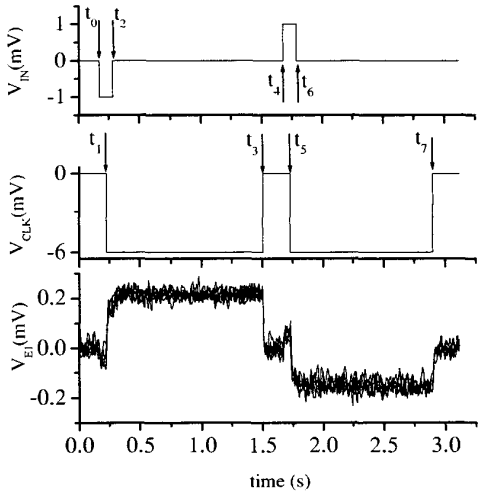

Figure 2. Operation of a QCA latch at 70 mK. Several successive traces are shown.

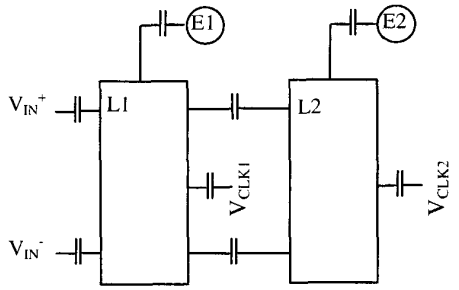

Figure 3. Simplified schematic of the QCA Shift Register.

is locked on one of the end dots), signal input is removed at t_2 (t_8) and the state of L1 does not depend on the input signal. Then the second clock CLK2 is applied to L2 at t_3 (t_9) in Fig. 4, and an electron in L2 switches in the direction determined by the state of the first latch. The second latch remains active when CLK1 is removed at t_4 (t_{10}) in Fig. 4 for as long as CLK2 is active (until t_5 (t_{11})). Thus, the above experiment demonstrates the operation of the QCA shift register. The cycle describing the operation of a QCA shift register is as follows:
neutral → input applied → 1st clock applied and 1st latch is active → input removed → second clock applied and 2nd latch is active → 1st clock is removed. At this moment the first latch becomes neutral and is ready to receive new information. The information encoded in the position of a single electron is shifted to a second latch and stored there. Thus, we demonstrate a functioning QCA shift register.

5. Error analysis in QCA Latch and Shift Register

For reliable operation of digital device all possible sources of errors must be investigated. In clocked QCA circuits the errors physically are caused by (a) thermally activated processes; (b) errors caused by random background charge fluctuations; (c) errors caused by second-order tunneling processes. From the system standpoint we can divide these errors into two basic categories of errors: (a) switching errors,

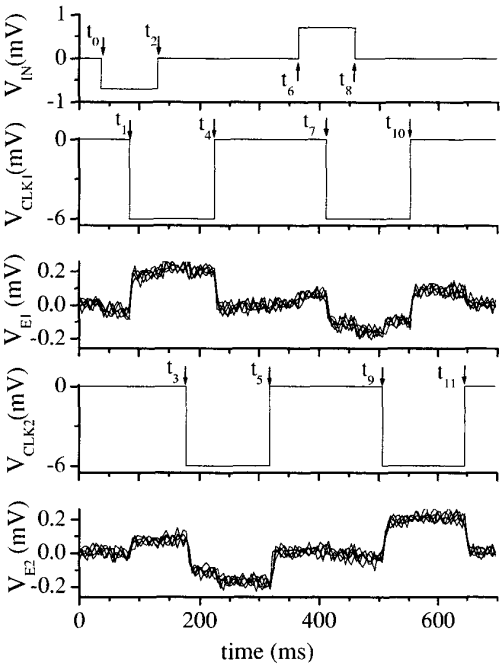

Figure 4. Operation of a metal tunnel junction QCA shift register at 70 mK (10 scans shown).

which include all possible sources of errors which force a QCA latch to switch into a "wrong" (opposite to the one suggested by the input signal) final polarization by the time the clock signal is raised to "high"; (b) "decays," errors related to the loss of information during the retention period.

5.1 Analysis of switching errors in a QCA latch

For a single latch, the probability of the "thermal" switching error is given by :

$$P_{sw.th.} = A \exp(-\Delta/kT), \qquad (1)$$

where Δ is the energy difference between the end dots caused by the input signal ΔV_{IN} [6]. Since the probabilities for an electron to switch into one of the end dots for $\Delta V_{IN} = 0$, are equal, $A = 0.5$. In turn, $\Delta = \alpha e \Delta V_{IN}$, where the coefficient α depends on the ratio of the input capacitance to the total capacitance of an end dot. In our case $\alpha \sim C_{IN}/C_{\Sigma} \sim 0.05$. For a given temperature this

error could be minimized by applying stronger input bias ΔV_{IN}. For example, the expected error probability at 200 mK for ΔV_{IN} =1 mV is: $P_{sw.th.}$ = 0.0275. To find $P_{sw.th.}$ we apply N clock pulses (typically, N = 1000) to the latch and then looked at the outcomes at the time when clock reaches steady state. The probability of switching error is then given by the ratio $P_{sw.th.} = n_{err}/N$, where n_{err} is the number of switching into the wrong state. Special care was taken to make sure that the outcome of experiment is not affected by the decay errors (see section 5.2). We used clock pulses with duration T much shorter than the average lifetime of the metastable state τ, so that $T/\tau \sim 10^{-3}$. Figure 5 shows the result of the error rate measurements. It shows good correlation between the expected and observed error for T = 200 mK. However, we did not find any noticeable change in the error probability for temperature varied from 50 mK to 200 mK. The reason for this is currently being investigated. At the same time, for a fixed temperature of 100 mK we observe a change (by a factor of ~ 2) in the slope of the exponent for different cooldowns. We believe this could be caused by a "parasitic" trapping of the switching electron in one of the islands of the MTJ. In this case the switching electron is getting stuck at one of the small islands of the MTJs, rather then moving all the way to an end dot. The random offset charge of the MTJs islands might create a local minimum in potential energy leading to parasitic trapping. This is possible because we do not have good control over the charge state of the islands forming MTJs. Since only one SET-detector per latch is used, an electron trapped into MTJ appears as being switched to a wrong (opposite) state. Thermal cycling changes the configuration of random offset charges and therefore could change the energy states in the trap. More experiments are required to resolve this discrepancy. As one obvious solution to this problem we plan to use electrometers on both of the end dots so that we can see whether a switching

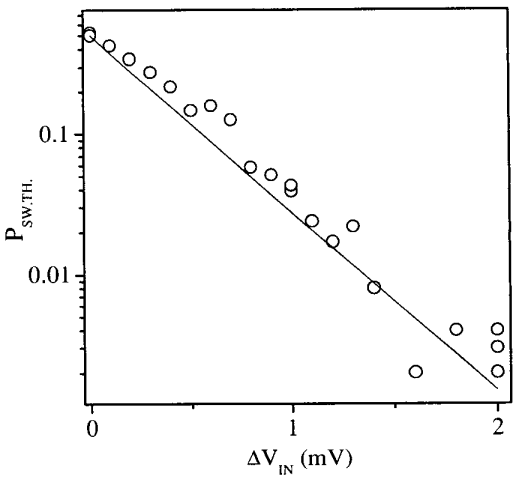

Figure 5. Switching error in a QCA latch as a function of the input potential difference.
Solid line – calculations (1) for kT=200 mK.

electron moves all the way from D1(D3) to D3(D1). Switching errors caused by the random background charge fluctuations (RBCF) are a common problem for single-electron logic devices [10]. There are two basic effects related to RBCF. "Big events," which have a very low frequency of occurrences (~ one over a day) reveal themselves as random shifts of the device charge state by at least a half period of Coulomb blockade oscillations. The slow monotonic drift (when we can see a detectable change in the position of the "phase plot" – an electrostatic 3D map which completely describes the charge state of a QCA latch [11]) causes a gradual shift in the working point of a latch which will eventually lead to a switching error. In our experiment, a typical time during which the device remains unaffected by this drift is $\tau_d \sim 10^3$ sec. Therefore, for the typical time of the experiment ~10 seconds, the effect of the drift can be neglected. Finally, so called "dynamic errors" which occur when the switching speed is too high compared to the tunneling rate ($\sim 10^{10}$ Hz for our junctions)[6] also lead to a switching error. However, at lower frequencies the probability of these errors is exponentially

small. Since our experiment is performed at low frequencies (<1000 Hz), the dynamic error can also be neglected.

5.2 "Decay" errors in a QCA latch.

We define "decays" in a QCA latch as events which correspond to the escape of an electron from the latched metastable state [5]. The effect of thermal excitation is one of the possible sources of such error, however for the case $E_B >> kT$ (where E_B is the Coulomb barrier formed by MTJ) the probability of this error becomes very small and can be neglected in our case for temperatures below 200 mK. Let us consider the "decays" caused by the higher-order tunneling processes [12] which dramatically reduce the lifetime of an electron in a trap even at 0 K. The use of MTJ exponentially increases the retention time, τ. (We need to stress that the use of MTJ, required for prototypes operating at low frequencies, will not be required for high speed applications at a clock rate $T_{CLK} \sim 1$ ns). A theoretical estimate for kT=0 [12] gives for a QCA latch with two single junctions (R_J =100 kΩ ; C_J =0.3 fF) $\tau \sim 5$ ns, whereas for a latch with two MTJs consisting of three such junctions calculation gives $\tau \sim 3000$ s. Our preliminary measurements of the temperature dependence of the escape rate $\Gamma = 1/\tau$ found it to be a weak function of temperature below 200 mK: $\Gamma \sim kT^{\alpha}$, where $\alpha \sim 2$, which is a characteristic feature of electron transport caused by cotunneling [13]. For temperatures higher than ~250 mK the temperature dependence of Γ changes its character and becomes exponential. This means that first-order processes become dominant and our device cannot anymore act as a latch. The decay error probability is given by :

$$P_{DEC} = 1 - \exp(-t/\tau), \qquad (2)$$

which for $t << \tau$ is reduced to $P_{DEC} \approx t/\tau$. To find τ we apply batches of clock pulses (N_s= 1000) with different length to the latch and then measure the interval of time from the application of the clock signal to the first escape from the latched state. We should note that for reliable measurements of τ, the acquisition time should be of the order of 1-2 τ. In the case of large τ the measurement time becomes comparable with typical drift time $\tau \sim \tau_d$, which distorts the result of the measurement. We estimate the lower bound of the average lifetime of an electron in a latched state for our devices at T~70 mK to be greater than 100 sec. For the clock pulse length T_{CLK} ~200 ms (see Fig. 4) (2) gives the decay error probability to be about 0.002 by the end of clock pulse and remains below $2 * 10^{-4}$ for t = 20 ms clock hold time. Experimentally, T_{CLK} ~200 ms corresponds to a single decay for a batch of 500 pulses. This number of decays does not give us a reliable statistics but is in reasonable agreement with experiment. For a higher clock rate (say, 100 MHz) the probability of decay errors falls below $\sim 10^{-10}$.

5.3 Errors in a QCA shift register

As we show above (Fig. 5) the probability of switching error for a QCA latch exponentially depends upon the applied input signal, and can be reduced by increasing the input signal ΔV_{IN}. In a shift register, however, the input signal for the second latch is fixed at a potential difference produced by the first latch, ΔV_{L1}. The switching error rate for a second latch itself is therefore also fixed at the level defined by ΔV_{L1} and coupling capacitance C_C. The error probability for a shift register is defined by the errors, produced by first P_1 and second latch P_2:

$$P = P_1 + P_2(1-P_1) \qquad (3)$$

We measured the probabilities of the switching error in the shift register and found that it follows (3). The switching error probability produced by a second latch is found to be constant $P_{SW.THERM} \sim 0.03$ and independent of the input bias (applied to a first latch). For the decay errors in the shift register the probability is also given by (3),

however in the current experimental setup the probability of the decays remains within noise margins.

5. Summary

Using Al tunnel junction technology we experimentally demonstrated the operation of two QCA clocked logic devices, the QCA latch and QCA shift register, at low temperature. We study the error rate in these devices and found good latching parameters, corresponding to a small decay rate. We found an exponential dependence of the switching error rate on the input signal, but did not observe expected temperature dependence. The source of this discrepancy is currently being investigated.

Though current QCA prototypes operate at the low temperature of 70 mK, the future generations of the QCA devices are expected to work at liquid nitrogen (metal nanoclusters QCA) or even room temperatures (molecular QCA), at much higher speeds, and lower levels of errors.

6. Acknowledgements

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