Carbon Nanotubes for Quantum-Dot Cellular Automata Clocking

Sarah E. Frost†, Timothy J. Dysart†, Peter M. Kogge† and Craig S. Lent‡
† Dept. of Computer Science and Engineering
‡ Dept. of Electrical Engineering
University of Notre Dame
Notre Dame, IN 46556, USA
Email: {sfrost,tdysart,kogge,lent}@nd.edu

Abstract **Quantum-dot cellular automata (QCA) is a computing model that has shown great promise for ef£cient molecular computing. The QCA clock signal consists of an electric £eld being raised and lowered. The wires needed to generate the clocking £eld have been thought to be the limiting factor in the density of QCA circuits. This paper explores the feasibility of using single walled carbon nanotubes (SWNTs) to implement the clocking £elds, effectively removing the clocking wire barrier to greater circuit densities.**

I. Introduction

Quantum-dot cellular automata (QCA) is a computing model that uses charge con£guration to represent and transport data, exploiting the characteristics of the nanoscale world [1], [2]. Carbon nanotubes (CNTs) have been demonstrated to be powerful tools for the nanoscale. In particular, the electrical properties of metallic single wall nanotubes (SWNTs) have been shown to be excellent conductors [3]. This paper explores the feasibility of using metallic SWNTs to implement the QCA clocking scheme.

The basic computing device of QCA is a square cell with a quantum dot at each corner. Two excess electrons are introduced into each cell. Due to Coulombic repulsion, the two electrons repel each other to antipodal corners of the cell, resulting in two stable cell polarizations, $P = +1$ and $P = -1$, corresponding respectively to a logical one and zero. Several cells can be placed in a row to create the QCA "wire". Cells tend to assume the same polarization as their neighbors due to Coulombic interaction between them. Additionally, a functionally complete set of logic gates can be created with the majority gate and inverter [4].

To move data across the circuit, a four phase "clock" is used. The clocking signal is an electric £eld that is raised and lowered to control the tunneling within the cells [4]–[6]. A complete clock cycle brings the £eld for each cell includes high, falling, low, and rising £eld strengths. An array of cells controlled by the same £eld phase is referred to as residing in the same clock zone. A QCA cell in a high £eld has a de£nite con£guration and can drive other neighboring cells into its con£guration, passing along its data to them. Cells in a rising zone can assume a con£guration from a neighbor driver cell. The clocking phase layout needed to move a bit in a wire from left to right is shown in Fig. 1. It is important to note that unlike traditional circuits in which the clock is like any other signal, the QCA clock is a different kind of phenomenon than the values being carried by the QCA cells.

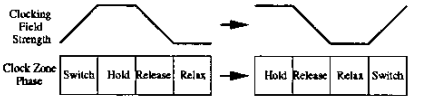

Fig. 1. The four phases of the QCA clock (hold, switch, relax, release) and the transition of phase in order to move a bit in a wire left to right.

The QCA theory has been veri£ed through experimentation using metal-dot cells [7]–[9]. The great promise of QCA, though, lies in a molecular implementation [10], [11] which will allow room temperature circuit operation. Current work includes the construction and investigation of candidate molecules [12]–[14], the clocking of these molecules [2], and the self-assembly of circuits using these molecules [15]. Concurrent with the device work, architectures have been explored to exploit the unique device characteristics of QCA and to demonstrate that QCA can be used for ef£cient computing [4], [16]–[18]. The architecture work has demonstrated the potential of QCA for densely implementing general purpose computing.

The purpose of this work is to examine the feasibility of using carbon nanotubes to implement QCA clocking and examine the effects of the clocking wire layout on circuit designs and architectures. To do this, the carbon nanotube properties assumed are brie¤y discussed, followed by a discussion of clocking wire density. Next, examples of two clocking wire layout strategies are discussed along with their impact on a sample memory architecture.

II. Carbon Nanotubes

This work uses the frequently studied (10,10) SWNTs. With a diameter of ~1.4nm and lengths up to several hundreds of microns, these metallic nanotubes are on the

0-7803-8536-5/04/$20.00 ©2004 IEEE

same size scale as proposed QCA molecules. The role of these nanotubes is to generate the clocking £elds required by QCA circuits. The molecule being considered is a two-dot QCA cell with a cell-cell distance of 1.4 nm [14]. The associated cell-to-cell distance of the four dot cells built from these 2 dot cells is 2.8 nm (Fig. 2).

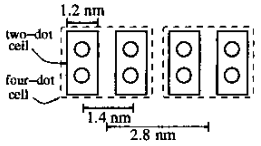

Fig. 2. Cell to cell distance of a four dot QCA cell built from two 2-dot molecules.

III. Clocking Wire Density

The layout and density of QCA circuits depends signi£cantly on the underlying clocking wire layout. The clocking wires create the ¤oor plan for which the QCA circuits will be designed. The linear density of the clocking wires ($wires/\mu m$) can be calculated by $clockDens = 1/max(wirePitch, CCdist)$ where $wirePitch$ is the minimum distance between adjacent wires and $CCdist$ refers to the cell to cell distance, or minimum spacing between adjacent 4-dot QCA cells.

Using atomic force microscopes (AFMs), nanotubes can be placed precisely, leading to a wire pitch of approximately two SWNT diameters, or 2.8 nm. The end of the ITRS roadmap, 2016, calls for a metal 1 pitch of 54 nm. Using the $clockDens$ equation discussed above, these metal clocking wires have a linear density of 18.52 $wires/\mu m$. Assuming the two-dot molecule discussed above with a cell-to-cell distance of 2.8 nm for the full four-dot cell and SWNTs for the clocking wires, the clocking wire density is 35.7 $wires/\mu m$. This is a linear density increase of 19.29 times, implying potential overall density gains of roughly 372 times over end of the roadmap metal wires.

IV. Clocking Wire Layout

To implement useful computing, QCA circuits require data to ¤ow in two basic ways, as a straight wire and as a turning wire. In this section, two £rst cut implementation strategies of the clocking wire layout are discussed. These are £rst cut designs that demonstrate the feasibility of this scheme.

The £rst strategy, proposed by Blair [19], is to lay down a series of clocking wires perpendicular to the direction of the QCA signal (Fig. 3 a). When placed at the correct distance, these wires can generate a clocking £eld that will smoothly propagate the QCA signals. This approach requires the clocking wires to assume a range of orientations to support turns in the wires (Fig. 3 b).

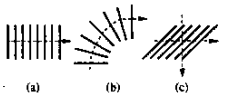

Fig. 3. Three clocking wire layouts: (a) Straight QCA signal traveling perpendicular to the clocking wires. (b) QCA turn with perpendicular wires. (c) QCA signal traveling at 45 degree angle to clocking wires.

The second approach places the clocking wires at a 45 degree angle to the direction of the QCA signal (Fig. 3 c). This allows the QCA signal to travel along two axes for any given set of clocking wires and requires only two clocking wire orientations, perpendicular to each other, to implement a full QCA circuit.

V. Effect on Architecture

The H-memory is a memory architecture designed to take advantage of the characteristics of QCA [17], [18]. The memory cell is a wire spiraled into itself that stores a word of data. Since the H-memory was designed to exploit QCA, it is a valuable circuit on which to demonstrate the potential of the nanotube clocking schemes.

There are several ways to layout the spiraled memory cell, including the ¤attened spiral, the expanded spiral and the snake con£gurations (Fig. 4). The ef£ciency of each con£guration implemented with the two clocking schemes discussed above is compared by two metrics. $Bits/area$ measures the density of the resulting circuit. $Bits/wire$ measures the ef£ciency of each clocking wire and is an indirect measure of the manufacturability of the clocking circuitry.

Fig. 4. Three spiral con£gurations for storing multiple bits: (a) a ¤attened spiral, (b) an expanded spiral, and (c) a snake con£guration. The shading indicates the clocking zones of each QCA cell.

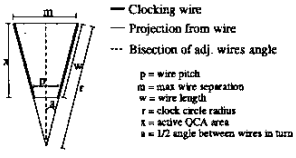

Fig. 5. Parameters used to calculate clocking wire density on a turn for the perpendicular clocking wire layout.

TABLE I

EQUATIONS FOR TWO CLOCKING SCHEMES

Layout type	bits/area	Number Wires
P spiral	$\frac{n}{4\alpha r^2}$	$\frac{\pi}{\alpha}$
P ¤at spiral	$\frac{n}{4\alpha r^2} + \frac{w}{4prQ}$	$\frac{\pi}{\alpha} + \frac{l}{p}$
P snake	$s(\frac{1}{4\alpha r^2} + \frac{1}{4pr})$	$s(\frac{\pi}{\alpha} + \frac{l}{p})$
Diag spiral	$1/32p^2$	$32n$
Diag ¤at	$1/32p^2$	$32n + 2(\frac{l}{p} + 4n)$
Diag snake	$1/32p^2$	$s(32 + 2(\frac{l}{p} + 4)$

The $bits/area$ calculation for the perpendicularly placed wires depends on a number of factors, including the wire pitch, the maximum distance between wires to continue to smoothly propagate the overlying QCA signals, and the number of wires per clocking circle (Fig. 5). To compare the spiral and clocking wire con£gurations, samples of the density and ef£ciency of the circuits were calculated using the equations in the table and assuming a pitch of $2.8nm$, a max separation of $14nm$, and an elongated side of $168nm$ for the ¤attened spiral and snake con£gurations, and 16 wires per full circle for the perpendicular wire turns.

The most least ef£cient con£guration was the perpendicular spiral with only $776bits/\mu m^2$. It also had low wire reuse, only $4bits/wire$. The perpendicular snake con£guration made excellent use of space, with a density of $9223bits/\mu m^2$. However, it does not reuse any wires, resulting in $0.25bits/wire$. The diagonal layout all had achieved the same density of $3990bits/\mu m^2$. The best wire usage was $32bits/wire$ for the spiral.

Wire reuse increases the ef£ciency and manufacturability of the clocking layouts. The snake con£gurations have low turn costs in terms of area but require a large number of short wires, making them less attractive for mass fabrication. The diagonal strategy pays a minor density penalty compared to the perpendicular clocking scheme, but it uses wires substantially more ef£ciently, making this a strategy worthy of further study.

VI. FUTURE WORK AND CONCLUSION

Previously, QCA has been shown to offer great gains in density over end of the road transistor based electronics [16], [20], [21]. The clocking wires needed to generate the clocking £elds, though, were thought to be a density limiting factor. This paper has presented the use of SWNTs to implement the clocking £elds and has demonstrated that the clocking wires may be removed from the density equation. In addition, we have presented a new clocking wire layout strategy that supports high density circuits and simpli£es fabrication requirements.

This work was supported in part by the University of Notre Dame, in part by the National Science Foundation under grant CCR-0210153, and in part by SRC under grant ID 2000HJ836.

REFERENCES

[1] C. Lent, P. Tougaw, and W. Porod, "Quantum Cellular Automata," *Nanotechnology*, vol. 4, no. 49, 1993.

[2] C. S. Lent and B. Isaksen, "Clocked molecular quantum-dot cellular automata," *IEEE Trans. on Electron Dev.*, vol. 50, no. 9, pp. 1890–1895, Sept 2003.

[3] *Carbon Nanotubes: Synthesis, Structure, Properties, and Applications*. Springer-Verlag, 2001.

[4] C. S. Lent and P. D. Tougaw, "A device architecture for computing with quantum dots," *Proceedings of the IEEE*, vol. 85, no. 4, pp. 541–557, Apr. 1997.

[5] G. Toth and C. S. Lent, "Quasiadiabatic switching for metal-island quantum-dot cellular automata," *J. Appl. Phys.*, vol. 85, no. 5, pp. 2977–2984, Mar. 1999.

[6] K. Hennessy and C. S. Lent, "Clocking of molecular quantum-dot cellular automata," *J. Vac. Sci. Technol. B*, vol. 19, no. 5, pp. 1752–1755, Sept./Oct. 2001.

[7] I. Amlani *et al.*, "Digital logic gate using quantum-dot cellular automata," *Science*, vol. 284, pp. 289–291, April 1999.

[8] A. O. Orlov *et al.*, "Clocked quantum-dot cellular automata shift register," *Surface Science*, vol. 532-535, pp. 1193–1198, June 2003.

[9] R. K. Kummamuru *et al.*, "Operation of a quantum-dot cellular automata (qca) shift register and analysis of errors," *IEEE Trans. on Electron Dev.*, vol. 50, no. 9, pp. 1906–1913, September 2003.

[10] M. Lieberman *et al.*, "Quantum-dot cellular automata at a molecular scale," *Ann. N.Y. Acad. Sci.*, vol. 960, pp. 225–239, 2002.

[11] C. S. Lent, B. Isaksen, and M. Lieberman, "Molecular quantum-dot cellular automata," *J. Am. Chem. Soc.*, vol. 125, no. 4, pp. 1056–1063, 2003.

[12] Z. Li and T. P. Fehlner, "Molecular qca cells. 2. characterization of an unsymmetrical dinuclear mixed-valence complex bound to a au surface by an organic linker," *Inorganic Chemistry*, vol. 42, pp. 5715–5721, 2003.

[13] J. Jiao *et al.*, "Building blocks for the molecular expression of quantum cellular automata. isolation and characterization of a covalently bonded square array of two ferrocenium and two ferrocene complexes," *J. Am. Chem. Soc.*, vol. 125, pp. 7522–7523, 2003.

[14] H. Qi *et al.*, "Molecular quantum cellular automata cells. electric £eld driven switching of a silicon surface bound array of vertically oriented two-dot molecular quantum cellular automata," *J. Am. Chem. Soc.*, vol. 125, pp. 15 250–15 259, 2003.

[15] Q. Hang *et al.*, "Molecular patterning through high-resolution polymethylmethacrylate masks," *Appl. Phys. Lett.*, vol. 80, no. 22, pp. 4220–4222, June 2002.

[16] M. T. Niemier, M. J. Kontz, and P. M. Kogge, "A design of and design tools for a novel quantum dot based microprocessor," in *27th Ann. Design Automation Conference*, June 2000, pp. 227–232.

[17] S. E. Frost *et al.*, "Memory in motion: A study of storage structures in qca," in *1st Workshop on Non-Silicon Computing (NSC-1) held in conjunction with HPCA-8*, Boston, MS, USA, Feb. 2002.

[18] S. Frost *et al.*, "Bouncing threads: Merging a new execution model into a nanotechnology memory," in *IEEE Annual Symp. on VLSI*, Feb 20-21 2003.

[19] E. Blair, "Tools for the design and simulation of clocked molecular quantum-dot cellular automata circuits," Master's thesis, Univ. of Notre Dame, Dept. of Electrical Engineering, November 2003.

[20] M. T. Niemier and P. M. Kogge, "Exploring and exploiting wire-level pipelining in emerging technologies," in *28th Ann. Int. Symp. on Comp. Arch.*, Goteborg, Sweeden, July 2001, pp. 166–177.

[21] M. T. Niemier and P. M. Kogge, "Problems in designing with QCAs: Layout = timing," *Int. J. of Circ. Theory and App.*, vol. 29, pp. 49–62, April 2001.