A two-stage shift register for clocked Quantum-dot Cellular Automata

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Quantum-Dot Cellular Automata (QCA) is a computational scheme utilizing the position of interacting single electrons within arrays of quantum dots ("cells") to encode and process binary information. Clocked QCA architectures can provide power gain, logic level restoration and memory features. Using arrays of micron-sized metal dots, we experimentally demonstrate operation of a QCA latch-inverter and a two-stage shift register.

As the microelectronics industry approaches to the limits imposed by the laws of nature in shrinking down the size of the "work-horse" of modern electronics, the field-effect transistors (FETs), the search for an alternative computational paradigm becomes vital. As FETs become smaller, effects such as sub-threshold and gate leakage (to name a few) and increasing device density lead to intolerable levels of power dissipation: the power dissipation per square area of a Pentium-4 chip is comparable to that of a home electric range-top unit. It is therefore necessary in the search for a new computational paradigm to look at schemes with minimal achievable power dissipation. Attempts to minimize energy dissipation in implementing binary functions have a long history. Keyes and Landauer [1] described one such scheme credited to von Neumann in the 1950s. It is designed to use in systems which, under external control, can be taken continuously from a monostable state into a bistable state and back to monostability (MBM) in a cyclic fashion. Authors of [1] considered a particle in a time-varying potential well to represent binary "0" and binary "1" by the position of the particle in one of the wells (Fig. 1). The sequence of events in Fig.1 is SWITCH-HOLD-RESTORE. Here during the SWITCH phase the system is transformed from a monostable to a bistable state, where the particular binary state is chosen by the external input, so that the information is stored in the system. During the HOLD stage the information is preserved and the particle in the well acts as an input for the subsequent stage (e.g., by means of Coulomb interaction). Finally, during the RESTORE part of the cycle the well returns to its initial monostable state. Since binary logic operations are performed by manipulation of the spatial configurations of single particles, which do not involve significant current flows, the power dissipation in such system is greatly reduced compared to conventional, FET-based logic. By changing the barrier slowly compared to the characteristic settle-down time of the system (quasiadiabatically), the energy dissipated in the process can be further reduced and thus the goal of minimal energy dissipation can be achieved.

Theoretical calculations suggesting the use of MBM devices to implement logic functions with single electrons were performed in [2,3]. Lent et al. [4] developed a complete set of binary transformations to implement basic logic functions using geometrically arranged quantum wells (quantum dot cells) with each cell being composed of four quantum dots arranged in the corners of a square and charged with two extra electrons. Single electrons within the cells are used to encode binary information in this paradigm known as Quantum-dot Cellular Automata (QCA). Control over the barriers (clocking) for QCA [3] provides the means for implementing the device described in [1], with a system where the barriers separating the dots in the cell can be varied by external voltage. For example, in semiconductor dot implementations clocking can be performed by a common back gate controlling an array of QCA cells. A scheme to provide the MBM function in systems with fixed barriers separating the dots was proposed in [2]. In recent publications these ideas were further developed for metal tunnel junction systems [5, 6]. In accordance with [1] the input signal only defines the direction of switching (by creating asymmetry in the wells), while the clock signal performs the actual electron transfer (by changing the potential profile in the system from monostable to bistable). Clocking also provides the means for short-term information storage (HOLD) so that a cell remains polarized even in the absence of the input signal. Recently, power gain in clocked QCA needed for the restoration of logic levels in nanodevices was theoretically demonstrated [7]. The QCA architecture also provides the means for quasiadiabatic switching and thus leads to extremely low power dissipation in arrays of cells by using clock signals slower than the tunneling times between dots. This is particularly important for future molecular implementations of QCAs, where theoretical calculations show an expected capacitance of approximately 0.1 aF, with switching times of approximately 1 picosecond. By implementing QCA in molecules, room-temperature operation could be achieved. In early experiments a QCA cell, small binary wire, and digital logic gate, have been demonstrated [8]. However, these devices repre-

sented a family of edge-driven QCA devices, where the only source of energy was the signal input. Recently, a basic unit realizing the MBM switching scheme in metal-dot QCA was demonstrated [9].

In this paper we present an experimental demonstration of a new functional QCA device implemented in metal dots working in accordance with MBM scheme - a two-stage shift register.

To fabricate a prototype metal-dot QCA we use aluminum tunnel junction technology which combines electron beam lithography (EBL) with a suspended mask technique [10]. In this method, thin-film aluminum dots separated by tunnel junctions are produced. The advantage of this technology is its relative simplicity (only 3 processing steps: direct EBL writing, development, and metal deposition with *in situ* oxidation), good uniformity (junction resistance in one run typically varies by only 20-30% compared to orders of magnitude difference in today's semiconductor-dot implementations), and high yield (up to 100%). The small charging energy ($E_C = e^2/2C$) of the aluminum "dots" (< 1 meV), due to relatively large junction capacitances, limits the operating temperature to below 1 K. To satisfy the condition $E_C >> kT$ the experiments are performed in a dilution refrigerator at the temperatures 50-200 mK. We use the lock-in technique to measure conductance of single-electron transistors (SET) acting as electrometers. To suppress the superconductivity of aluminum, a magnetic field of 1 T is applied to the device.

The simplified circuit diagram of the device is shown in Fig. 2A, with an SEM micrograph shown in Fig. 2B. The device consists of two QCA latches [9] (delineated by a dashed line in Fig.2A) and two readout electrometers E1 and E2. The two latches are capacitively coupled to each other using lateral capacitors C4 and C6. Each QCA latch consists of three micron-size Al "dots" D1-D3, and D4-D6, separated by multiple tunnel junctions (MTJ). The area of each junction is about 50 by 50 nm, and the thickness of the Al oxide is about 2 nm.

Three gates are used to control the charge state of the device. SET electrometers E1 and E2 capacitively coupled to dots D1 and D4 are used to measure the state of the latch. The MTJ design is used to suppress second-order tunneling processes [11] which can result in the loss of information during the hold time (for detailed discussion on this subject, see [9]).

The operation of a QCA shift register consists of several time phases. In phase 1 latch L1 is switched from a monostable to a bistable state while L2 is kept in a monostable state. This is achieved by applying a small signal to the inputs of L1 to define the direction of the switching with a subsequent application of the 1st clock signal, V_{CLK1}, to the gate of D2 which accomplishes the electron transfer and establishes the bistability by changing interdot barrier. Once the transfer of an electron is achieved, the input can be removed and L1 remains in a HOLD state where it acts as the input signal for L2. A QCA latch can be viewed as an inverter, since the output signal it provides to a subsequent QCA element is the inverse of the input. In a second time phase, L2 is activated by application of the second clock signal, V_{CLK2}, applied to the gate of D5. With V_{CLK2} applied, L2 becomes bistable and switches into the state opposite (inverted) to the state of L1. An interesting feature of this design is that either latch can be used as an input to the other, providing means for bidirectional computation.

Figure 3 demonstrates the operation of latch L1 with L2 in a monostable (inactive) state. As the pulse V_{IN} is applied to the input gates (logical "0" at t_1 , and logical "1" at t_5) no charge transfer happens (and the latch remains neutral) until the clock signal is applied (at t_2 , t_6). Application of the clock signal transfers an electron from D2 to D3 (at t_2) or D1 (at t_6), in accordance with the polarity of the input signal. The input can then be removed (at t_3 , t_7). The electron remains latched (HOLD) in the dot, providing a source of signal for the next latch until the clock signal is set to low (at t_4 , t_8). It is clear from Fig. 3 that the QCA latch operates in accordance with expectations.

Operation of the QCA shift register is performed using a two-phase clock (CLK1 and CLK2). The differential signal V_{IN} corresponding to logical "0" (logical "1") is, as before, applied to the inputs V_{IN}^{+}, and V_{IN}^{-} at t_1 (t_7) (Fig. 4). Again, L1 remains in the monostable state until CLK1 is set "high" at t_2 (t_8) in Fig. 4. When clock CLK1 is set high, L1 becomes active. Once L1 is set (an electron is locked on one of the end dots), the signal input is removed at t_3 (t_9) and the state of L1 no longer depends on the input signal. Then the second clock CLK2 is applied to L2 at t_4 (t_{10}) in Fig. 4, and an electron in L2 switches in the direction determined by the state of the first latch. The second latch holds the bit after CLK1 is removed at t_5 (t_{11}) in Fig. 4 for as long as CLK2 is high (until t_6 (t_{12})). The cycle describing the operation of a QCA shift register is as follows: monostable $\rightarrow$ input applied $\rightarrow$ first clock applied and first latch is active $\rightarrow$ input removed $\rightarrow$ second clock applied and second latch is active $\rightarrow$ first clock is removed. At this time the first latch becomes neutral and is ready to receive new information. The information encoded in the position of a single electron is shifted to the second latch and stored there. We can see that the QCA shift register indeed operates in a way predicted in [1,9]. Thus, the operation of a functioning QCA shift register is demonstrated.

One of the vital parameters which determine the fate of any binary logic device is the speed of switching for binary operations. The operational speed of the latch is determined primarily by the tunneling time of the electron ($\tau \sim R_J C_J \sim 10^{-10}$ sec, where $R_J \sim 10^6$ Ω, and $C_J \sim 10^{-16}$ F are the resistance and the capacitance of the junction). To perform the switching quasiadiabatically the switching speed needs to be reduced by approximately one order of magnitude, thus for our current Al/AlOx prototype the estimate for the switching "speed limit" is of the order of 1 ns. For the future molecular implementations due to much lower capacitance ($C \sim 10^{-19}$ F) the expected switching speed is of the order of picoseconds.

The clock speed in our current experiment is limited by the experimental setup: it is set by parasitic RCs in the electrometer circuits. As a result, the temporal resolution of the

SET readout is of the order of 1 ms. With the use of an RF-SET [12] the temporal resolution of the Al-SET electrometer is expected to be in nanosecond range.

The ultimate utility of a shift register would be in large-scale QCA circuits, to control the flow of binary information through the circuit. Hence the performance of a multi-stage shift register, especially with regard to preservation of logic levels and propagation of errors, is of considerable interest. The current device can be used to replicate the propagation of a single bit through such a shift register. In a multi-stage shift register, a bit is first written into the circuit by the input and then moved along the circuit using each latch as an input to the next (Fig. 5A). The same situation can be simulated using the two-stage shift register by moving the bit back and forth from one latch to the other (Fig. 5B). Initially, a bit is written into the first latch by the input. Then using L1 as input, the bit is copied into L2 after which L1 is turned off. Then using L2 as input, the bit is copied back into L1, and L2 is turned off. This process can be repeated a number of times to achieve the same effect as transferring a bit through a long line of latches.

Figure 6 shows the timing diagram of the experiment performed for 5 cycles. Initially, all the signals are zero and the two latches are in the neutral state. Once the input (binary "1") and clock signals are applied to L1, it switches. The input is then removed and the bit is stored in L1. The clock signal is then applied to L2, and it switches using L1 as its input. L1 is then switched off, and the bit is now stored in L2. Instead of applying the clock signal to a third latch in the line, it is applied to L1 which sees L2 as an input and switches accordingly. Then L2 is switched off and the bit is stored once again in L1. This cycle is repeated 5 times to simulate a shift register made of 11 latches. In the second half of the experiment, this scheme is repeated with an input of the opposite sign (binary "0"). This is necessary to verify that bit inversion at the input leads to the bit inversion at the output. The above experiment demonstrates that the direction of flow of information in the circuit is controlled by the sequence of

clock signals applied to latches. Another observation that can be made from Fig. 6 is that, although the input is applied only once at the beginning of the cycle, we do not see any degradation in the voltage levels as the bit is moved back and forth between the latches indicating that signal levels would be preserved in multi-stage QCA shift registers. The major reason for this stems from the ability of clocked QCA to exhibit power gain which has been recently demonstrated theoretically [7] and experimentally [13]. The clock signal here provides the energy needed for power restoration just as a conventional power supply does it for FET logic.

What limits the number of "back and forth" switching operations that can be reliably performed in a shift register? The output latch-to-latch signal (produced by a switching electron) which acts as an input to the other latch, is set by a coupling parameter between latches. The probability of a "switching error" in a latch [5] is reduced exponentially with the increase of the input signal. Therefore, for a given coupling between latches (and thus a fixed latch-to-latch input signal) the number of "back and forth" switching operations is set by the electrical and thermal noise in the system. For a current shift register implementation the magnitude of the latch-to-latch input signal is only marginally larger than the combined noise. As a result the probability of error-free operation of 11 stage shift register is only about 0.3. However, as the size of the QCA elements gets smaller (and corresponding charging energy is higher) the probability of the switching error drops down exponentially, thus ensuring reliable operation of a multi stage shift registers.

To conclude, we experimentally demonstrate the operation of a QCA two-stage shift register working at a temperature of 70 mK. Though the current prototype operates only at low temperatures, future generations of the QCAs and other devices based on the algorithm described in [1] are expected to work at liquid nitrogen (metal nanoclusters QCA) and at room temperature (molecular QCA), at much higher speeds.

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Figure Captions

Figure 1: Three states of the system [1] : (1) SWITCH (2) HOLD (3) RESTORE

Figure 2: (a) Schematic Diagram of a QCA shift register. (b) SEM micrograph of the device.

Figure 3: Operation of a QCA latch. A small input signal defines the direction of switching in the latch, while the clock signal triggers the switching. The latch retains the bit as long as the clock is applied. Five successive traces are shown to delineate the noise margins.

Figure 4: Operation of a shift register. Phase-shifted clock signals are applied to two capacitively coupled latches to shift binary information from one latch to the next in a sequential manner controlled by the clock. Five successive traces are shown.

Figure 5: Using a two-stage shift register to simulate a multi-stage shift register. (a) In a multi-stage shift register, a bit is moved sequentially in a single direction from one latch to the next. The bit is inverted at each step. (b) The two-stage shift register can be used to simulate a longer shift register by moving the bit back and forth from one latch to the other instead of moving it in a single direction.

Figure 6: Experiment to simulate a multiple stage shift register. The input is applied only at the beginning, to write a bit into the shift register. Then the bit is transferred from one latch to the other for five cycles. In the second half of the experiment, the sequence of events is repeated with an input of the reverse polarity. This experiment can be used to investigate the propagation of errors in a multi-stage shift register.

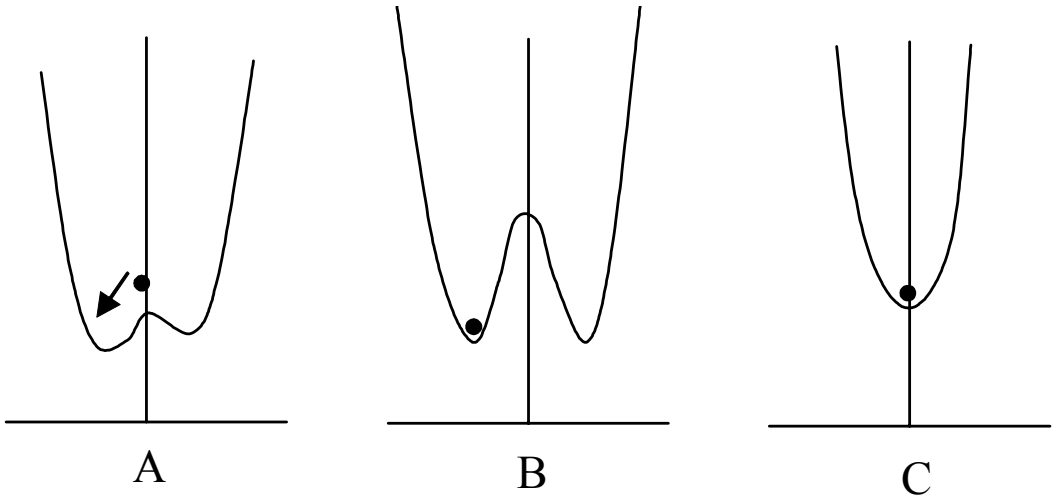

Figure 1.

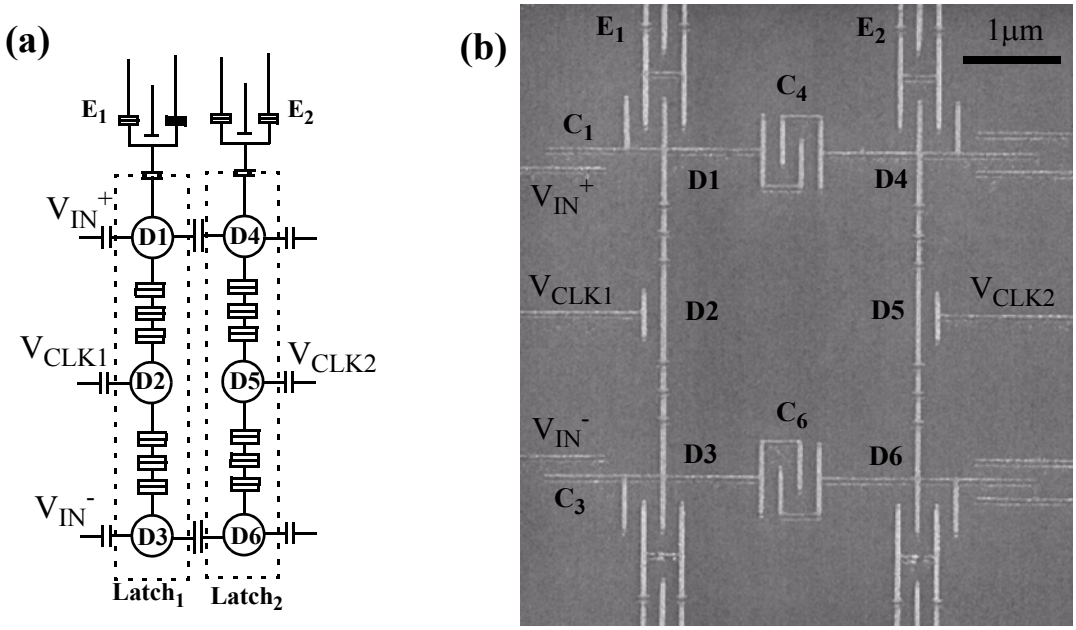

Figure 2.

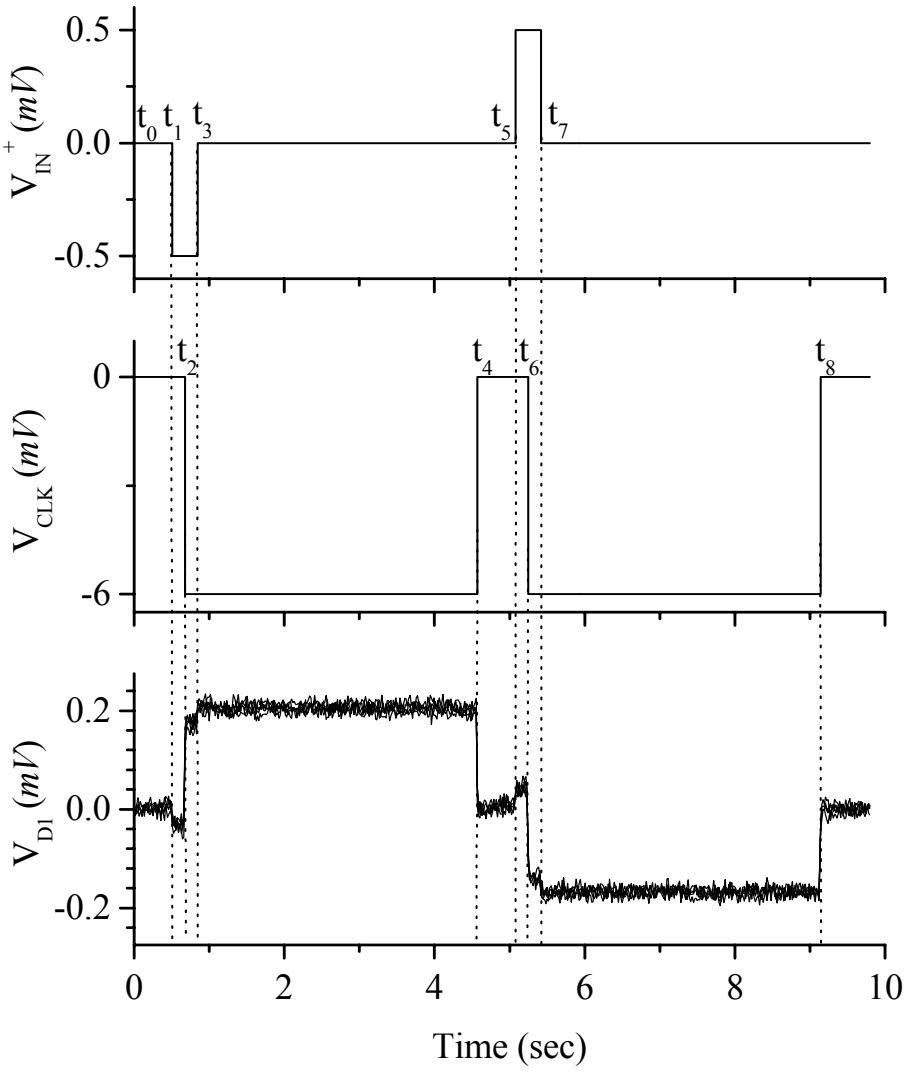
0.5
0.0
-0.5
V_{IN}^{+} (mV)
t_0 t_1 t_3
t_5 t_7
0
-6
V_{CLK} (mV)
t_2
t_4 t_6
t_8
0.2
0.0
-0.2
V_{D1} (mV)
0
2
4
6
8
10
Time (sec)

Figure 3.

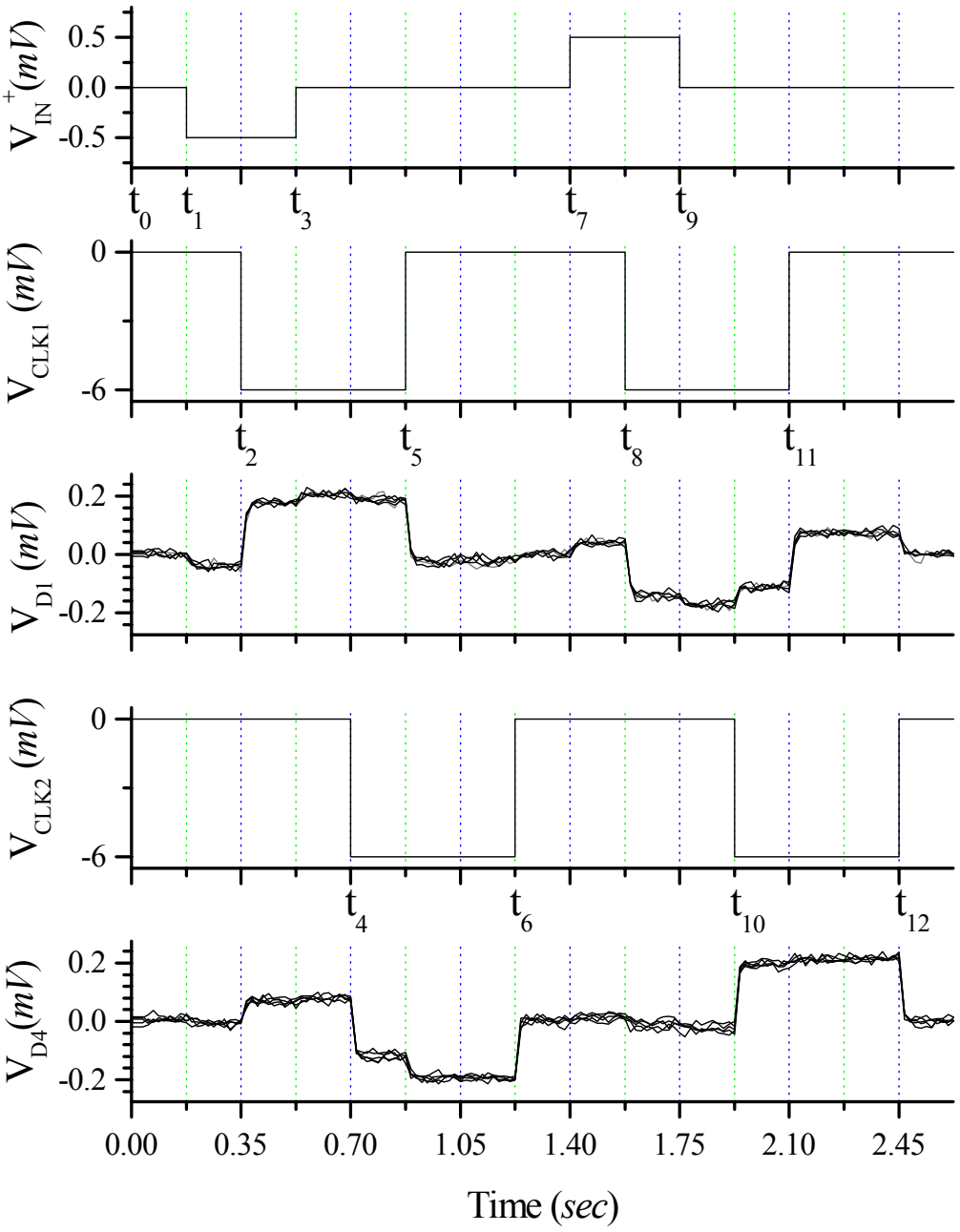
0.5
0.0
-0.5
$V_{IN}^{+}(mV)$
t_0 t_1 t_3 t_7 t_9
0
-6
V_{CLK1} (mV)
t_2 t_5 t_8 t_{11}
0.2
0.0
-0.2
V_{D1} (mV)
0
-6
V_{CLK2} (mV)
t_4 t_6 t_{10} t_{12}
0.2
0.0
-0.2
$V_{D4}(mV)$
0.00 0.35 0.70 1.05 1.40 1.75 2.10 2.45
Time (*sec*)

Figure 4.

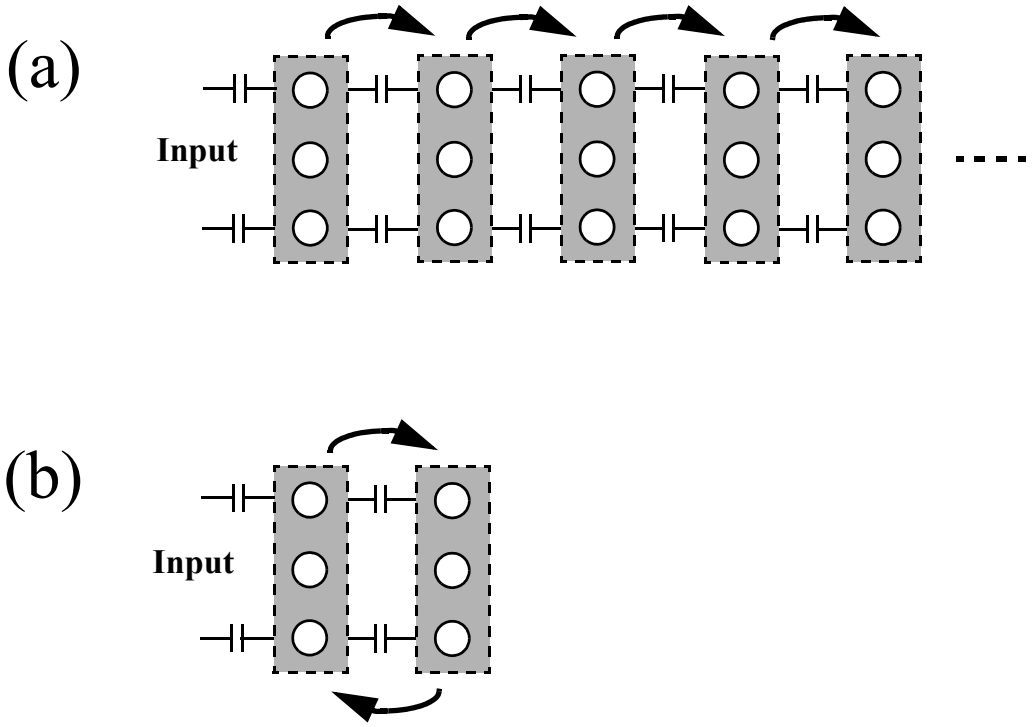

Figure 5.

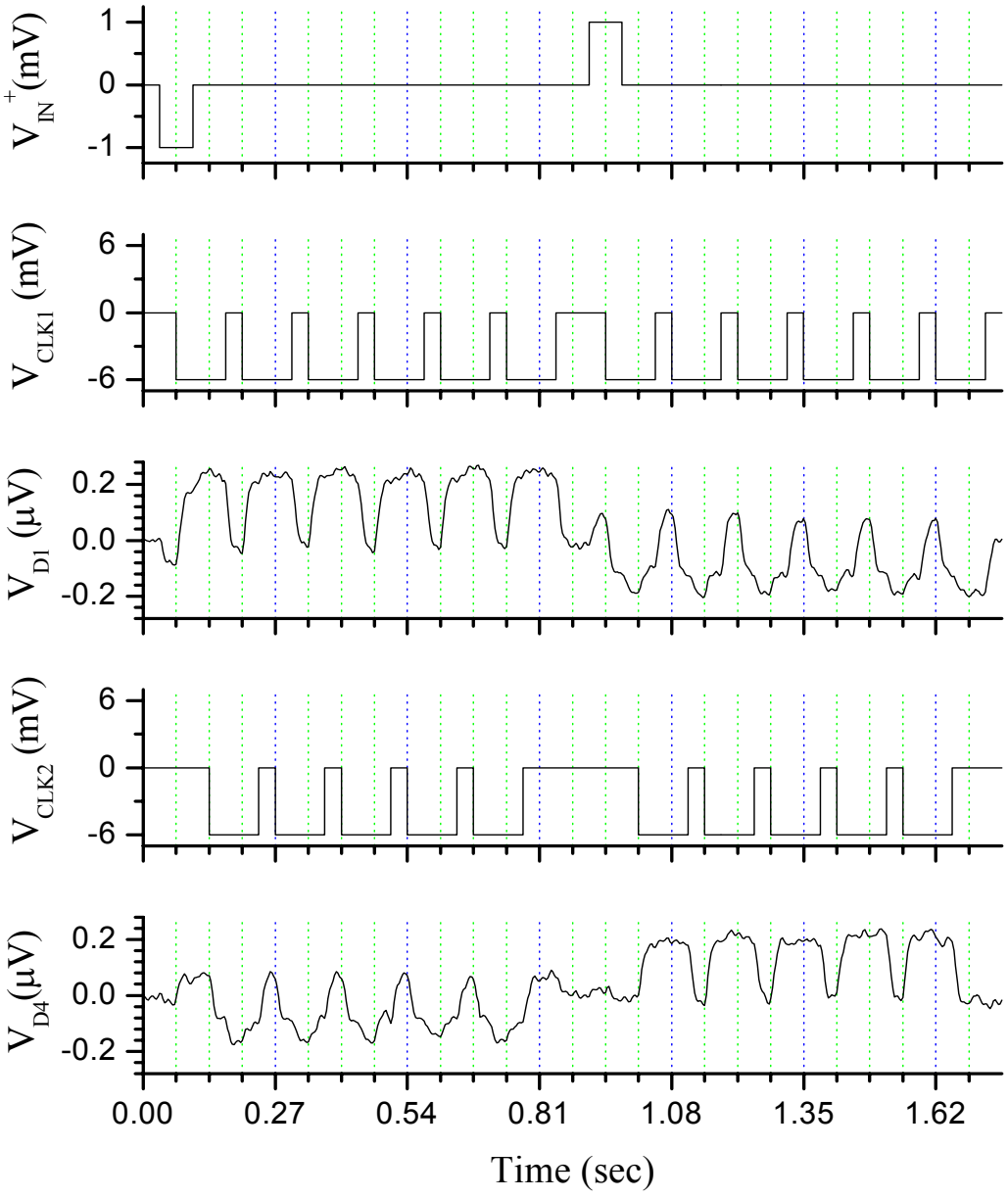
V_{IN}^{+}(mV)
1
0
-1
V_{CLK1} (mV)
6
0
-6
V_{D1} (μV)
0.2
0.0
-0.2
V_{CLK2} (mV)
6
0
-6
V_{D4}(μV)
0.2
0.0
-0.2
0.00
0.27
0.54
0.81
1.08
1.35
1.62
Time (sec)

Figure 6.