

# Fluidic-Based Ion Memristors and Ionic Latches

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Micro/nanofluidic circuitry and organic bioelectronics allow precise control of ion and biomolecule transport in high-ionic strength physiological buffers.<sup>[1–6]</sup> Active ionic circuit elements that are analogs of basic electronic logic devices such as ionic transistors and passive ionic circuit elements like nonlinear ionic resistors that exhibit inflection points and transient hysteresis in the current–voltage relationship have been reported.<sup>[1,2,7–9]</sup> The charge carriers in these ionic logic devices are represented by ions and charged molecules in aqueous environment, instead of electrons in solid state devices.<sup>[6]</sup> Various applications for such ionic circuits in biosensing and other medical technologies have been realized. For example, a bipolar membrane junction can amplify the electric field to split water and establish local pH gradients for isoelectric separation of proteins.<sup>[10,11]</sup> A permselective membrane shows a nonlinear current–voltage signature shift upon capturing target biomolecules for ion current biosensing.<sup>[9,12]</sup> Ionic transistors have been used to regulate the transport of ions and charged biomolecules by on and off switching of electrical signals in microfluidic systems.<sup>[1,2,7,8]</sup>

If these basic elements can be synthesized into massively large fluidic-based logic circuits, complex active chemical circuits can be built to allow precise spatial and temporal delivery of drugs,<sup>[8]</sup> as well as distributed detection of specific signaling ions/molecules in living organs or *in vitro* cell or tissue cultures.<sup>[5,6]</sup> These two functionalities can also be linked by feedback control via fluidic logic circuits. Such distributed fluidic-based circuitry may help decipher cell signaling dynamics to detect specific diseases such as Alzheimer's disease and Parkinson's disease,<sup>[5,6,13,14]</sup> hence allowing corresponding localized and automated drug delivery, together with smart drug screening chips.<sup>[15]</sup> In addition, the fluidic-based circuitry can facilitate the integration of massively large smart sensor array, with sequential actuation of different separation, concentration and sensing functionalities, to monitor different subsets of biomarkers and signal proteins that appear in random intervals within a galaxy of

molecules.<sup>[9]</sup> By using such medium-immersed fluidic-based sensors, actuators, and logic circuits, complex wireless or hard-wired connectivity to external solid-state integrated circuits is eliminated, thus permitting much greater versatility and larger signals in future implanted and embedded smart medical devices.

Such large-scale ionic logic circuits require a robust flip-flop latch memory element that can digitize the ion transport signals and enable robust sequential operation in a physiological fluid. Two main subgroups of ionic transistors for regulating ion transport are reported thus far: nanofluidic field-effect transistors which modulate charge density in nanochannels by tuning the electrical double layer thickness with an external gating voltage,<sup>[1,2]</sup> and ion bipolar junction transistors which control ion conductivity in a conductive polymer junction between ion-selective membranes due to ion enrichment and depletion.<sup>[7]</sup> However, they do not offer a latch element that can operate under physiological conditions, mainly because of their inability to operate in high ionic strength physiological solutions (nanofluidic field-effect transistors) or long 100 s switching times (ion bipolar junction transistors).<sup>[1,2,8]</sup> More importantly, both nanofluidic field-effect transistors with charge on–off states and ion bipolar junction transistors with voltage on–off states discharge easily in the lossy environment of a conducting physiological fluid.

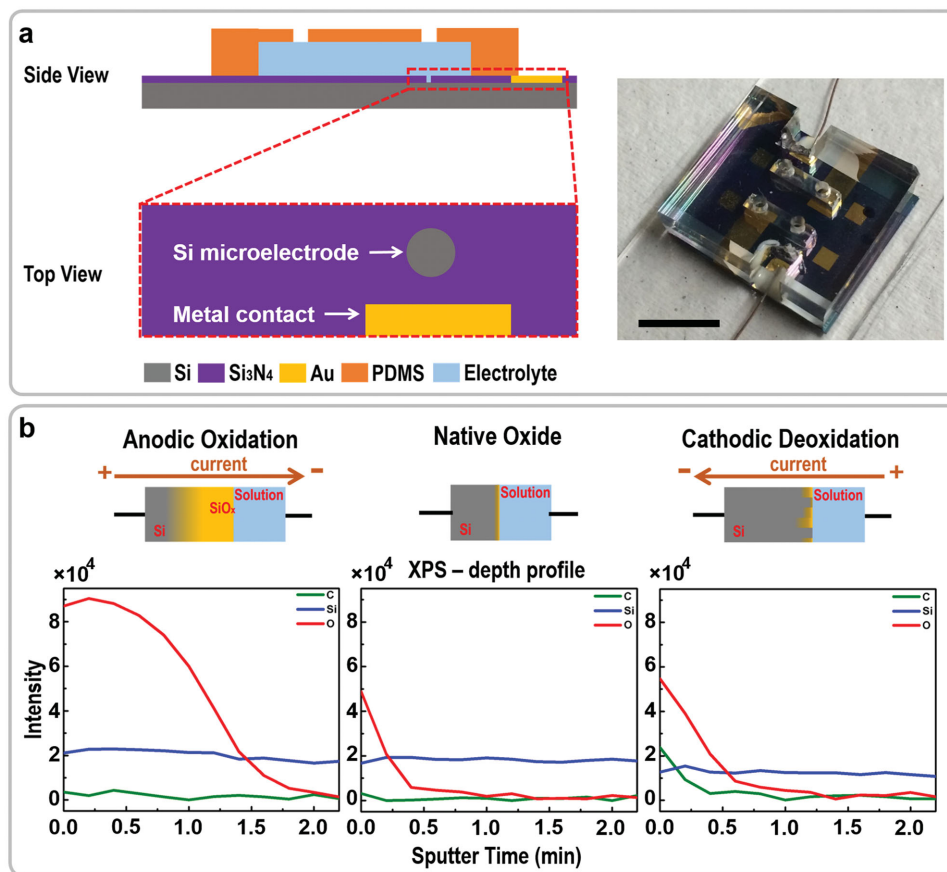
Here we report a new ionic logic element, a fluidic-based ion memristor, which can overcome the above bottlenecks to offer fast and robust flip-flop latch action for a large physiological ionic circuit. A memristor, short for “memory resistor,” is a basic electronic device whose resistance is dependent on the current or voltage history.<sup>[16–18]</sup> Hence a memristor can be converted into a bistable element with two possible resistance states, rather than the voltage states of transistor-based flip-flop elements. Conventional solid-state memristive devices are typically fabricated with a metal–insulator–metal (M–I–M) configuration, with a metal oxide, for example, TiO<sub>2</sub> or HfO<sub>2</sub>, as the middle solid electrolyte layer.<sup>[17,19–21]</sup> Nanoscale conductive filaments can grow in the insulator layer to bridge the two metal electrode layers under applied biases with a certain polarity, enabling the resistive switching.<sup>[22]</sup> In contrast, our new fluidic-based ion memristor is based on ionic currents in aqueous solutions of arbitrary ionic strength. The ionic memristor consists of a silicon microelectrode combined with an aqueous solution environment. The interfacial resistance of the silicon–electrolyte interface is switched by fluidic ion currents which induce the formation of an interfacial silicon oxide layer. Since the resistive state of the fluidic-based ion memristor does not change after the ion current inputs are withdrawn, it allows latching

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**Figure 1.** a) Schematic illustration and image of the fluidic-based ion memristor. It is made of a confined silicon microelectrode in contact with a microfluidic channel. Scale bar, 10 mm. b) The interfacial oxide layer growth or reduction at the silicon–electrolyte interface with respect to the external voltage accounts for the two resistive states of the memristive phenomenon. The XPS-depth profiles of silicon and oxygen content demonstrate the thicker oxygen-rich interfacial silicon oxide layer after anodic oxidation (left), relative to the thin layer of native oxide layer (middle) and after cathodic deoxidation (right). The sputter time indicates the depth from the silicon microelectrode surface. The carbon content shows the noise level.

with nonvolatile memory and low power consumption even in a lossy physiological solution. The rapid formation and reduction kinetics of the interfacial silicon oxide layer produces a switching time that is much shorter than ionic transistors. Moreover, we develop an ionic latch built on the fluidic-based ion memristor, along with an operation protocol for sampling upstream electrical signal from either biological systems, adjacent memristors or ion-current biosensors. It lays the groundwork for the construction of complex ionic logic circuits in fluidic systems for the various envisioned applications.

**Figure 1** presents the configuration and the resistive-state switching mechanism of the fluidic-based ion memristor. The memristive characteristic is due to a variation of interfacial resistance at the silicon–electrolyte junction when an oxide layer forms reversibly and hysterically with respect to alternating polarity of the voltage drop across the junction. The fluidic-based ion memristor is composed of a circular n-type silicon microelectrode, in contact with a polydimethylsiloxane (PDMS) microfluidic channel filled with an aqueous electrolyte, as shown in Figure 1a. The silicon microelectrode is electrically controlled via the metal contact through the silicon substrate. Platinum electrodes are inserted into electrolyte

through the top inlets of the PDMS channel to complete the electrical connection. The silicon microelectrode is fabricated with standard silicon manufacturing technology, as described in the Experimental Section and Supporting Information, Figures S1 and S2, whose size can be tuned based on different designs. The electrolyte can be an arbitrary aqueous physiological buffer solution. To demonstrate that the device is robust at high ionic strength, we have carried out our experiments in 1 M KCl buffers.

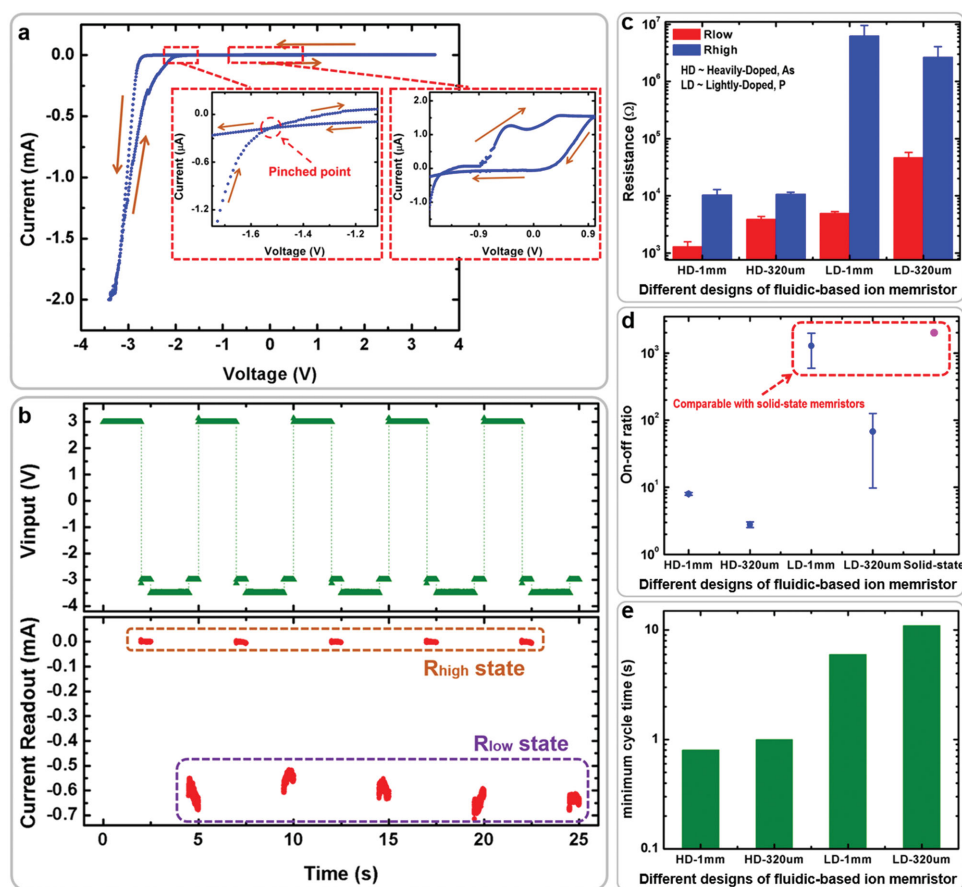
In a memristor, the switching of the device resistance is decided by certain physical state change of the device with applied voltage or current—for example, the formation of nanoscale conductive filaments across the insulator layer determines the overall resistance of most conventional solid-state memristors.<sup>[22]</sup> For our fluidic-based ion memristor, the memristive effect is due to anodic oxidation and cathodic deoxidation of the silicon microelectrode in an aqueous environment because of certain voltage or current history across the silicon–electrolyte junction.

As shown in Figure 1b, a nanoscale interfacial silicon oxide layer grows under anodic bias due to a series of possible reaction pathways:  $\text{Si} + \text{H}_2\text{O} + h^+ \rightarrow \text{SiOH} + \text{H}^+$ ;  $2\text{SiOH} \rightarrow \text{Si}_2\text{O} + \text{H}_2\text{O}$ ;  $2\text{Si}_2\text{O} \rightarrow \text{SiO}_2 + 3\text{Si}$ .<sup>[23]</sup> This thin anodic

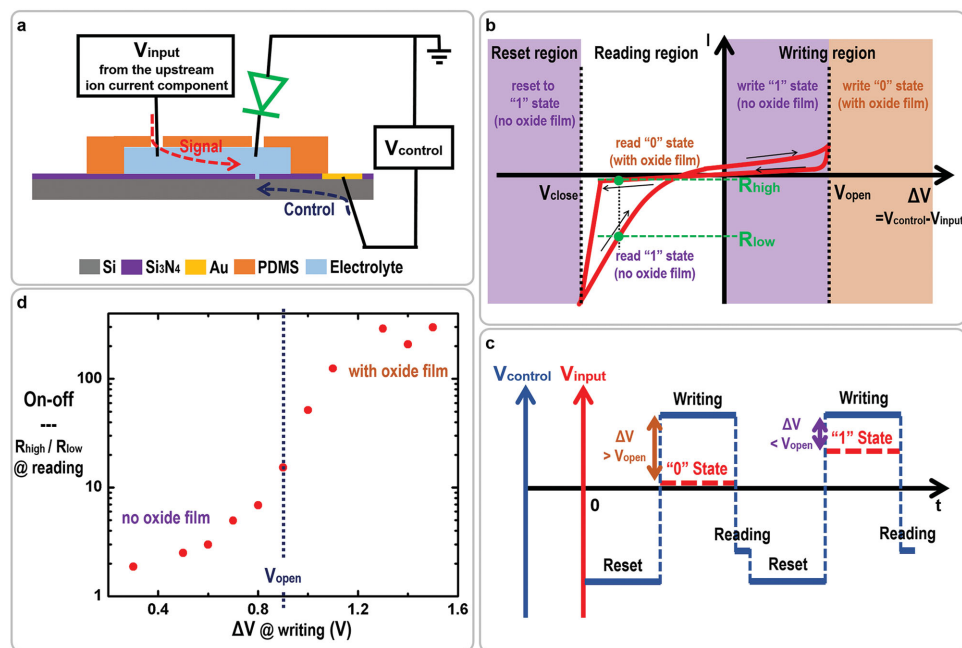
oxide layer partially blocks the electron transfer reaction at the silicon–electrolyte junction to drive the silicon–electrolyte junction to the high resistive state. When cathodic bias is then applied, the thin oxide layer is deoxidized with the possible reaction pathway:  $\text{SiO}_2 + 4e^- \rightarrow \text{Si} + 2\text{O}^{2-}$ .<sup>[24]</sup> The junction then returns to the original low resistive state. The electrochemical oxide layer growth and decomposition are confirmed with X-ray photoelectron spectroscopy (XPS) depth-profile tests. The oxide film thickness is proportional to the etching sputter time (see the Experimental Section). After the fluidic-based ion memristor is anodic biased for 10 min, a much thicker oxide layer ( $\approx 6\text{--}8$  nm) with higher oxygen content is observed on the silicon microelectrode surface comparing with native oxide layer ( $\approx 1.2$  nm, Figure 1b). The same fluidic-based ion memristor is then cathodic biased for the same amount of time. The result from the subsequent XPS depth-profile test shows that both the thickness ( $\approx 1.5$  nm) and the oxygen content of the surface oxide layer

reduced to the level of the native oxide layer (Figure 1b), which probably regrew before the XPS analysis. This analysis indicates that the presence and the thickness of surface anodic oxide layer can be tuned by switching the bias polarity applied across the silicon–electrolyte junction, hence altering the overall resistance.

The most distinct “finger print” of a memristor is the pinched hysteresis with respect to bipolar voltage scanning.<sup>[16,19]</sup> The hysteresis allows one to retain or switch the state depending on the magnitude of an input signal. It also allows one to read the state by measuring the different output signals of the two possible states of the hysteresis. The pinched hysteresis of our memristor is confirmed by cyclic voltammetry, using the silicon microelectrode as the working electrode, with a silver/silver chloride (Ag/AgCl) reference electrode right on top of the silicon–electrolyte junction through an inlet on the PDMS channel and a platinum wire into another inlet as a counter electrode. Shown in Figure 2a,



**Figure 2.** a) The pinched hysteretic current–voltage dependence demonstrates the history-dependent resistance of the fluidic-based ion memristor. The magnified insets show the pinched point and hysteresis loop at the anodic bias in the current–voltage plane. b) The reliability of performing bistable resistive-state switching by the fluidic-based ion memristor is assessed by an on–off switching test. A switching cycle containing four steps “reset”–“reading”–“set”–“reading” (the green dots in the upper panel) is applied through the silicon microelectrode. The resistance values of the silicon–electrolyte junction after “reset” or “set” are characterized by the current readout (the red dots in the lower panel), showing a distinct bistable resistive switching. c) The resistance values in two states of the fluidic-based ion memristor can be easily changed by tuning the doping and size of the silicon microelectrode to match further circuit designs ( $n = 5$ ). HD: heavily arsenic doped n-type silicon microelectrode; LD: lightly phosphorous doped n-type silicon microelectrode; 1 mm and 320  $\mu\text{m}$  are the diameters of circular silicon microelectrodes. d) The on–off ratios between two resistive states of the fluidic-based ion memristors characterize the bistable resistive-state switching ( $n = 5$ ). The on–off ratio of the fluidic-based ion memristor fabricated by 1 mm lightly phosphorous doped silicon microelectrode is comparable with a solid state memristor (the magenta dot).<sup>[26]</sup> e) The minimum cycle times of different fluidic-based ion memristors in the on–off switching test are measured to characterize the switching speed. It shows that the fluidic-based ion memristor can be toggled on and off in the order of 0.1–10 s.



**Figure 3.** a) The schematic illustration of setting the fluidic-based ion memristor into an ionic latch by connecting it in a crossbar configuration. The control voltage is applied through the silicon microelectrode while the signal potential is transmitted through the electrolyte in the microfluidic channel. b) Based on the schematic pinched-hysteretic current–voltage dependence of the fluidic-based ion memristor, the memristor is switched to the low resistive state when the  $\Delta V$  is greater than  $V_{\text{close}}$  in cathodic bias, while it is switched to high resistive state when the  $\Delta V$  is greater than  $V_{\text{open}}$  in anodic bias. c) The reset–writing–reading cycle contains three steps in one cycle: the first “reset” step switches the fluidic-based ion memristor to the low resistive state regardless the input signal; the second “writing” step decides whether to switch the memristor to the high resistive state or to leave it in the low resistive state depending on the input signal; the third “reading” step drives the value written in the fluidic-based ion memristor out to the electrolyte in the microfluidic channel again. d) The on–off ratios of the LD-320  $\mu\text{m}$  fluidic-based ion memristor, with varying  $\Delta V$  at the writing step from 0.3 to 1.5 V. The on–off ratio of the reading value is larger than 10 when the  $\Delta V$  at the writing step exceeds 0.9 V. It indicates that  $V_{\text{writing}}$  in the “writing” step should be chosen as the difference between  $V_{\text{writing}}$  and input high/low potential signal is smaller/larger than 0.9 V.

the current–voltage dependence of the silicon–electrolyte junction shows a rectified pinched hysteresis loop. A more obvious hysteresis lobe can be observed under cathodic bias. Because the majority carrier in the n-type silicon is electron, which is concentrated at the silicon–electrolyte interface as the silicon microelectrode is negatively biased, a much higher current appears when the surface oxide layer is absent.<sup>[25]</sup> The pinched point and the other hysteresis lobe under anodic bias, though insignificant, can also be found (insets of Figure 2a).

For our memristor, the hysteresis is based on how the oxide film resistance depends on the scanning voltage, which is the difference between the control (the silicon microelectrode side) and input (the fluidic side) voltages,  $\Delta V = V_{\text{control}} - V_{\text{input}}$ . The pinched hysteresis schematically shown in **Figure 3b** allows the magnitude of  $V_{\text{input}}$  and a judiciously chosen  $V_{\text{control}}$  to write a thick oxide film (state 0) with a forward jump to a positive value of  $\Delta V_{\text{writing}} > V_{\text{open}}$ , or not write one (state 1) for  $\Delta V_{\text{writing}} < V_{\text{open}}$ , and to read whether an oxide film is there with a backward jump with  $|\Delta V_{\text{reading}}| < |V_{\text{close}}|$ . A low current at the negative  $\Delta V_{\text{reading}}$  implies existence of the oxide film (state 0) and a high current the absence of it (state 1). The oxide film can also be erased by setting  $V_{\text{control}}$  to a negative  $V_{\text{reset}}$ , such that  $|\Delta V_{\text{reset}}| > |V_{\text{close}}|$ , to reset the memristor. Illustrated in **Figure 3c**, a writing protocol would then be a two step process at  $V_{\text{control}}$ , a negative  $V_{\text{reset}}$  followed by a positive  $V_{\text{writing}}$ , whereas a reading protocol would

just involve a backward jump of  $V_{\text{control}}$  to a negative  $V_{\text{reading}}$ . The voltage ramp direction (forward and backward) is important for both protocols because of the path-dependent pinched hysteresis.

We assess the reliability of this hysteretic bistable element by performing an on–off switching test. With the same three-electrode set-up as the cyclic voltammetry experiment, a sequence of “reset/set–reading” cycle is applied onto the fluidic-based ion memristor through the silicon microelectrode. In each cycle, the “reset” step is to reset the memristor to the low resistive state, while the “set” step is to set the memristor to the high resistive state. Both “reset” and “set” steps are followed by a short “reading” step to check the interfacial resistance and assess the switching. For the current design, the reset voltage is chosen to be  $-3.5$  V; the set voltage  $3$  V; and the reading voltage  $-3$  V. The resistance value in each resistive state is characterized by the current value readout. **Figure 2b** shows the input “reset/set–reading” cycle in the upper panel, and the current readout in the lower panel corresponding to each reading step. The fluidic-based ion memristor can be toggled reversibly between high and low resistive states multiple times with consistent high and low resistance values, respectively. Due to the stability of silicon oxide,<sup>[25]</sup> the memory recorded in the memristor is non-volatile—the memory does not attenuate after the memristor is disconnected from the power supply.



We can vary the two resistance values of the bistable memristor by changing the doping and the size of the silicon microelectrode. Lightly phosphorous doped and heavily arsenic doped n-type silicon microelectrodes are fabricated at two different sizes (1 mm and 320  $\mu\text{m}$  in diameter). The “reset/set-reading” cycle test is applied to these four different fluidic-based ion memristors to evaluate the resistance values from both high and low states. It demonstrates that fluidic-based ion memristors with a wide range of resistance values over three orders of magnitude can be achieved (Figure 2c). Broad-spectrum impedance matching with electronic and biological circuits is hence possible.

The on–off ratio is defined by the ratio between high and low resistance values. Ideally, we expect that the fluidic-based ion memristor can “block” all electrical signals when it is in the high resistive state, while allowing passage of all electrical signals in the low resistive state. A high on–off ratio hence facilitates binary toggling and binary memory. Lightly phosphorous doped silicon microelectrodes show higher on–off ratios, due to better insulation of the interfacial electron transfer reaction in the high resistive state, as shown in Figure 2d. It is probably because the anodic oxide layer grown on the lightly phosphorous doped silicon has a denser structure.<sup>[25]</sup> For certain design of the fluidic-based ion memristor, the on–off ratio can be higher than 1000. It is comparable with solid-state memristors used to build electronic memristor-based logic circuits,<sup>[26]</sup> and much better than any fluidic-based transistor type ionic logic devices.

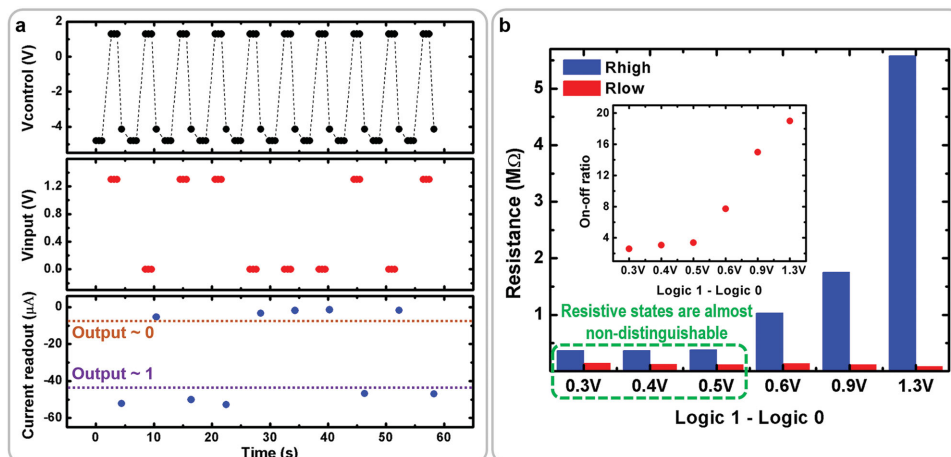
Unlike a three-terminal device such as a transistor, a two-terminal memristor can be designed to function as a memory unit in one time interval and as an arithmetic unit in another time interval—time multiplexing is used to simplify connectivity for signal transmission.<sup>[27]</sup> Therefore, the switching speed of our fluidic-based ion memristors is characterized by measuring the minimum cycle time of a “reset/set-reading” cycle in an on–off switching test, instead of the switching response time commonly measured for transistor logic devices. The switching of resistive states of the fluidic memristor is the growth or reduction of the surface oxide layer, thus too short a “reset” or “writing” step may not be able to fully reduce the existing oxide layer or grow oxide layer sufficiently to cover the entire microelectrode. Since the on–off ratio is used to characterize the switching of fluidic-based ion memristors, the minimum cycle time is defined as the shortest cycle time which can maintain the on–off ratio for a particular device. Our results demonstrate that the minimum cycle time are on the order of 0.1–10 s for fluidic-based ion memristors (Figure 2e), which is sufficiently fast for most biological dynamics, such as 20–30 s for calcium wave propagation.<sup>[28]</sup> In contrast, transistor-based ionic logic devices, such as ion bipolar junction transistors usually exhibit a switching time order of 100 s or more.<sup>[8]</sup> This rapid switching speed of fluidic-based ion memristors can be further improved by accelerating the oxidation and reduction rates of the surface layer.

An ionic latch is further built to maintain the fluidic-based ion memristor at a particular state or switch it to the other state in response to a particular ion current input. The signals can be of electrophysiological origin or from an adjacent

ionic logic device such as another fluidic-based ion memristor or an ion-current biosensor. The ionic latch is used to sample and digitize these input ion current signals by developing the proper writing and reading protocol. Due to the memristor’s nonvolatile memory, the ionic latch itself is an elementary memory cell for storing ionic logic information that can be retrieved much later with a reading protocol.

Comparing with the conventional solid-state latch based on transistor logic, where two or more transistors are needed, only one memristor is needed to build a memristor-based latch. The architecture of a fluidic-based ion memristor latch is analogous to a solid-state memristor latch.<sup>[27,29]</sup> The designed device is set and considered to be a crossbar structure:<sup>[27]</sup> the electrolyte in the microfluidic channel serves as a signal line, indicating the signal is carried by ions in fluidic environment, while the silicon substrate side acts as a control for the voltage applied through the silicon microelectrode. The fluidic-based ion memristor—the silicon–electrolyte junction, is sandwiched between the signal line (electrolyte) and the control line (silicon substrate), to complete the whole crossbar structure. As shown in Figure 3a, the silicon microelectrode is connected to one voltage source,  $V_{\text{control}}$ . Input voltage signals  $V_{\text{input}}$  from upstream ion current components, for example, the voltage shift signature from an ion-current biosensor,<sup>[9,12]</sup> are transmitted through the fluidic channel to set the state of the ionic latch. Another platinum wire electrode is placed on top of the fluidic-based ion memristor to provide the ground of the ionic latch. A diode is added to prevent grounding of the input signal. During the two-step forward writing protocol of  $V_{\text{control}}$ , the sandwiched fluidic-based ion memristor can hence convert the ionic electrical signal  $V_{\text{input}}$  into one of the two binary states. The one-step cathodic reading protocol allows the state to be identified through the measured current at  $V_{\text{reading}}$ . Unlike transistor-based latches with an input signal line and a separated output signal line, a memristor-based latch multiplex in time with a single signal line. The signal line, in our case, the electrolyte carrying the ionic information, acts as either input or output during the two-step writing or one-step reading protocols.

As was done for solid-state memristor-based latches,<sup>[27]</sup> we test our ionic latch with a sequence of three-step reset–writing–reading cycles (Figure 3c) to input and read an arbitrary sequence of binary numbers: two steps for writing and one for reading. The key to this testing cycle is the choice of  $V_{\text{writing}}$  in the “writing” step. A series of on–off switching tests used to characterize the fluidic-based ion memristor are performed to determine the minimum anodic voltage drop needed for oxide layer growth—and allow switching from low to high resistive states. The fluidic-based ion memristor with 320  $\mu\text{m}$  lightly phosphorous doped silicon microelectrode is used. In this series of tests, reset voltage in the “reset/set-reading” cycle is set constantly at  $-4.6\text{V}$ , while the set voltage (i.e.,  $\Delta V$  at the writing step) is varied from 0.3 to 1.5 V. The resistive-state switching performance corresponding to each different set voltage is characterized by the on–off ratio. Figure 3d shows that for this memristor design, when the  $\Delta V$  is larger than 0.9 V, the on–off ratio maintains a high value ( $>10$ ), indicating a sufficient growth of oxide layer to switch the memristor to the high resistive state. In contrast, for  $\Delta V$



**Figure 4.** a) Bistable latching action: a control voltage sequence is applied to the silicon microelectrode with  $V_{\text{reset}} = -4.8\text{ V}$ ,  $V_{\text{writing}} = 1.3\text{ V}$ , and  $V_{\text{reading}} = -4.15\text{ V}$  (upper panel). It contains ten reset–writing–reading cycles. An input ionic logic sequence (1011000101) is transmitted through the electrolyte in the microfluidic channel with 1.3 V for state 1, and 0 V for state 0 (middle panel). The state sampled in each latching cycle by the ionic latch is driven out in reading steps and characterized by the current readout, demonstrating the flip-flop latching action (lower panel). b) The capability to sample small input signals: the resistance values stored in the ionic latch are varied when input potential for state 1 changed from 1.3 to 0.3 V. The on–off ratios are used to characterize the performance of flip-flop latching action corresponding to different input potentials for state 1 (inset). This prototype ionic latch has an on–off ratio larger than 10 when the potential difference between binary logic values exceeds 600 mV.

less than 0.9 V, a relatively low on–off ratio ( $<10$ ) is observed due to insufficient oxide growth. Hence we can define the  $V_{\text{open}}$  as 0.9 V. Comparing  $V_{\text{open}}$  to the input potential values, we choose  $V_{\text{writing}}$  so that the difference between  $V_{\text{writing}}$  and the high/low input potential value is always smaller/larger than 0.9 V.

The result of the cyclic latching test is shown in **Figure 4a**. The ionic input potential signal fed into the ionic latch is 1.3 V for state 1, and 0 V for state 0. The operation sequence includes a  $V_{\text{reset}} = -4.8\text{ V}$  to ensure full reset to the low resistance state,  $V_{\text{writing}} = 1.3\text{ V}$ , and  $V_{\text{reading}} = -4.15\text{ V}$ . Hence the  $\Delta V$  between  $V_{\text{writing}}$  and  $V_{\text{input}}$  for the 1 state is 0 V, while the  $\Delta V$  between  $V_{\text{writing}}$  and  $V_{\text{input}}$  for the 0 state is 1.3 V, satisfying the conditions for reading and writing. The current readout retrieves the resistive state stored during the “reading” step at the end of each cycle. An input of “1011000101” is transmitted through the electrolyte in the microfluidic channel and latched into the ionic latch. The readout demonstrates that the ionic latch successfully samples and retrieves the input logic sequence (Figure 4a).

It is critical that the ionic latch can differentiate state 1 and state 0, even if the potential difference between the two states is small, as the ionic potential signal from biological systems is typically small, ranging from a few ten millivolts to a few hundred millivolts,<sup>[6,30]</sup> and the signal passed from one fluidic-based ion memristor to another may degrade due to high electrical loss of the electrolyte. Figure 4b shows the capability of this first ionic latch prototype to retrieve small or degraded input voltage signals with the designed operation principle. In a series of latching tests,  $V_{\text{input}}$  for the 0 state is set as 0 V,  $V_{\text{input}}$  for the 1 state is reduced from 1.3 to 0.3 V. The resistance values stored in the latch corresponding to different state 1 inputs are measured and the on–off ratios are calculated. It is demonstrated that this first ionic

latch prototype can perform successful latching action, distinguishing the binary input (on–off ratio is around or larger than 10), when potential difference between binary logic values is larger than 600 mV (inset of Figure 4b). Although this potential difference is still large compared with many biological potential changes, it is within the potential and current operation range of many ion-current biosensors (with operation range between hundreds millivolts to volts and tens microamperes to milliamperes).<sup>[9,12]</sup> Hence, this ionic latch can be integrated with ion-current biosensors directly to individually sample and store the sensing result, facilitating the design of large-scale multitarget biosensor arrays. By scaling down the silicon microelectrode area to increase the oxide growth efficiency,<sup>[31]</sup> the distinguishable input potential difference can further be reduced to that of action potential of individual cells. Miniaturization likely requires doping changes, since its larger  $RC$  times will result in longer oxide formation time.

We have demonstrated, to our knowledge, the first fluidic-based ion memristor for a fluidic physiological environment that can lead to large-scale integrated ionic logic circuits. We have purposefully tested our fluidic-based ion memristor with a 1 M KCl solution to demonstrate its robustness at high ionic strength. However, the formation of the oxide layer and its reduction is known to be very robust over a large ionic strength from  $10 \times 10^{-3}\text{ M}$  to at least 1 M and almost the entire range of pH.<sup>[25]</sup> It is hence a simple and robust way to realize fluidic-based ionic logic for active chemical circuits with much better performance (fast switching speed and high on–off ratio). Its fabrication involves standard silicon technology, compatible with complementary metal-oxide-semiconductor (CMOS) processes, thus making the scaling down, mass production and integration of multiple fluidic-based ion memristors straightforward, without any major modifications.

The stability/reproducibility of the design (Figures S3 and S4, Supporting Information), and easy tuning of its impedance and switching speed also facilitates large-scale integration. Characterization of the fluidic-based ion memristor shows a high on–off ratio comparable to solid-state memristors, with a switching speed much faster than any ionic transistors.

The ionic latch based on this memristor is built for sampling electrical signals from fluidic ionic system for the first time. An operation principle based on time multiplexing is designed and proved to successfully manipulate the ionic latch. The first prototype of the ionic latch shows the potential to capture ionic potential signals of only a few hundred millivolts which are within the range of voltage signals from biosensors. By scaling down in size and tuning the doping level of the silicon electrode, input signals with even lower voltage difference can be captured with faster switching rates. We hence expect immediate applications of our fluidic memristor array for remote multiplexed biosensing. Each ionic latch in the array will be individually attached to an ion-current biosensor<sup>[9,12]</sup> to provide nonvolatile memory of random transient signals from different sensors, thus permitting parallel operation of multitarget sensors and eliminating the demand of complicated equipments for data acquisition. This will likely be followed by *in vitro* autonomous sensing/delivery units embedded in cell cultures for applications in drug-testing and regenerative medicine. In the more distant future, we envision implantable or wearable units for sequential/combinatoric drug delivery that is activated by transdermal or *in vivo* monitoring of a large library of biomarkers, as well as large-scale integration with the body's neuronal circuits for prosthetics actuation and neuronal regeneration.

## Experimental Section

**Silicon Microelectrode Manufacturing:** Detailed silicon microelectrode fabrication process is shown in Figure S1, Supporting Information. Two kinds of silicon wafer (phosphorus-doping with resistivity of 1–10  $\Omega$  cm; arsenic-doping with resistivity of 0.001–0.005  $\Omega$  cm) were used for different designs. Before the process, the silicon wafers were sequentially cleaned by Piranha (3:1  $\text{H}_2\text{SO}_4$ : $\text{H}_2\text{O}_2$ , 120  $^\circ\text{C}$ , 10 min), RCA 1 (30:1:1 DI water: $\text{NH}_4\text{OH}$ : $\text{H}_2\text{O}_2$ , 70  $^\circ\text{C}$ , 10 min), and RCA 2 (30:1:1 DI water: $\text{HCl}$ : $\text{H}_2\text{O}_2$ , 70  $^\circ\text{C}$ , 10 min) followed by HF dip (50:1 DI water:HF, 10 s) to remove surface oxide. A 1  $\mu\text{m}$  silicon nitride layer was first deposited onto silicon substrates by low-pressure chemical vapor deposition (First Nano LPCVD system, 40 sccm ammonia, 0.1 slpm dichlorosilane, 0.35 Torr, 780  $^\circ\text{C}$ , 9 h 7 min), to insulate silicon substrate from the electrolyte except the silicon microelectrode region. A layer of Shipley s1813 photoresist was spin-coated onto the substrate and sequentially exposed with a mask aligner (Karl Suss MJB-3 contact mask aligners) followed by development in AZ 917 MIF. The patterned silicon nitride layer was dry-etched by  $\text{O}_2/\text{CF}_4$  plasma (Plasmatherm 790 reactive-ion-etching, 200 W, 15 min), subsequently wet-etched by phosphoric acid (160  $^\circ\text{C}$ , 30 min). This etching process exposed the metal contact regions without damaging the silicon surface. A layer of 20 nm titanium and a layer of 200 nm gold were sequentially deposited onto the substrate by e-beam evaporation (Oerlikon Leybold 8-pocket

electron-beam, dual thermal evaporation system). A second layer of photoresist (Shipley s1813) was then spin-coated and patterned by the same procedure to define the metal contact regions on the Au/Ti layer. The exposed metal layer was then wet-etched by gold etchant (Transene, Type TFA, room temperature, 90 s) and phosphoric acid (180  $^\circ\text{C}$ , 10 s, for titanium etching). A third lithography process was performed followed by the same silicon nitride etching process to define the silicon microelectrode regions. The metal contacts were finally annealed by a rapid thermal process (Allwin RTP, 600  $^\circ\text{C}$ , 30 s) to form Ohmic contact between metal and silicon.

**Microfluidic Channel Fabrication:** Detailed microfluidic channel fabrication process is shown in Figure S2, Supporting Information. The preliminary microfluidic channel mold was fabricated on a Poly(methyl methacrylate) (PMMA) sheet using a micro-milling machine (Roland IM-01 iModela). The secondary mold was casted on the PMMA mold with silicone (TAP Plastics, 10:1 Silicone:Catalyst, cured at room temperature for 24 h). Polyurethane casting resin (TAP Plastics, 1:1 Side A: Side B, cured at room temperature for 30 min) was used to make the final channel mold through the secondary silicone mold. The microfluidic channel was finally achieved by casting polydimethylsiloxane (Sylgard 184, 10:1 base:curing, cured at 70  $^\circ\text{C}$  for 2 h) onto the resin mold. The microfluidic channel and the silicon microelectrode substrate were bonded by double sided tape to complete the entire device.

**XPS Test:** The XPS experiments for analyzing silicon microelectrode surface oxide layer composition and thickness were performed by an X-ray photoelectron spectrometer (PHI VersaProbe II X-Ray Photoelectron Spectrometer). The surface chemical element contents (oxygen, silicon, and carbon) were analyzed every 12 s, while the silicon microelectrode was etched gradually by an argon ion gun (1 kV), providing the depth profile. The argon etching rate is approximately 3 nm  $\text{min}^{-1}$ .

**Electrical Characterization:** The devices were soaked and infused with aqueous 1 M KCL solution prior to use. The on–off switching test for assessing reliability and characterizing on–off ratio and switching speed of fluidic-based ion memristors were performed by an electrochemical potentiostat (Gamry Reference 600). In the latching test, the data was obtained with a Keithley 2636A Dual-Channel System SourceMeter Instrument.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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